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Suppressing Ambipolar Conduction Using Dual Material Gate in Tunnel-FETs Having Heavily Doped Drain

Dawit Burusie Abdi, Mamidala Jagadesh Kumar

***Abstract*—**In this paper, using 2D TCAD simulations, the application of a dual material gate (DMG) for suppressing ambipolar conduction in a tunnel field effect transistor (TFET) is demonstrated. Using the proposed DMG concept, the ambipolar conduction can be effectively suppressed even if the drain doping is as high as that of the source doping. Achieving this symmetrical doping, without the ambipolar conduction in TFETs, gives the advantage of realizing both n-type and p-type devices with the same doping sequences. Furthermore, the output characteristics of the DMG TFET exhibit a good saturation when compared to that of the gate-drain underlap approach. This improved behavior of the DMG TFET makes it a good candidate for inverter based logic circuits.

***Keywords*—**Dual material gate, suppressing ambipolar current, symmetrically doped TFET, tunnel FETs, PNPN TFET.

I. Introduction

THE dynamic and static power dissipations of inverter based circuits mainly depend on the operating voltage (V_{DD}) and the OFF-state leakage current, respectively. To achieve ultra-low power circuits, these sources of power dissipation must be reduced simultaneously without affecting the overall performance of the circuit. However, the limiting *kT/q* subthreshold swing (SS) of the traditional carrier injection over the barrier of metal oxide semiconductor field effect transistor (MOSFET) makes it difficult to scale down the operating voltage without increasing the OFF-state leakage current. Owing to its different carrier injection mechanism (i.e. band to band tunneling), the tunnel field effect transistor (TFET) overcomes the *kT/q* limit and becomes a potential candidate to realize ultra-low power circuits [1]-[4].

Despite its sub-*kT/q* subthreshold swing, TFET exhibits low ON-state current and ambipolar conduction which have adverse effects on the performance of circuits and makes the use of TFETs questionable for inverter based logic. The low ON-state current affects the charging and discharging time reducing the speed of the circuit. The ambipolar conduction, which is a conduction of a current for both positive and negative gate voltages, leads to malfunctioning of the inverter based logic. Therefore, improving the ON-state current and suppressing the ambipolar conduction are the main research challenges in making TFETs a real candidate for ultra-low power circuits. The focus of this paper is on suppressing the ambipolar conduction of TFETs without affecting the ON-state current. Different techniques are proposed in literature to suppress the ambipolar current in TFETs [5]-[11]. Requiring asymmetric source and drain dopings, non-saturated output characteristics, and increased gate to drain capacitance are some of the limitations of these techniques. Therefore, in this paper, using 2D TCAD simulations, it is demonstrated that the dual material gate (DMG) TFET suppresses the ambipolar current without the aforementioned adverse effects. The DMG structure has been extensively studied to improve the performance of both MOSFETs as well as TFETs [12]-[19]. However, the application of DMG for the suppression of ambipolar conduction in a TFET has not been reported. In a DMG structure, the gate is split into two regions i.e. the tunneling gate on the source side and the auxiliary gate on the drain side having different work functions. By properly choosing the work function of the auxiliary gate in a dual material gate TFET, it is shown that the ambipolar current reduces by more than four orders of magnitude even for symmetrically doped source and drain. This symmetry has the advantage of realizing both n-type and p-type devices with the same doping sequences. The proposed technique, compared to the gate-drain underlap structure, also shows improved output characteristics. To demonstrate the concept, a PNPN TFET structure is used as it exhibits a high ON-state current and a steep SS [20]-[28].

II. Devices Structure and Working Principle

The simulations are carried out for the three PNPN TFET structures shown in Fig. 1 (a) dual material gate PNPN TFET (DMG-PNPN TFET), (b) gate-drain underlap PNPN TFET (GDU-PNPN TFET) and (c) single material gate PNPN TFET (SMG-PNPN TFET). The following parameters are used in simulations: silicon film thickness t_{si} = 10 nm, gate oxide thickness (SiO_2) t_{ox} = 3 nm, channel length (L) = 50 nm, source doping (N_A) and drain doping (N_D) = 1×10^{20} cm^{-3}, channel doping $N_A = 1 \times 10^{16}$ cm^{-3}, and pocket doping $N_D = 4 \times 10^{19}$ cm^{-3}. The width of the pocket is 4 nm. For the DMG-PNPN TFET, the work functions of the tunnel gate metal (TG) and the auxiliary gate metal (AG) are ϕ_{TG} and ϕ_{AG}, respectively.

All the simulations were done in Silvaco Atlas, Version 5.19.20.R [29]. The nonlocal band-to-band tunneling (BTBT) model is used to take into account the tunneling along the

Dawit Burusie Abdi, Mamidala Jagadesh Kumar are with the Department of Electrical Engineering, Indian Institute of Technology, Delhi, Hauz Khas, New Delhi 110016, India (e-mail: dave.abdi@gmail.com, mamidala@ee.iitd.ac.in).

lateral direction. The Lombardi mobility model and band-gap narrowing (BGN) model are enabled to include the mobility effect and to take care of high doping, respectively. The Fermi-Dirac statistics and the Shockley-Read-Hall (SRH) recombination models are also enabled. As done earlier in [10], [11], [24] and [26]-[28], the simulation models are calibrated by reproducing the results in [7].

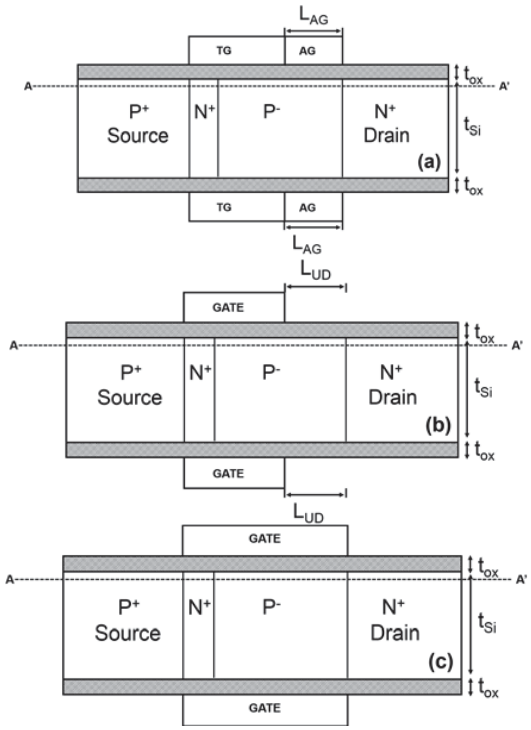


Fig. 1 Schematic view of a symmetrically doped (a) the dual material gate PNPN TFET with tunnel gate (TG) and auxiliary gate (AG). L_{AG} is the length of the AG, (b) the gate-drain underlap PNPN TFET with gate drain underlap of L_{UD} and (c) the single material gate PNPN TFET

For the n-type TFET, the ambipolar current is a current due to the narrowing of the tunneling barrier width at the channel-drain junction for the negative gate voltage. This narrowing is due to the accumulation of holes in the channel of the device. As the concentration of the accumulated holes increases, the tunneling barrier width gets narrower leading to a higher ambipolar conduction. For $V_{GS} - V_{FB} < 0$, where V_{GS} is the gate to source voltage and V_{FB} is the flat band voltage, the concentration of the accumulated holes p_{acc} increases exponentially with the surface potential ψ_s as given by:

$$p_{acc} = N_A e^{-q\psi_s / kT} \quad (1)$$

where; N_A is the channel doping, k is the Boltzmann constant and T is the temperature. For an ideal gate oxide with zero net charge density, the flat band voltage is equal to ϕ_{MS} (the work function difference between the gate metal and the semiconductor). The sign of the surface potential ψ_s in (1) has the same sign as $V_{GS} - V_{FB}$ (i.e. $\psi_s > 0$ if $V_{GS} - V_{FB} > 0$ and $\psi_s < 0$ otherwise). Therefore, if the work function of the gate metal is low, V_{FB} becomes negative and thus, more negative gate voltage is required to increase the accumulated holes exponentially.

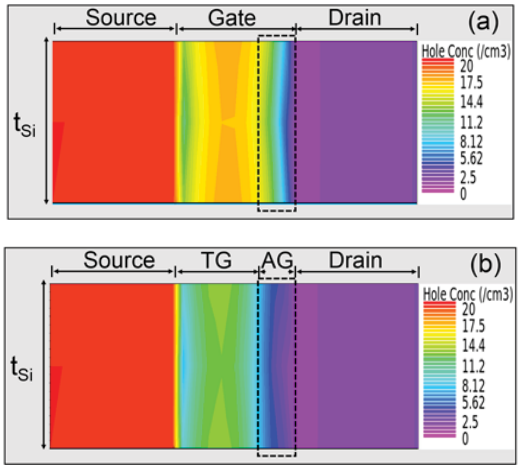
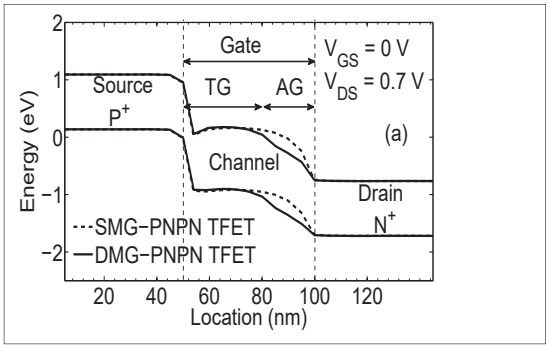


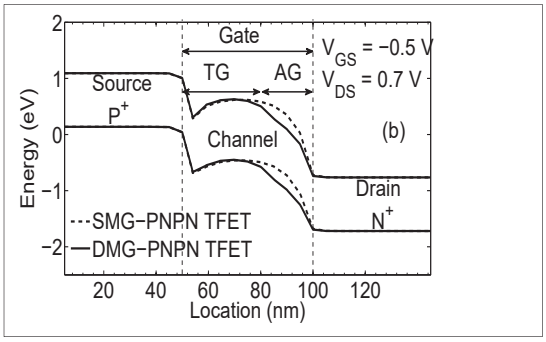
Fig. 2 Hole concentration contours at ambipolar state (V_{GS} = -0.5 V and V_{DS} = 0.7 V) for (a) SMG-PNPN TFET (b) DMG-PNPN TFET

Based on this, the idea of the proposed technique is therefore, to divide the channel into two regions so that it is possible to control the proportion of the accumulated holes in each region. According to this, the channel region under the low work function gate requires more negative gate voltage to accumulate an equal concentration of holes as that of the high work function gate. Therefore, for the same applied gate voltage, the concentration of accumulated holes is less in the channel region under the low work function gate. If the concentration of accumulated holes is less, the band bending near the channel-drain junction will be less resulting in a wider tunneling barrier width at this junction. The wider the tunnel barrier width at the channel-drain junction, the lower is the ambipolar conduction. To achieve this, therefore, an auxiliary gate metal with ϕ_{AG} = 3.9 eV and a tunneling gate metal with ϕ_{TG} = 4.4 eV are used.

Fig. 2 shows the accumulated hole concentration contour under ambipolar conditions (V_{GS} = -0.5 V and V_{DS} = 0.7 V) for the SMG-PNPN and DMG-PNPN TFET. As discussed earlier, the concentration of the induced holes in the channel (see the rectangular box in Fig. 2) under the auxiliary gate of the DMG-PNPN TFET is much less than that of the SMG-PNPN TFET. This is also reflected in the band diagram (Fig. 3) which shows a wider tunneling barrier width at the channel-drain junction for the DMG-PNPN TFET compared to the SMG-PNPN TFET in both the OFF-state and the ambipolar conditions. The band diagram is taken at the cutline 1 nm below the silicon oxide interface along the A-A' line shown in Fig. 1. This wider tunneling barrier width in DMG-PNPN TFET results in suppressed ambipolar current compared to the SMG-PNPN TFET.



(a)



(b)

Fig. 3 Energy-band profiles of the DMG-PNPN TFET and SMG-PNPN TFET at (a) OFF-state (V_{GS} = 0 V and V_{DS} = 0.7 V) and (b) ambipolar state (V_{GS} = -0.5 V and V_{DS} = 0.7 V)

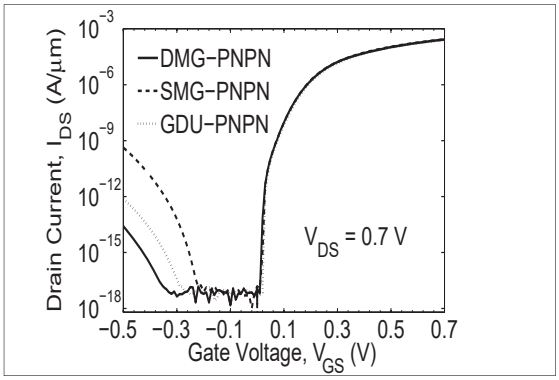
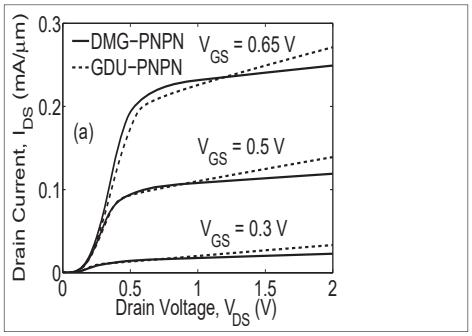


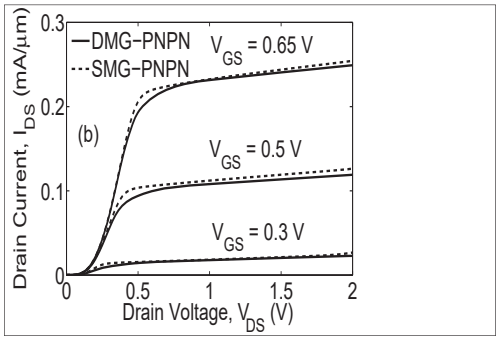
Fig. 4 Transfer characteristics of the DMG-PNPN, SMG-PNPN and GDU-PNPN TFET. Both the auxiliary gate metal length L_{AG} in DMG-PNPN and the underlap length L_{UD} in SMG-PNPN TFET are 15 nm

III. Results and Discussions

To show the effectiveness of the proposed technique, the transfer characteristics of DMG-PNPN, SMG-PNPN and GDU-PNPN TFET are shown in Fig. 4. To keep the threshold voltage of the three devices identical, the work function of the tunnel gate metal in DMG-PNPN TFET and the work function of the gate metals in GDU-PNPN and SMG-PNPN TFET are chosen to be 4.4 eV, 4.38 eV and 4.36 eV, respectively. As shown in Fig. 4, the ambipolar current of DMG-PNPN TFET is suppressed about four orders of magnitude compared to SMG-PNPN TFET and one order of magnitude compared to GDU-PNPN TFET. The underlap length L_{UD} for GDU-PNPN TFET is chosen to be equal to the auxiliary gate length L_{AG} of DMG-PNPN TFET.



(a)



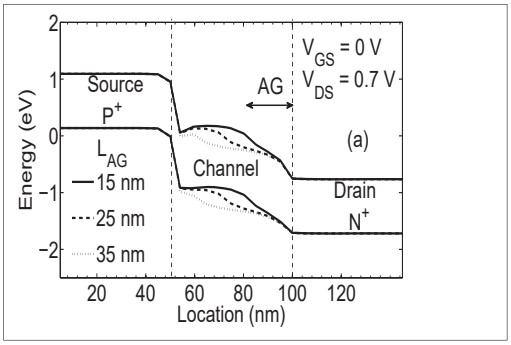
(b)

Fig. 5 Comparison of the output characteristics of (a) DMG-PNPN and GDU-PNPN TFET and (b) DMG-PNPN and SMG-PNPN TFET

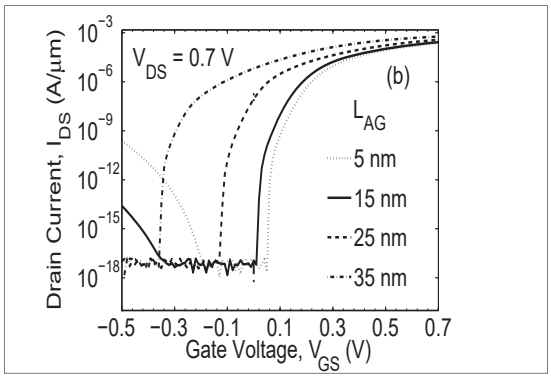
In addition to better suppression of ambipolar current, the DMG-PNPN TFET shows an improved output characteristics compared to GDU-PNPN TFET. The auxiliary gate metal in DMG-PNPN TFET modulates the conductance of the channel in the ON-state operation of the transistor. However, in the GDU approach the ungated low doped region adds a series resistance to the channel. As studied in detail by [30], [31], this resistive channel does not allow the device to have a good saturation region in its output characteristics. Fig. 5 shows the output characteristics of the DMG-PNPN, GDU-PNPN, and SMG-PNPN TFET for different gate voltages, V_{GS}. As shown in Fig. 5 (a), the DMG-PNPN TFET exhibits a good saturation compared to the GDU-PNPN TFET. This characteristic adds one more advantage to the DMG-PNPN TFET approach and makes it attractive for analog/mixed circuit design. Since both the SMG-PNPN and DMG-PNPN TFETs do not have ungated low doped region, the output characteristics of these structures exhibit good saturation as shown in Fig. 5 (b).

The length of the auxiliary gate in DMG-PNPN TFET has an impact on both the suppression level of the ambipolar current and the OFF-state current of the device. As the length

of auxiliary gate increases, though the ambipolar current still gets suppressed further, a longer auxiliary gate starts to affect the tunneling at the source-channel junction.



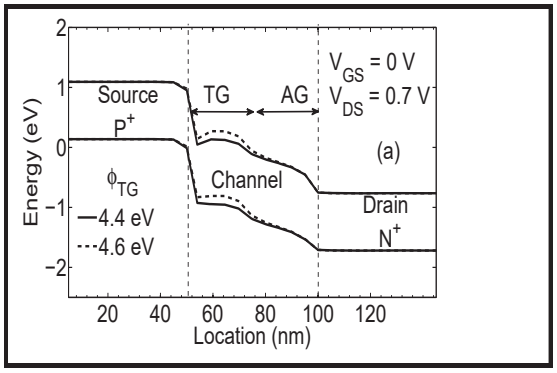
(a)



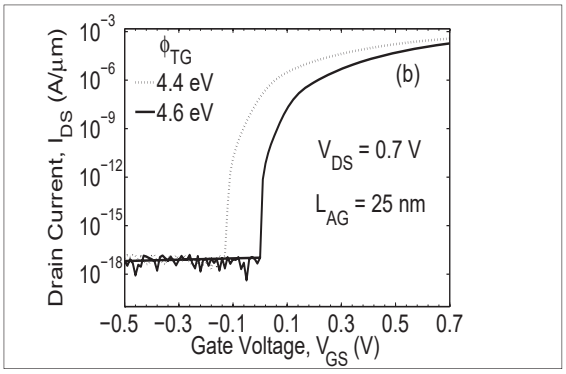
(b)

Fig. 6 (a) Energy-band profiles and (b) transfer characteristics of the DMG-PNPN TFET for different values of auxiliary gate length L_{AG}. The tunneling gate work function ϕ_{TG} = 4.4 eV and the auxiliary gate work function ϕ_{AG} = 3.9 eV

As a result, the transfer characteristics shift to the left leading to an increase in the OFF-state current due to a shift in the threshold voltage. The effect of the auxiliary gate length on the source-channel tunneling junction can be seen from the band diagram shown in Fig. 6 (a) and the shift in the transfer characteristics in Fig. 6 (b). This increment in the OFF-state current or shift of the transfer characteristics towards the left can be adjusted by increasing the work function of the tunneling gate, ϕ_{TG}. A higher ϕ_{TG} makes the energy band profile to be modulated in the OFF-state condition as shown in Fig. 7 (a). This results in a shift of the transfer characteristics so that the transistor is OFF for V_{GS} = 0 V as shown in Fig. 7 (b). Therefore, by increasing the work function of the tunneling gate, it is possible to adjust the OFF-state current for a longer auxiliary gate length.



(a)



(b)

Fig. 7 (a) Energy-band profiles and (b) transfer characteristics of the DMG-PNPN TFET for different values of tunnel gate work function, ϕ_{TG} and auxiliary gate work function, ϕ_{AG} = 3.9 eV and length L_{AG} = 25 nm

References

[1] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches," *Nature*, vol. 479, no.7373, pp. 329–337, Nov. 2011.

[3] Y. Khatami and K. Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits," *IEEE Trans. Electron Devices,* vol. 56, no. 11, pp. 2752–2761, Nov. 2009.

[4] A. C. Seabaugh and H. Lu, "Tunnel field-effect transistors – update," *IEEE International Conference on Solid-State and Integrated Circuit Technology*, no. 12, Oct. 2014, pp. 1-4.

[5] A. S. Verhulst, W. G. Vandenberghe, K. Maex, G. Groeseneken, "Tunnel field-effect transistor without gate–drain overlap," *Applied Physics Letters,* vol. 91, no. 5, pp. 053102-053103, Jul. 2007.

[6] J. Wan, C. Le Royer, A. Zaslavsky and S. Cristoloveanu, "SOI TFETs: Suppression of ambipolar leakage and low-frequency noise behavior," *Proc. European Solid-State Device Research Conference (ESSDERC)*, 2010, pp.341 – 344.

[7] K. Boucart and A. M. Ionescu, "Double gate tunnel FET with high-k gate dielectric," *IEEE Trans.on Electron Devices,* vol. 54, no. 7, pp. 1725-1733, Jul. 2007.

[8] A. Hraziia, C. Andrei, A. Vladimirescu, A. Amara, C. Anghel, "An analysis on the ambipolar current in Si double-gate tunnel FETs," *Solid-State Electronics,* vol. 70, pp. 67-72, Apr. 2012.

[9] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunnelling field effect transistors," *IEEE Trans. on Electron Devices,* vol. 57, no. 9, pp. 2317-2319, Sep. 2010.

[10] D. B. Abdi and M. J. Kumar, "Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain," *IEEE Journal of Electron Devices Society,* no. 6, vol.2, pp. 187-190, Nov. 2014.
[11] D. B. Abdi and M. J. Kumar, "Dielectric Modulated Overlapping Gate-on-Drain Tunnel-FET as a Label-Free Biosensor," *Superlattices and Microstructures*, vol.86, pp.198–202, October 2015.
[12] M. J Kumar and A. Chaudhry, "Two-Dimensional Analytical Modeling of Fully Depleted Dual-Material Gate (DMG) SOI MOSFET and Evidence for Diminished Short-Channel Effects," *IEEE Trans. on Electron Devices,* vol. 51, pp. 569-574, April 2004.
[13] G. V. Reddy and M. J. Kumar, "A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET – Two-dimensional Analytical Modeling and Simulation," IEEE *Trans. on Nanotechnology*, vol. 4, pp. 260 - 268, Mar. 2005.
[14] A. Chaudhry and M. J. Kumar, "Investigation of the Novel Attributes of a Fully Depleted (FD) Dual-Material Gate (DMG) SOI MOSFET," *IEEE Trans. on Electron Devices,* vol. 51, pp. 1463-1467, Sep. 2004**.**
[15] R. S. Saxena and M. J. Kumar "Dual Material Gate Technique for Enhanced Transconductance and Breakdown Voltage of Trench Power MOSFETs," *IEEE Trans. on Electron Devices,* vol. 56, pp. 517-522, Mar. 2009**.**
[16] S. Saurabh and M. J. Kumar, "Investigation of the Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field Effect Transistor," IEEE *Trans. on Electron Devices,* vol. 58, pp. 404-410, Feb. 2011.
[17] R. Vishnoi and M. J. Kumar, "Compact Analytical Model of Dual Material Gate Tunneling Field Effect Transistor using Interband Tunneling and Channel Transport," *IEEE Trans. on Electron Devices,* vol. 61, no. 6, pp. 1936 - 1942, Jun. 2014.
[18] R. Vishnoi and M. J. Kumar, "A Pseudo 2D-analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET," *IEEE Trans. on Electron Devices,* vol. 61, pp. 2264-2270, Jul. 2014.
[19] M. S. Ram and D. B. Abdi, "Dopingless Tunnel FET Hetero-Gate-Dielectric: Design and Analysis" *2nd IEEE International Conference on Emerging Electronics*, Dec., 2014, pp. 1-4.
[20] N. V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high performance transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013-1019, Apr. 2008.
[21] D. B. Abdi and M. J. Kumar, "In-built N^+ Pocket PNPN Tunnel Field-Effect Transistor," *IEEE Electron Device Letters,* vol.35, no. 12, pp. 1170 - 1172, Dec. 2014.
[22] A. Tura, Z. Zhang, P. Liu, Y-H. Xie, and J.C.S. Woo, "Vertical silicon p-n-p-n tunnel nMOSFET with MBE-grown tunneling junction," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1907-1913, Jul. 2011.
[23] H.-Y. Chang, B. Adams, P.-Y. Chien, J. Li, and J.C.S. Woo, "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 92-96, Jan. 2013.
[24] M. S. Ram and D. B. Abdi, "Single grain boundary tunnel field effect transistors on recrystallized polycrystalline silicon: Proposal and investigation," *IEEE Electron Device Lett.,* vol. 35, no. 10, pp. 989–991, Oct. 2014.
[25] S. Cho, and I. M. Kang, "Design optimization of tunneling field-effect transistor based on silicon nanowire PNPN structure and its radio frequency characteristics," *Current Applied Physics*, vol. 12, issue. 3, pp. 673-677, May 2012.
[26] D. B. Abdi and M. J. Kumar, "PNPN Tunnel FET with Controllable Drain Side Tunnel Barrier Width: Proposal and Analysis," *Superlattices and Microstructures*, vol.86, pp.121–125, October 2015.
[27] M. S. Ram and D. B. Abdi, "Dopingless PNPN Tunnel FET with Improved Performance: Design and Analysis", *Superlattices and Microstructures*, vol. 82, pp. 430-437, June 2015.
[28] M. S. Ram and D. B. Abdi, "Single Grain Boundary Dopingless PNPN Tunnel FET on Recrystallized Polysilicon: Proposal and Theoretical Analysis" *IEEE Journal of Electron Devices Society*, vol.3, no. 3, pp. 291-296, Jan, 2015.
[29] *ATLAS Device Simulation Software,* Silvaco Int., Santa Clara, CA, USA, 2014.
[30] A. Mallik and A. Chattopadhyay, "Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel," *IEEE Trans. on Electron Devices*, vol. 58, no. 12, pp. 4250-4257, Dec. 2011.
[31] A. Mallik and A. Chattopadhyay, "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications," *IEEE Trans. on Electron Devices*, vol.59, no.4, pp.888-894, Apr. 2012.

Dawit Burusie Abdi received the B.Sc. degree in Electrical Engineering from Jimma University, Ethiopia, in 2009; and M. Tech degree in Microelectronics, from Addis Ababa Institute of Technology, Ethiopia, in 2011. He is currently working toward the Ph.D degree with the Department of Electrical Engineering, Indian Institute of Technology, Delhi, India. His current research interests include design, simulation and modeling of nanoscale semiconductor devices.

Mamidala Jagadesh Kumar (SM '98) is a Professor of Electrical Engineering at the Indian Institute of Technology, New Delhi, India. He is the Editor-in-Chief of *IETE Technical Review* and an Editor of *IEEE Transactions on Electron Devices*. He has widely published in the area of Micro/Nanoelectronics and is known for his excellence in teaching. More details about Dr. Kumar can be found at http://web.iitd.ac.in/~mamidala