International Journal of Information, Control and Computer Sciences
ISSN: 2517-9942
Vol:4, No:8, 2010

Software Digital Phase-locked Loop for Induction Motor Speed Control

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***Abstract*—**This article deals to describe the simulation investigation of the digital phase locked loop implemented in software (SDPLL). SDPLL has been developed for speed drives of an induction motor in scalar strategy. A drive was implemented and simulation results are presented to verify the robustness against motor parameter variation and regulation speed.

***Keywords*—**Induction motor, Software Digital Phase Locked Loop, Speed control, Simulation.

I. Introduction

PHASE Locked Loop (PLL) have been applied in various fields. They are increasingly popular telecommunication systems [1]–[11] (wireless systems [2], telecom), power engineering and biological systems.

It is a buckled system which causes one signal to track another one. It keeps an output signal synchronising with a reference input signal in frequency as well as in phase. More precisely, it controls the phase of a local oscillator to that of an external signal in such a way that the phase error between output phase and reference phase reduces to a minimum [4]. There has been significant interest recently in the application of phase locked loop techniques to motor speed control. This technique provided excellent accuracy for speed regulation [5]. This type of control has been applied to DC motor [3]–[6] and in a few cases to ac induction motor [5]–[7]–[8]. Conventionally, this achieved by analog PLL [9] and classical digital PLL [10]–[12]. In this case, the output of the phase detector is seen as a continuous time voltage and this voltage is fed to analog loop filter. However, this analog feedback system is not satisfactory in some application where excellent speed regulation and fast dynamic response are required [6]. These features can be achieved performing an all digital phase locked loop implemented in software. This has the advantage of flexibility.

The objective of this paper is to develop SDPLL. This is applied to the induction motor in scalar strategy for speed drives.

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This paper is organized as follows: In the second section we give a description of the SDPLL. The third section describes the induction motor speed regulation by SDPLL. The simulated results illustrate the performances of the speed drives against parametric variation and disturbances.

II. Description of the SDPLL

The block diagram of the Software Digital Phase Locked Loop is shown in Figure 1. The basic digital phase-locked loop consists of four elements: a phase detector, a K-counter, an increment/decrement circuit and a divide by N-counter. The phase detector compares the phase of the incoming signal, Φin, with the phase of signal produced by the SDPLL, Φout, and outputs an error signal. The k-counter, which acts as the loop filter, adjusts the frequency of the digitally controlled oscillator (DCO). DCO is constituted of the increment/decrement (I/D) circuit and divide by N counter. The k-clock has a frequency of Mfc and the I/D-clock has a frequency of 2Nfc, where M is a constant, fc is the loop center frequency, and N is the modulus of the divide by N counter. The I/D-clock, frequency and divide by N modulus will therefore determine the loop center frequency.

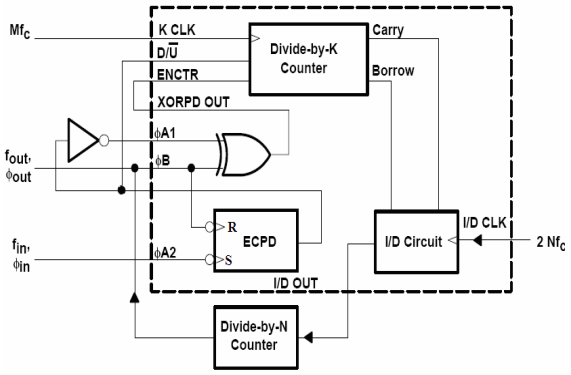


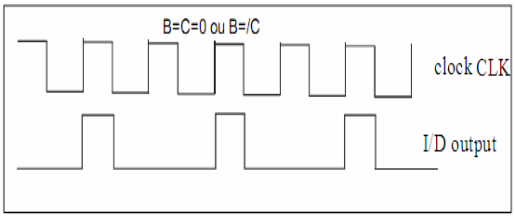
Fig. 1 Digital phase-locked loop

A. The K-counter

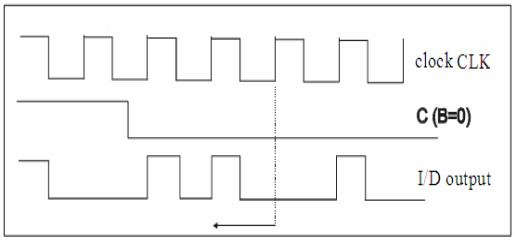
The K-counter works together with the I/D circuit to produce a signal which is fed back through the divide by N counter to the phase detector to be compared with the incoming signal. The K-counter consists of an up-counter and a down-counter with the respective carry and borrow outputs.

B. The increment/decrement (I/D) circuit

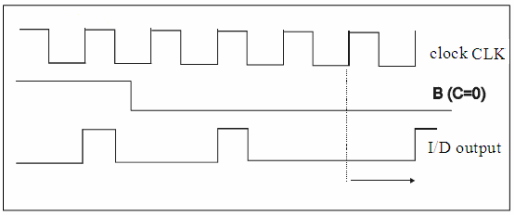
The carry and borrow outputs of the K-counter are internally connected to the increment and decrement inputs of the increment/decrement (I/D). This circuit which, in the absence of any carry or borrow pulses has an output that is one half of the input clock (I/DCP). A pulse to the decrement input causes one half-cycle to be deleted from the I/D output, while a pulse to the increment input will result in a half-cycle being added to I/D output. This is illustrated in figure 2.



(a) 1/2 of the input clock I/D CLK.



(b) 1/2 cycle added.



(c) 1/2 cycle deleted.
Fig. 2 I/D Circuit waveforms.

C. The phase detector

Two types of phase detectors are provided with the DPLL: a conventional Exclusive-Or (EXOR) gate and an Edge Controlled Phase Detector (ECPD). The ECPD is a flip-flop which functions as follows: A high-to-low transition at φ_B will produce a high-level output, while a high-to-low transition at φ_{A2} will produce a low-level output. The phase error, φ_e , is defined to be zero when the phase detector output has a 50% duty cycle. Figure 4 illustrates that for φ_e =0, the absolute phase difference between f_{in} and f_{out} is 1/4 cycle for the EXOR case and 1/2 cycle for the ECPD case. The EXOR phase detector has a gain, K_d, of 4 and phase error limit of +/- 90°. The ECPD has a k_d of 2 and a phase error limit of +/- 180°.

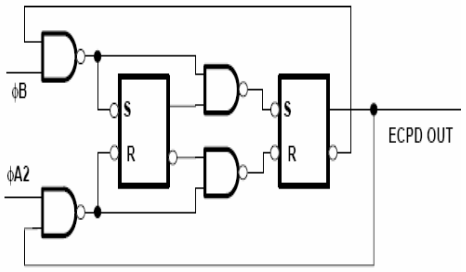


Fig. 3 Edge Controlled Phase Detector (ECPD)

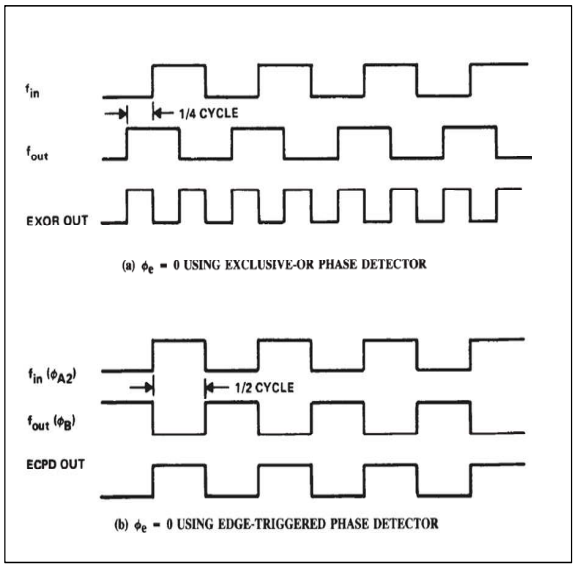


Fig. 4 Phase detector input and output with zero phase error

When the loop is hung with *Fe=Fc*, EXOR phase detector is used to disable the K-counter this circuit act to minimize ripple. So that no carry C or B is generated. If the difference in phase between Fe and Fout is worth $\pi + \Delta\phi$, the K-counter is active only when the signal:

$$X = F_{out} \oplus \overline{DU} \tag{1}$$

At the high level for one length of time $Te\frac{\Delta\phi}{2\pi}$ the K-counter receives then:

$$K_{in} = MFcTe\frac{\Delta\phi}{2\pi} \tag{2}$$

The K-counter delivers:

$$K_{out} = MFcTe\frac{\Delta\phi}{2\pi}\frac{1}{K} \tag{3}$$

For one length of time Te, the I/D circuit receives a pulse repetition frequency useful:

$$I/D_{out} = 2NFcTe - \frac{MFc}{K}\frac{\Delta\phi}{2\pi} \tag{4}$$

The loop output is:

$$Fout = Fc - \frac{MFc}{2NK}\frac{\Delta\phi}{2\pi} \quad (5)$$

From this equation we can derive the tracking frequency range:

$$\Delta Fout = Fout - Fc = \frac{MFc}{2NK}\frac{\Delta\phi}{2\pi} \quad (6)$$

At the limit of lock range $\Delta\Phi = \pm\pi$ the maximal tracking frequency range is defined as:

$$\Delta F_{out\max} = \frac{MFc}{4NK} \quad (7)$$

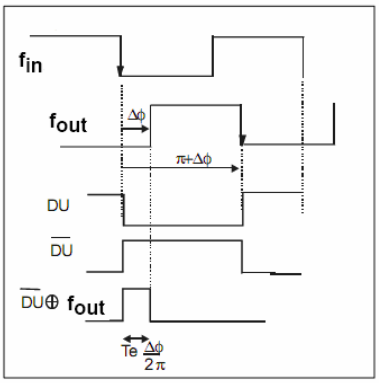


Fig. 5 The signals f_{in}, f_{out}, DU and the exclusive-OR out put

It should be noticed that the signal from the comparator of phases is exploited directly by the counter K which immediately modifies its counting rate or countdown without any integration being necessary. The pull-out range and locking range are thus confused; it is an advantage of the numerical PLL.

III. Induction Motor Drive with SDPLL

The main purpose of this work is to propose a structure control of an induction motor scalar drives using the SPLL. Precise speed control of the induction motor drives is achieved by using the software digital phase locked loop technique in feedback system. The block diagram of the total control system which has been studied and tested is shown in Figure. 6.

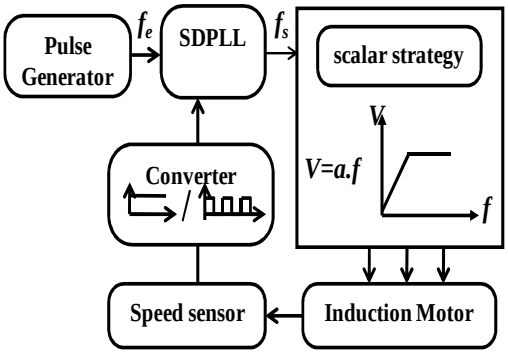


Fig. 6 Block diagram of SPLL motor control system

In this scheme, instead of comparing the frequency of the DCO with the frequency of the reference signal as in third section, the speed of the motor is compared with the reference frequency. The square wave output of the DCO determines the frequency of the scalar control signal of the induction motor and hence its speed. The transducer is a tacho generator whose output voltage signal is proportional to the motor speed. The output of this transducer is converted to square signal with converter. The square signal automatically tracks the reference frequency as target motor speed.

If the motor slows down, encoder output frequency will decrease. The digital phase detector will produce an error voltage which, after filtering, will increase the output of the DCO and compensate the scalar control signal to decrease the motor speed. The SDPLL forces the motor speed to synchronize with the reference digital pulse train, thus enabling a precise speed control of the drive system.

IV. Simulation Results

We present in this section the simulation results of the SDPLL. The system is simulated under MATLAB Software Package. The tests carried out confirm the robustness of the proposed control scheme.

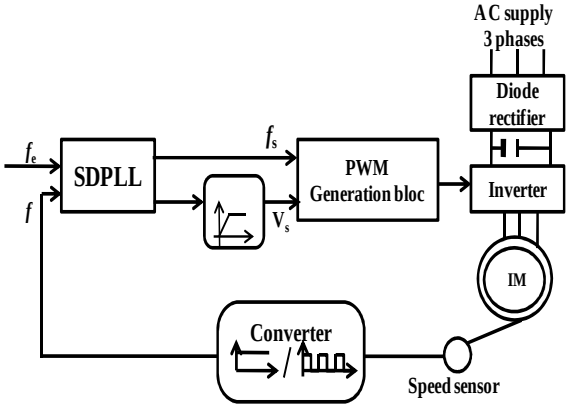


Fig. 7 Block diagram of SDPLL motor control system

The reversal speed response of the induction motor is shown in Fig. 8 (a). The speed tracks precisely the reference values of speed targets. The fig. 8. c shows the speed error which is obtained as the difference between the desired input signal and the actual system output that tends towards zero. The fig. 8. b shows the control signal.

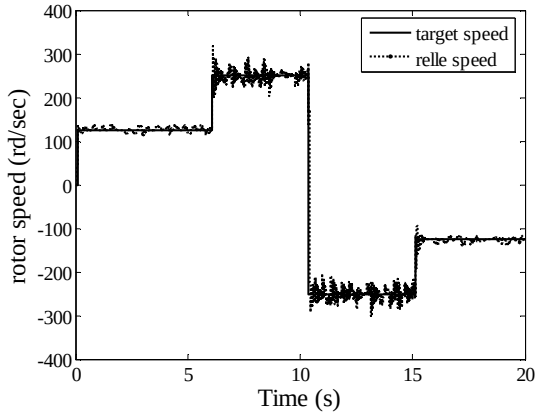


Fig. 8 a Motor speed response with a variable target speeds

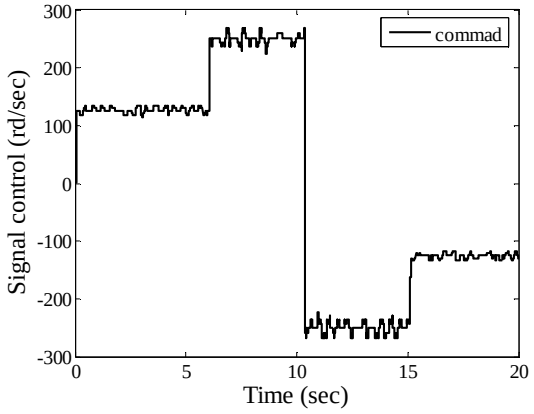


Fig. 8 b. Signal control

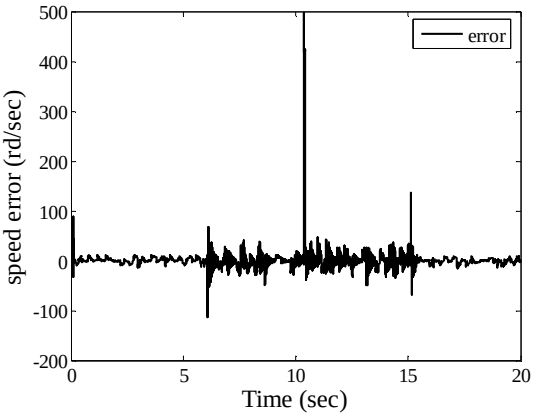


Fig. 8 c Speed motor error

Fig. 9 presents the speed responses of the proposed control; Figure. 9.a presents the simulation result of motor speed response under disturbance. Fig. 9. b shows the command speed. Fig. 9. c shows the speed error of the proposed control scheme. A rated load torque of 5 Nm is applied to the induction motor at time 2 s. The application of the load torque creates a disturbance on the output of the model. This disturbance is rejected and the regulation remains precise.

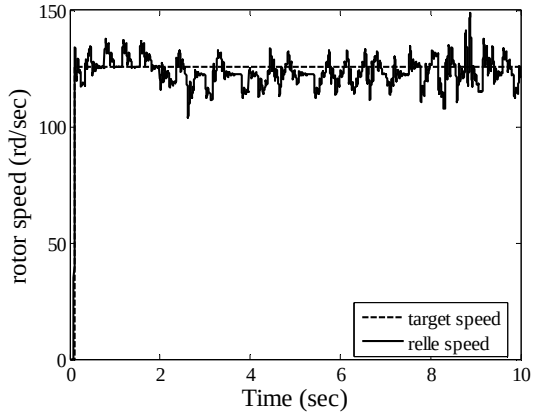


Fig. 9. a. Motor speed response under disturbance

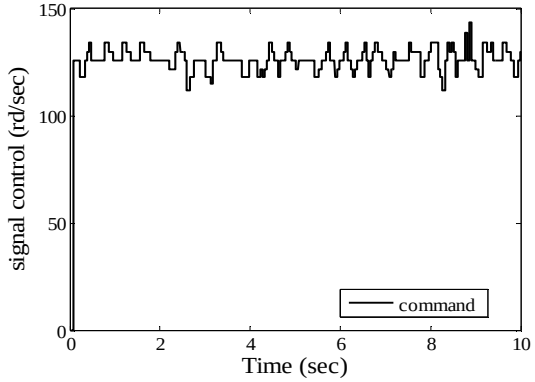


Fig. 9 b. Motor speed control response under disturbance

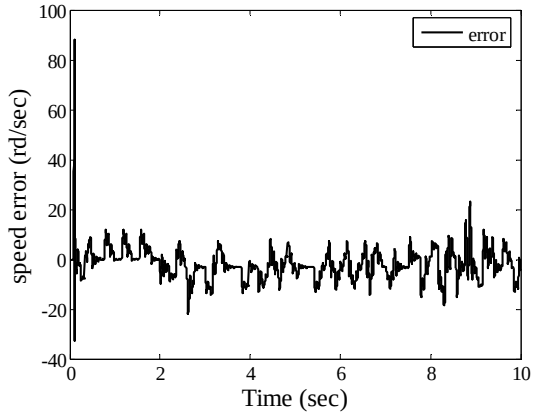


Fig. 9 c. Motor speed error response under disturbance

The fig. 10. a shows the behaviour of the induction motor speed under a rated load torque at time 2 s and a variation of the rotor resistance from actual Rr to 1.5Rr at time 10 s. The fig. 10. c shows the speed error which is obtained as the difference between the desired input signal and the actual system output that tends towards zero. The fig. 10. b shows the control signal dynamics.

The results show the robustness of the control law under external disturbances and parameters variations.

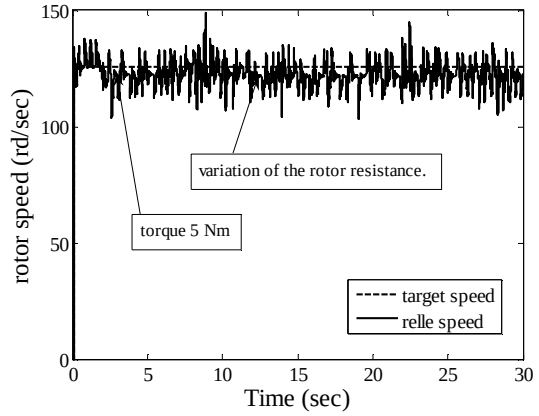


Figure. 10 a Simulation result of motor speed response

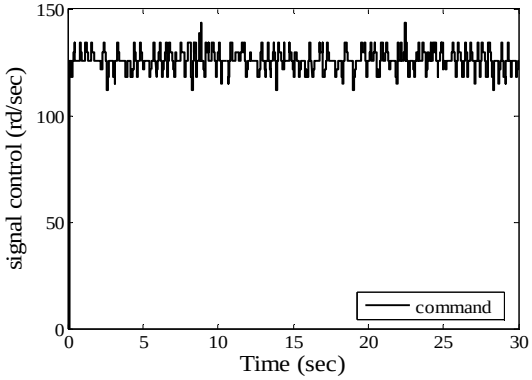


Fig. 10 b Motor control response

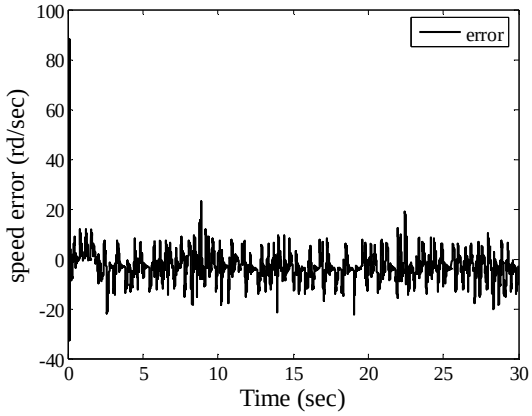


Fig. 10 c. Motor speed error response

V. Conclusion

In this paper, software digital phase-locked loop technique for the speed control of an induction motor scalar drives is presented using scalar strategy, where satisfactory results were obtained. The control system possesses high performance including the precise speed regulation, robustness to the motor parameter variations and insensitivity to the torque disturbance. Simulation results were verified to prove the validity of the proposed system.

VII. Appendix

Induction motor parameters:

Power	P_{rat}=1 Kw
Nominal voltage	U_{rat}=220/380 V
Frequency	f_{rat}=50 Hz
Stator resistance	R_s=2.3 Ω
Rotor resistance	R_r=1.5 Ω
Stator induction	L_s=261 mH
Rotor induction	L_r=261 mH
Number of pair pole	n_p=2
Inertia moment	J=0.0076 Kgm^2
Friction factor	f=0.0007 N.m.s/rad

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