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Simulation Study of Lateral Trench Gate Power MOSFET on 4H-SiC

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***Abstract*—**A lateral trench-gate power metal-oxide-semiconductor on 4H-SiC is proposed. The device consists of two separate trenches in which two gates are placed on both sides of P-body region resulting two parallel channels. Enhanced current conduction and reduced-surface-field effect in the structure provide substantial improvement in the device performance. Using two dimensional simulations, the performance of proposed device is evaluated and compare of with that of the conventional device for same cell pitch. It is demonstrated that the proposed structure provides two times higher output current, 11% decrease in threshold voltage, 70% improvement in transconductance, 70% reduction in specific ON-resistance, 52% increase in breakdown voltage, and nearly eight time improvement in figure-of-merit over the conventional device.

***Keywords*—**4H-SiC, lateral, trench-gate, power MOSFET.

I. Introduction

SILICON CARBIDE (SiC) has been recognized as a promising semiconductor material for high-voltage, high-power, high-frequency, and high-temperature devices because of its superior properties such as wide band-gap, high breakdown field, high saturation velocity, and high thermal conductivity leading to reduced power dissipation and cooling requirements [1]. Among various polytypes of SiC, 4H-SiC is most suitable polytype for power devices due to its higher bulk mobility, small anisotropy, and increasing maturity of material quality. 4H-SiC power metal-oxide-semiconductor field-effect transistor (MOSFET) is one of the promising devices for a variety of power electronics applications. The desirable features of a power MOSFET are higher drain current, low threshold voltage, low ON-resistance, high transconductance, high breakdown voltage, and high switching speed. In a conventional power MOSFET, designer has to make a trade-off between these parameters because they are related with each other. There are reports on 4H-SiC lateral power MOSFETs [2], [3] which utilize the reduced-surface-field (RESURF) techniques to improve the trade-off between breakdown voltage and ON-resistance. Although, RESURF techniques reduce the electric field along the surface in lateral power devices to improve breakdown voltage while minimizing the drift region resistance. However, the presence of drift region near the surface limits ON-resistance in lateral devices. On the other hand, concepts of trench-gate structures have effectively demonstrated [4]–[6] to enhance the output current, reduce threshold voltage and ON-resistance, improve breakdown voltage and switching speed in lateral power MOSFETs on Si. In literature, attention has not been given to investigate the performance of a lateral trench-gate power MOSFET structure on 4H-SiC. Therefore, motive of this work is to evaluate the performance of a lateral trench-gate power MOSFET (LTGMOS) structure on 4H-SiC.

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II. Device Structure and Design Aspects

Fig. 1 shows the cross-sectional view of unit cells of a conventional and proposed LTGMOS structure implemented on 4H-SiC with semi-insulating substrate. The conventional lateral-diffused MOSFET (CLDMOS) structure is utilizing a field-plate over the drift region to improve breakdown voltage. In LTGMOS structure, the source contact is taken at top and center of the structure and two n^+ polysilicon gates are placed in two trenches on both sides of P-body region. The drain contacts are provided on outer sides of unit cell. A positive gate voltage higher than the threshold voltage creates two parallel channels in P-body region resulting increased drain current (I_D). The presence of two parallel gates also provides improvement in transconductance (g_m) and reduction in specific ON-resistance ($R_{on\text{-}sp}$) and threshold voltage (V_{th}).

TABLE I
Structural Parameters Used in Simulation

Parameter	Symbol	Units	CLDMOS	LTGMOS
Cell pitch	L	µm	6.0	6.0
Gate length	L_G	µm	0.5	0.5
Gate oxide thickness	t_{ox}	µm	0.03	0.03
Field-plate length	L_{FP}	µm	1.5	-
Oxide thickness 1	t_{ox1}	µm	-	0.5
Oxide thickness 2	t_{ox2}	µm	-	0.8
Oxide thickness 3	t_{ox3}	µm	-	0.2
Oxide thickness 4	t_{ox4}	µm	-	0.2
Drift region length 1	L_1	µm	-	1.55
Epilayer thickness	t_{epi}	µm	0.65	2.0
Drift region doping	N_d	cm^{-3}	$1x10^{16}$	$4x10^{16}$
P-body doping	-	cm^{-3}	$1x10^{17}$	$1x10^{17}$

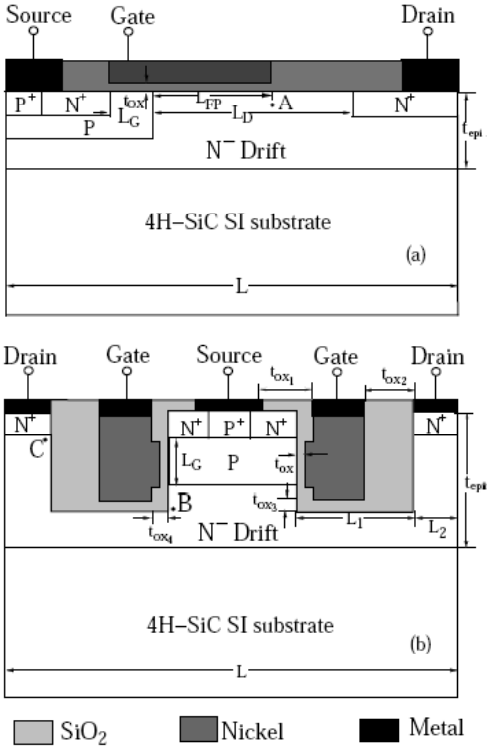

Fig. 1 Cross-sectional view of unit cell (a) CLDMOS and (b) LTGMOS

Further, in case of the CLDMOS, the breakdown of structure occurs in drift region at the end of field-plate (point 'A' marked in Fig. 1 (a)). On the other hand, trench structure of the LTGMOS causes RESURF effect in the device and a reduced peak electric field occurs in the drift region at points 'B' and 'C' as marked in Fig. 1 (b). This results in large improvement in breakdown voltage (V_{br}) of the proposed structure. The structural parameters used in simulation for both the devices are given in Table I. The drift region doping of two structures is optimized to obtain maximum breakdown voltage while keeping the electric field inside the oxide below 4 MV/cm [7]. A reduced electric field effect in the proposed structure allow higher drift region doping as compared to the conventional device for same cell pitch.

III. Simulation Results and Discussion

The performance of CLDMOS and LTGMOS structures are compared using two-dimensional simulations in device simulator, ATLAS [8]. Fig. 2 shows simulated output characteristics of the CLDMOS and LTGMOS devices. It is observed that for all gate voltages (V_{GS}), the drain current of LTGMOS is higher than that of CLDMOS device. This is due to formation of two channels in the proposed device. At V_{GS}=8V, the I_D of proposed and conventional devices are found to be 14.8 and 7.2 μA/μm, respectively i.e. output drain current of proposed device is double as compared to conventional device.

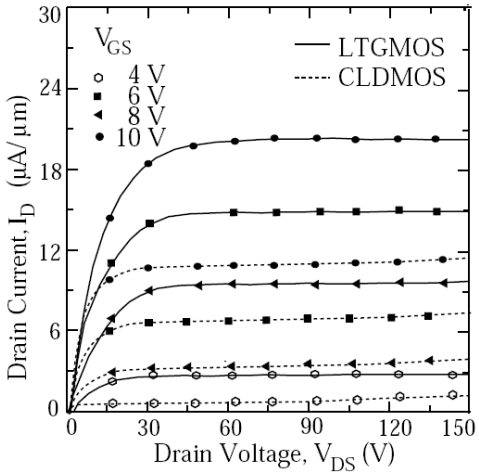

Fig. 2 Output characteristics of CLDMOS and LTGMOS

The transfer characteristics of both structures are shown in Fig. 3. These characteristics are used to calculate the threshold voltage of device which is taken as the intercept of a tangent drawn at the point of maximum slope of the curve with the gate voltage axis. V_{th} of LTGMOS and CLDMOS devices are observed to be 3.49 and 3.92 V, respectively, which gives 11% reduction in V_{th} of proposed device as compared to CLDMOS. The lower value of V_{th} of proposed structure indicates that I_D in the device reaches a predefined level (usually taken as 250μA for power MOSFETs) at relatively lower gate voltage as compared to CLDMOS. The transconductance curves of both the devices are also shown Fig. 3. As seen, the proposed device exhibits higher g_m i.e. a better control of gate over drain current. Peak g_m of LTGMOS and CLDMOS devices are obtained as 283 and 166 μS/μm, respectively, resulting 70% increase in peak g_m. Higher g_m of the proposed device is due to increased drain current and reduced $R_{on\text{-}sp}$.

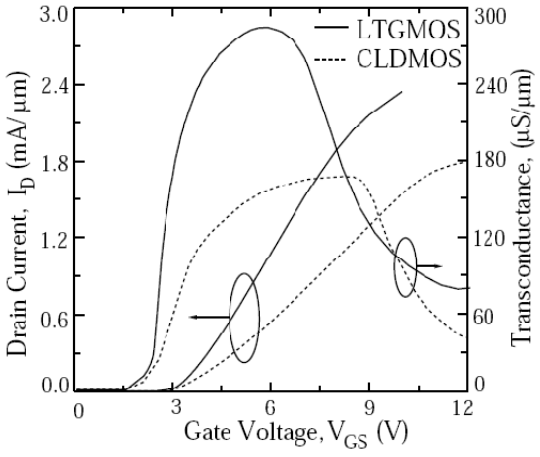

Fig. 3 Transfer and transconductance characteristics of CLDMOS and LTGMOS

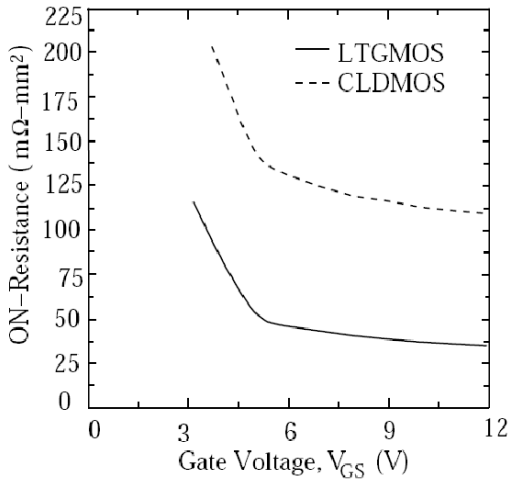

Fig. 4 ON-resistance variation with gate bias voltage of CLDMOS and LTGMOS

Fig. 4 shows ON-resistance variation with gate bias voltage for both the devices when low drain voltage (V_{DS}=0.5V) is applied so that device operates in linear region. At V_{GS}=12V, $R_{on\text{-}sp}$ of LTGMOS and CLDMOS devices is found to be 33 and 111 mΩ.mm^2, respectively i.e. the proposed device provides 70% lower $R_{on\text{-}sp}$ as compared to the conventional device. Reduction in $R_{on\text{-}sp}$ is due to increased drain current and higher drift region doping in proposed structure.

Fig. 5 shows the breakdown characteristics of the LTGMOS compared with that of CLDMOS under off-state. It is seen that V_{br} of LTGMOS and conventional structures is 510V and 335V, respectively, resulting 52% improvement in V_{br}.

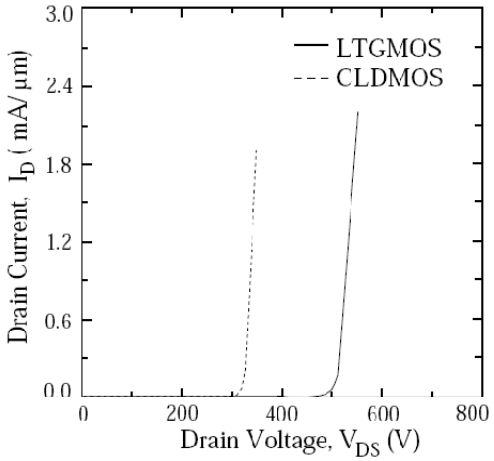

Fig. 5 Breakdown characteristics of CLDMOS and LTGMOS

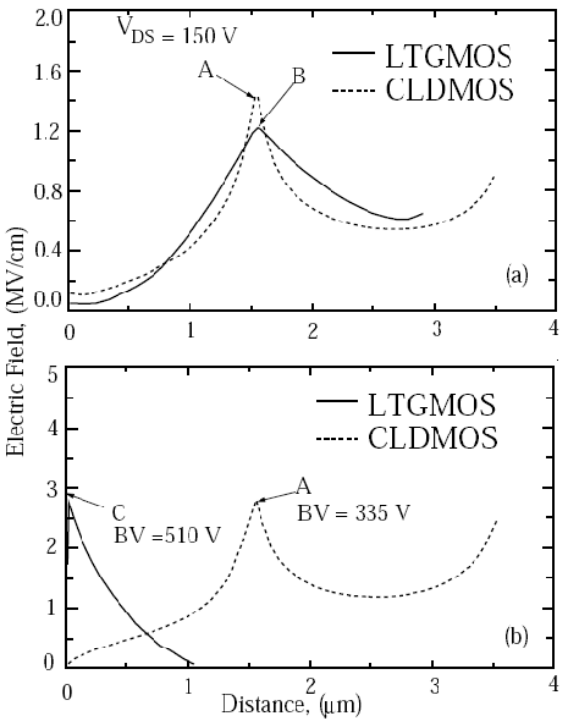

Fig. 6 Electric field (a) at V_{DS} = 150V and (b) at breakdown

In our simulation, it is seen that in case of CLDMOS, the electric field responsible for breakdown peaks on the surface in drift region at point 'A' i.e. at the end of field-plate. On the other hand, a reduced peak electric field is shifted to points 'B' and point 'C' in the proposed structure.

Fig. 6 shows the variation of electric field in the drift region at V_{DS}=150V and at breakdown. It can be seen that at V_{DS}=150V, the peak electric field occurring at point 'B' in proposed structure is lower than that of CLDMOS at point 'A'. However, at breakdown, the peak electric field in both the devices is equal resulting breakdown of CLDMOS and LTGMOS at point 'A' and 'C', respectively.

For better understanding of field distribution in devices, Fig. 7 shows 2D electric field distribution in both the structures at V_{DS}=150V. As seen, in CLDMOS device, the peak electric field in drift region is at point 'A' whereas a reduced peak electric field shifts to point 'B' for the LTGMOS. However, as shown in Fig. 8, the peak electric field at breakdown occurs at point 'A' and 'C' in CLDMOS and LTGMOS, respectively.

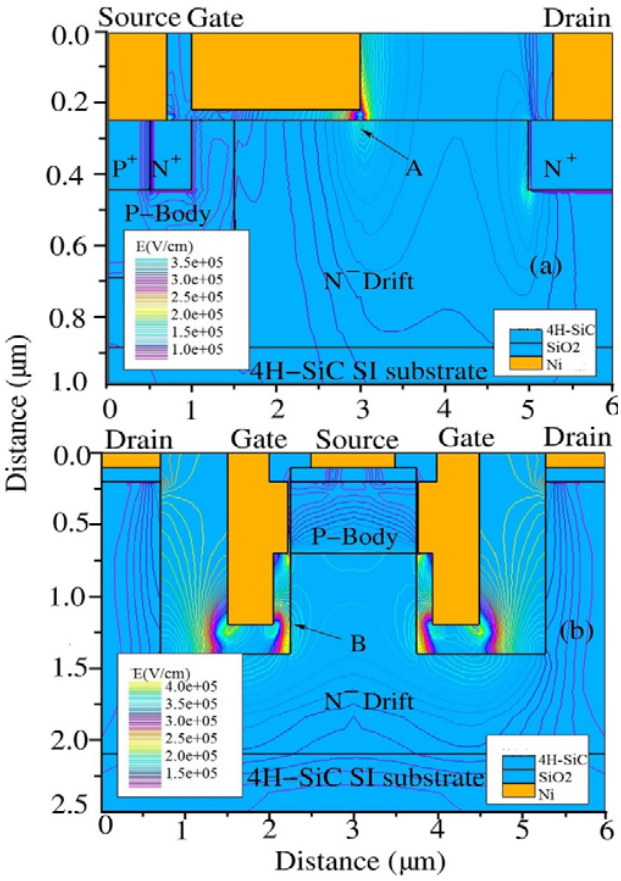

Fig. 7 Two-dimensional electric field distribution at V_{DS}=150V in (a) CLDMOS and (b) LTGMOS structures

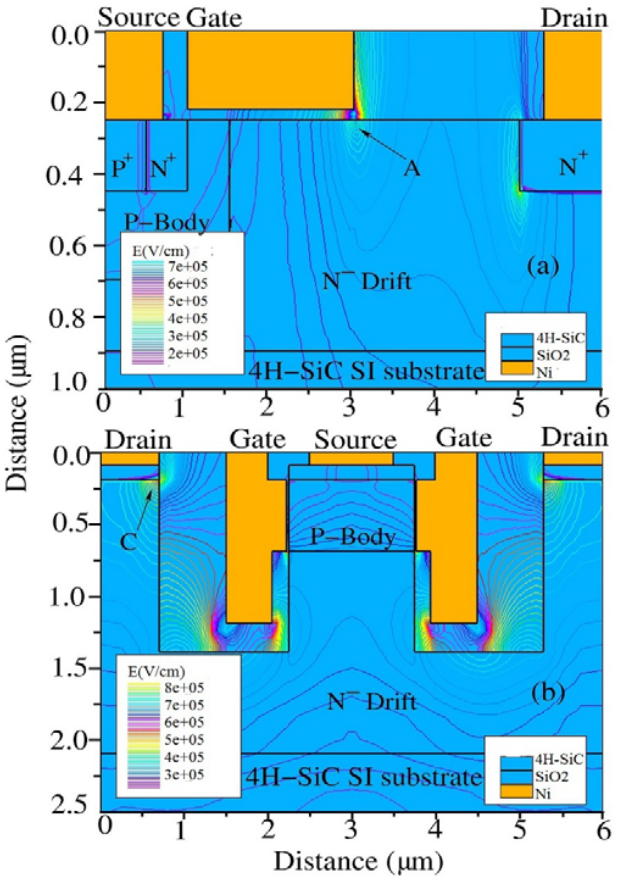

Fig. 8 Two-dimensional electric field distribution at breakdown in (a) CLDMOS and (b) LTGMOS structures

As discussed above, the proposed structure exhibits lower $R_{on\text{-}sp}$ and higher V_{br} as compared to the conventional device. The overall effect is that there is a large improvement in figure-of-merit ($FOM=V_{br}^2/R_{on\text{-}sp}$) of the LTGMOS. The FOMs of CLDMOS and LTGMOS are calculated as 101 and 788 MW/cm^2, respectively, resulting nearly eight times improvement in FOM.

IV. Conclusion

An integrable lateral power MOSFET structure called LTGMOS on 4H-SiC has been presented. The proposed device is having a trench-gate structure which enhances the current conduction and causes RESURF effect in the device. Based on 2D simulations, it is demonstrated that the proposed device exhibits two times improvement in output current, 11% decrease in threshold voltage, 70% increase in transconductance, 70% reduction in ON-resistance, 52% increase in breakdown voltage, and nearly eight times improvement in figure of merit as compared to the conventional lateral power MOSFET for the same cell pitch.

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