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Self Compensating ON Chip LDO Voltage Regulator in 180nm

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***Abstract*—**An on chip low drop out voltage regulator that employs elegant compensation scheme is presented in this paper. The novelty in this design is that the device parasitic capacitances are exploited for compensation at different loads. The proposed LDO is designed to provide a constant voltage of 1.2V and is implemented in UMC 180 nano meter CMOS technology. The voltage regulator presented improves stability even at lighter loads and enhances line and load regulation.

***Keywords*—**Analog, LDO, SOC.

I. Introduction

THE usage of the battery power devices in today's global village has become so pervasive that it has become almost indispensable in almost every walk of life. This accentuated the demand for low-voltage, low-dropout linear regulators (LDOs) [1]. These regulators primarily provide a reliable, constant output voltage to cater the different requirements of small sub-circuits, while extending battery-life in portable applications. These LDOs offer protection and filtering from electrical transients and noise. These features allow LDOs the preferred power management solution for applications where a low dropout voltage and low output current are required, either stand alone or in tandem with the switching regulators. Most common loads driven by LDOs include mobile phones, digital cameras, microcontrollers, memory chips.

This paper focuses design of LDO voltage regulator with improved efficiency and good transient response. In this LDO, the pass element is employed in common source configuration as against the common drain in the case of conventional voltage regulators. Improved efficiency relative to the conventional regulators is achieved by replacing the common-drain pass element with a common-source one to reduce the minimum required voltage drop across the control device [2]–[6]. The consequence of low voltage drop across the pass element is that the overall power dissipation is reduced. This facilitates the design of a low voltage, on chip regulator.

The conventional voltage regulators make use of large off chip capacitors (refer fig.1) in the micro farad range inorder to tackle stability problems. This mandates the provision of external pin. On chip LDO proposed in [3] gets rid off this problem. But it is not effective at all load currents. The off chip LDO while facilitating SOC design requires deft compensating scheme. Another off chip LDO [7] makes use of a fast path that does both compensation and improving transient response. This forces the design less flexible as it can not be tailor made to suit different requirements of the various subsections of mobile phone. Hence a compensation scheme is presented in section II, which takes care of this issue. Testing of the scheme and results of 180nm UMC LDO with 1.8 power supply are presented in section III. Finally concluding remarks are given in section IV.

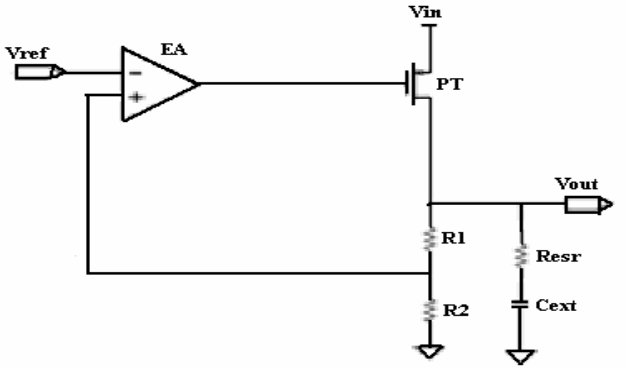

Fig. 1 OFF chip LDO regulator with CS pass element

II. Compensation Scheme

Most of the LDO specifications are greatly affected when the external capacitor is reduced by several orders of magnitude. The most significant side effect is stability degradation. The uncompensated capacitor-less LDO has two major poles, the error amplifier output pole, P1, and the load dependent output pole, P2. The standalone error amplifier has a pole located at relatively high frequency. The equivalent pass transistor input capacitance adds significant capacitance to the error amplifier output impedance. The pass transistor is very large in order to reduce VDSAT. Therefore, CGS and CGD are extremely large, in the tens of pico farads. The second pole, P_2, is located at the LDO's output. The output resistance decreases for increasing load current. P_2 is directly proportional to the load current and is load dependent. High load current pushes the output pole P_2, to higher frequency, and the capacitor-less LDO regulator is usually stable. At low currents, the effective load resistance increases significantly. P_2 is pushed to lower frequency in close proximity to the error amplifier pole. Stability cannot be guaranteed due to the

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decreased phase margin. The uncompensated capacitor-less LDO regulator is not stable at low currents, especially at the no-load condition. Hence compensation is necessary. The pole P_1 due to error amp O/P and large pass transistor is given by $1/(2.\pi.r_{o\cdot err.amp}.C_{Geff.(pass\ tst)}$. The pole P_2 which is at LDO output node is given by $1/(2\ \pi.C_L\ \ r_o)$. Consider the following two cases as I_{load} varies:

Case (i) Lighter Load conditions

As I_L decrease, r_o of the pass transistor increases. P_2 moves to lower frequencies and CGS variation is nominal as long as the transistor is in saturation. For NO LOAD current, $r_{o\ pass\ transistor}$ is maximum and C_{GS} is minimum. This is the consequence of two factors. The channel extinguishes since gain tends to zero and second reason being the withdrawal of miller effect. This moves P_1 to higher frequencies. Thus phase margin becomes very poor. Under these conditions the phase margin is observed to be 12^o for 180nm UMC technology. The above problem is solved by creating ZERO (R_z , C_z) at the error amplifier-pass transistor gate node that counters P_2, improving phase margin. This results in a creation of doublet, since an additional pole P_3 is also created as byproduct. Rz Cz is chosen to be nearer to P_2 (3-5 times away from P_2). The new pole P_3 generated due to the addition of compensating zero should be placed "AWAY from the new compensating zero". Since Rz is same for both compensating zero and new pole P_3 , Cz is chosen to be 'n' times greater than Cpass transistor so that the zero (1/CzRz) is located 'n' times LOWER to the new pole P_3. Hence Cz is chosen at least 10 times greater than pass transistor gate capacitance for no load current.

$$C_z = 10.\ (CGS@NO\ LOAD) = 10\ (5pF) = 50pF$$

Notice that Pole P_1 (now formed with Cz and error amplifier output impedance) is STILL DOMINANT since $C_z > C_{pass\ transistor}$

Locations:

x P1:(EA Output impedance||CzRz) ***x*** P2(LDO O/P) ***o*** Z (Rz Cz) ***x*** P3

Case (ii) Heavier Load Conditions

The compensating zero created is NOT required at high load currents, since the pole P_2 due to LDO output moves away from P_1 as load impedance decreases. At high load currents,

$C_{pass\ tst}$ >> Cz (created)

Then both zero and pole P_3 will be located approximately at the same frequency. Careful experimental observation and thorough mathematical analysis revealed that the zero which is unwanted now is cancelled by P_3 . Thus the device capacitance helps in getting rid off the zero created to counter the pole movement at no/low load currents which can be termed as **self compensation** since the device adapts itself to load variations.

III. Results

The block schematic for the proposed LDO is shown in Fig. 2.

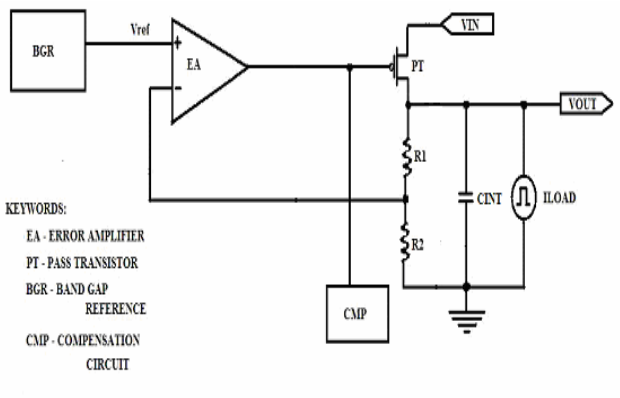

Fig. 2 Block schematic of the proposed LDO

The circuit is simulated using UMC 180nm technology. Fig. 3 reveals that uncompensated LDO at no load current exhibits very poor phase margin on the order of 12^o. It can be seen from Fig. 4 that the LDO exhibits good phase margin at full load current. Hence, one needs to compensate at load currents, but it is not necessary at high load currents. The proposed scheme adapts to the changes in the load currents and without any explicit efforts, the compensation done at no load currents will extinguish at high load currents as desired. This is demonstrated through the sub sequent results. The ac response of compensated LDO is shown in the Fig. 5 through Fig. 8 for different load currents from 50mA to no load current. It can be seen that the proposed LDO exhibits very good phase margin even at 0.1mA load current. Fig. 8 reveals that a reasonably fair phase margin (46^o) is maintained at no load currents as well. The LDO also demonstrates excellent robustness against different temperatures as illustrated in Fig. 9, which is obtained through ac response by varying temperatures from -55^oC to 125^oC. It is found that the variation in the phase margin is negligible. It exhibits pretty good phase margin of 89^o for all the temperatures in the range specified.

Transient response is demonstrated through Fig. 10. A sudden load transient of 0 to 50 mA is applied at the load with a rise and fall time of 1μsec. It can be observed that the peak over shoot is nearly 600mV and peak under shoot is 950mV.The line regulation is obtained by varying the supply voltage from 1.4V to 1.8V and the result is plotted as shown in Fig. 11. It is found to be 0.259%. The load regulations is obtained by varying load current from 0.1mA to 50 mA and corresponding result is shown in Fig. 12. It is found that the line regulation is 43.44ppm/mA. All these results are tabulated in Table I and Table II. The ac response is obtained by exciting the circuit with a small perturbation in the loop and varying the frequency of the same.

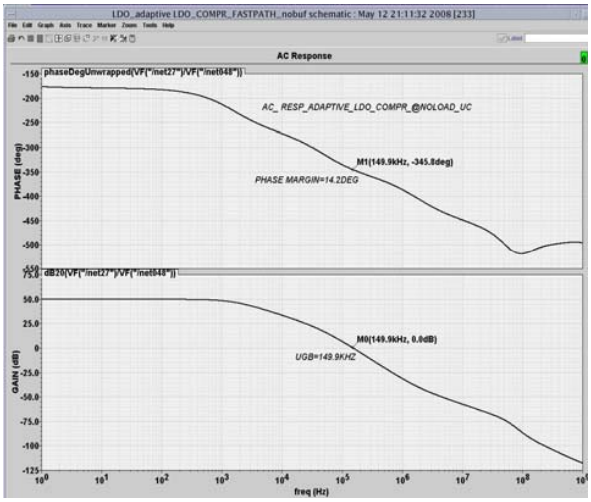

Fig. 3 Uncompensated LDO ac response at no load

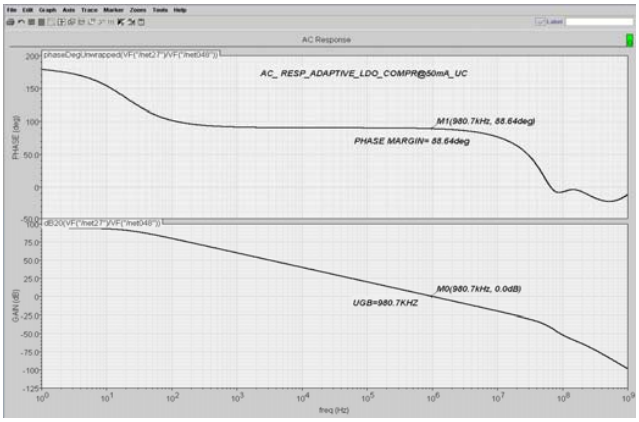

Fig. 4 Uncompensated LDO ac response at full load (50mA)

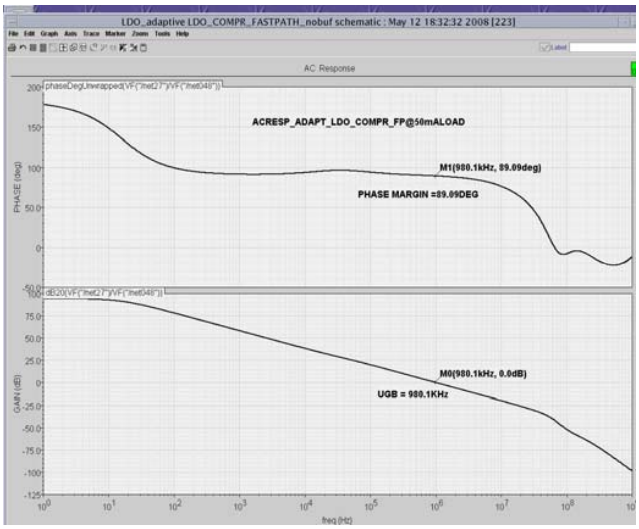

Fig. 5 Compensated LDO ac response at full load (50mA)

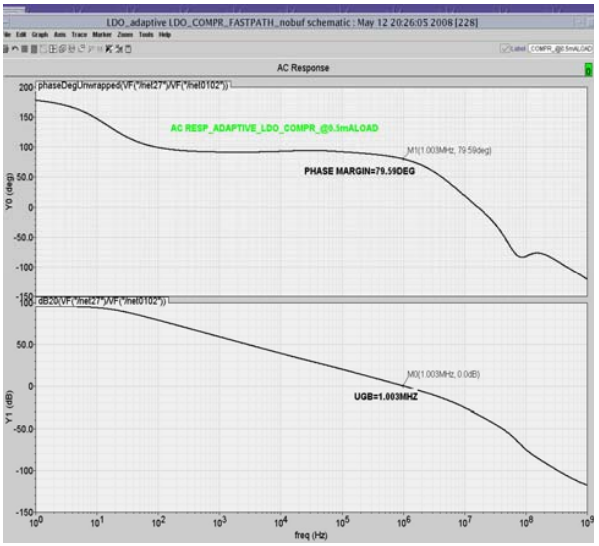

Fig. 6 Compensated LDO ac response at 0.5mA load current

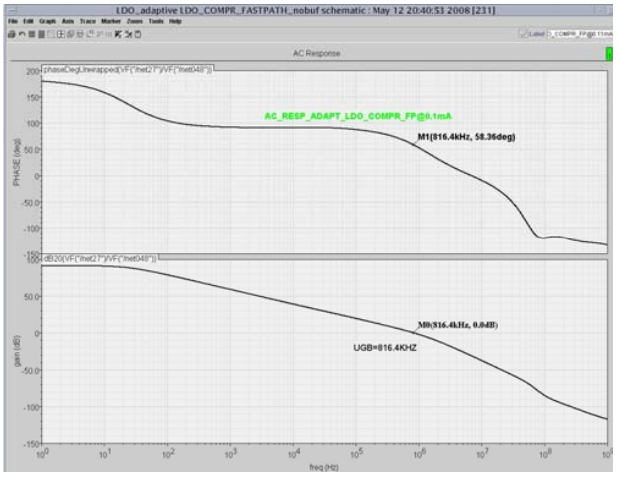

Fig. 7 Compensated LDO ac response at 0.1mA load current

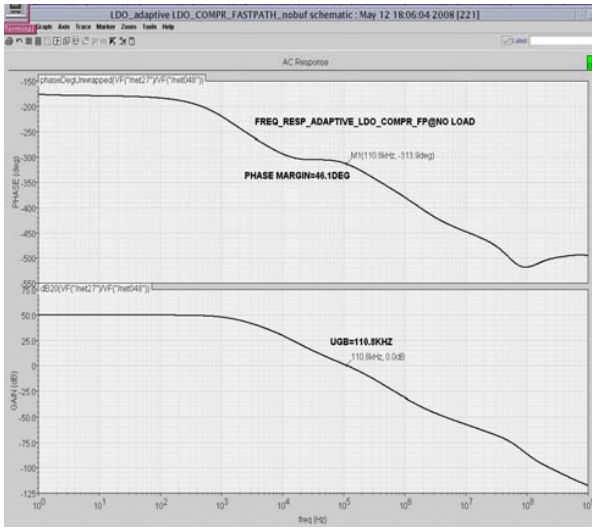

Fig. 8 Compensated LDO ac response at NO load current

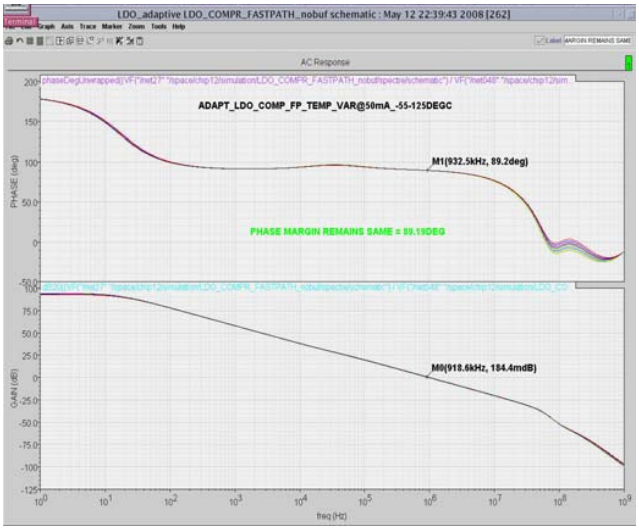

Fig. 9 Compensated LDO ac response at different temperatures (-55 to 125°)

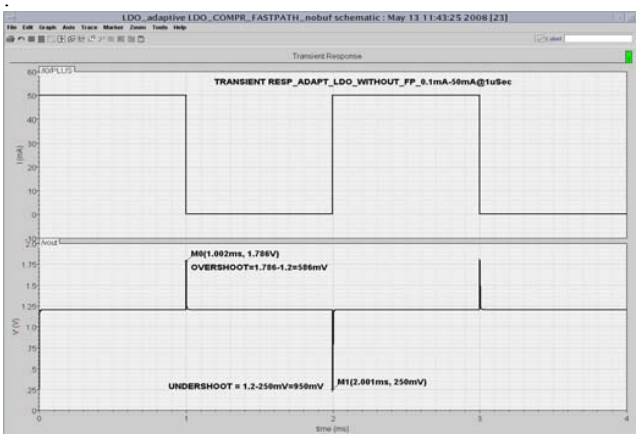

Fig 10 Transient response at 0.1-50mAload @1μ Sec rise and fall time

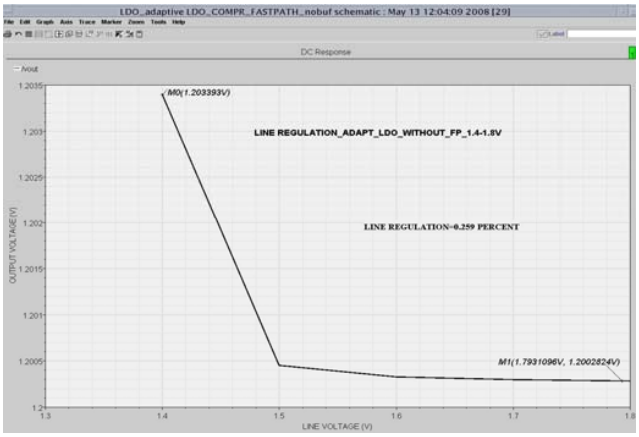

Fig. 11 Line regulation of the proposed LDO

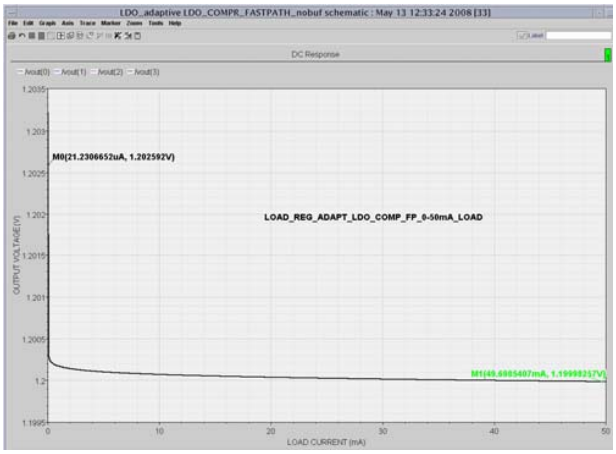

Fig. 12 Load regulation of the proposed LDO with load current varying from 0-50mA

TABLE I
RELATIVE COMPARISON OF AC RESPONSE OF THE PROPOSED LDO WITH AND WITHOUT COMPENSATION

Load current	50mA	1mA	0.5mA	0.1mA	0mA
Phase margin (deg)	88.64	83.5	78.9	54.57	12
Phase margin (deg)	89.09	83.9	79.5	58.27	47

TABLE II
TRANSIENT RESPONSE OF THE PROPOSED LDO AT 0.1MA-50MA LOAD TRANSIENT

Load current	Overshoot (mV)	Undershoot(mV)
0.1mA-50mA@1μSec	586	950

IV. CONCLUSION

An LDO voltage regulator is designed with a novel compensation scheme that adapts itself to the load changes. This LDO is designed using 180nm UMC technology. The proposed LDO facilitates one to improve the transient performance if necessary, independent of the compensation scheme. This particular architecture is designed to cater the digital base band section of the mobile phone. The proposed architecture exhibits very good stability. This can be seen from the Table I that the phase margin is nearly 80° at .5mA. The potential instability problem at lighter loads is circumvented and it is improved from 12 degrees to nearly 50 degrees without any complicated circuitry and hence power dissipation is minimized. The results also reveal that the LDO is pretty robust against different temperatures as well. Complete layout of the proposed regulator is shown in Fig. 13. Twin well process model is employed for the design. It is found that there are some layout hiccups with NMOS transistors in this process as it does not allow making substrate connection. Hence triple well technology transistors are used for NMOS where ever body bias effects are to be taken into account. It can be observed that most of the space is occupied

by the internal capacitor, compensation capacitor and the pass transistor.

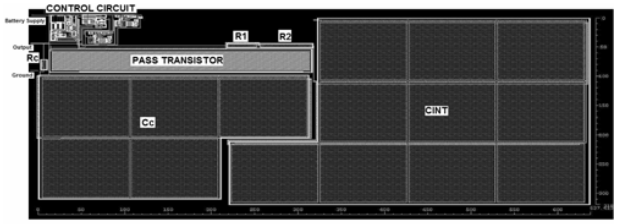

Fig. 13 Layout for the proposed LDO voltage regulator

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