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SCR-Based Advanced ESD Protection Device for Low Voltage Application

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***Abstract*—**This paper proposed a silicon controller rectifier (SCR) based ESD protection device to protect low voltage ESD for integrated circuit. The proposed ESD protection device has low trigger voltage and high holding voltage compared with conventional SCR-based ESD protection devices. The proposed ESD protection circuit is verified and compared by TCAD simulation. This paper verified effective low voltage ESD characteristics with low trigger voltage of 5.79V and high holding voltage of 3.5V through optimization depending on design variables (D1, D2, D3 and D4).

***Keywords*—**ESD, SCR, Holding voltage, Latch-up.

I. Introduction

AS processing technologies are more and more advancing, electrostatic discharge is becoming critical issue related to the reliability of integrated circuit. Although the advancement of processes resulted in miniaturization and enhanced performance, malfunctioning and breakdown due to electrostatic discharge at normal conditions are becoming critical issues [1]. Therefore, as the number of low voltage applications is increasing, it is required to develop ESD protection devices which have high robustness characteristics and latch-up immunity. Silicon Controlled Rectifier (SCR) has high current driving capability and high fault tolerance compared with area. It has superior characteristics compared with conventional ESD protection devices [Diode, metal oxide semiconductor (MOS), bipolar junction transistor (BJT)] [2], [3]. However, a general SCR structure has high trigger voltage more than approximately 20V due to avalanche breakdown voltage between N-well and P-well. In addition, turn-on voltage for NPN/PNP bipolar transistor which parasitically exists within SCR has approximately 2V lowered holding voltage [4]. Because of this problem, in the event that SCR is used as ESD protection device for low voltage integrated circuit, two problems such as high trigger voltage and low holding voltage should be solved. First, because high trigger voltage results in internal circuit breakdown (In general gate oxide), it is difficult to be applied for integrated circuit which uses low supply voltage. Second, if latch-up occurs from overshoot voltage and noise due to low holding voltage, internal circuit stops and high current is discharged through an ESD protection device. This causes thermal runaway, which in turn may cause the breakdown of an integrated circuit device. Therefore, effective ESD protection devices with low trigger voltage and high holding voltage are required [5].

This paper proposed a new SCR-based ESD protection device for low voltage application which has low trigger voltage and high holding voltage compared with conventional SCR. The proposed ESD protection device is verified and compared by TCAD simulation.

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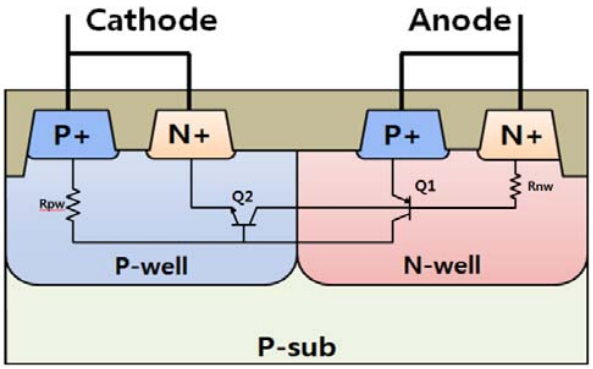

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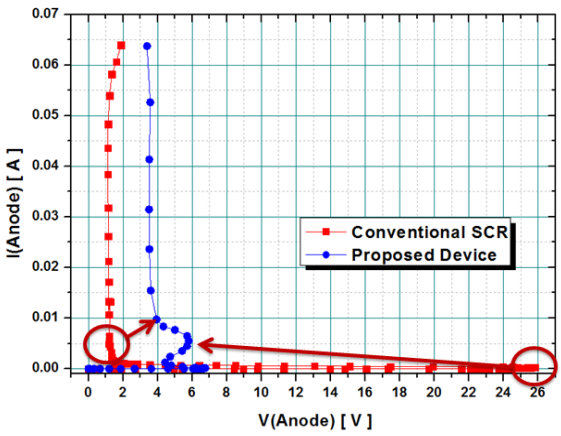


(b)

Fig. 1 Cross section view and simulation result for the conventional SCR

II. SCR-Based ESD Protection Device

A cross section view for the conventional SCR is shown in Fig. 1 (a). When ESD surge is applied to anode, junction between N-well and P-well is reverse biased until it goes into avalanche breakdown. The generated current can turn on parasitic NPN transistor. Its current makes voltage drop across

the Rnw and turns on PNP transistor as well. These two transistors discharge ESD current operating in positive feedback [6]. But this positive feedback results in low holding voltage about 1.5V. And trigger voltage is approximately 26V due to avalanche breakdown occurred at junction between N-well and P-well. So this conventional SCR is not appropriate for low voltage application as it doesn't meet ESD design window. Fig. 1 (b) shows simulation result of conventional SCR using TCAD simulation with ESD design window for low voltage application. Consequently, there is a need to narrow the gap between holding voltage and trigger voltage by increasing holding voltage and decreasing trigger voltage.

A cross section view for the proposed SCR-based ESD protection device is shown in Fig. 2. Characteristics for the proposed SCR-based ESD protection device are the followings. First, ggNMOS is a structure to reduce trigger voltage for conventional SCR structure. It provides trigger current in a way that adds bridge P+ diffusion area to SCR structure. Because of this, it reduces avalanche breakdown voltage in N-well of SCR and acquires low trigger voltage. Second, it raises holding voltage by reducing current gain widening base for NPN/PNP bipolar adding floating n+ diffusion area to n-Well area of SCR structure and floating p+ diffusion area to p-Well

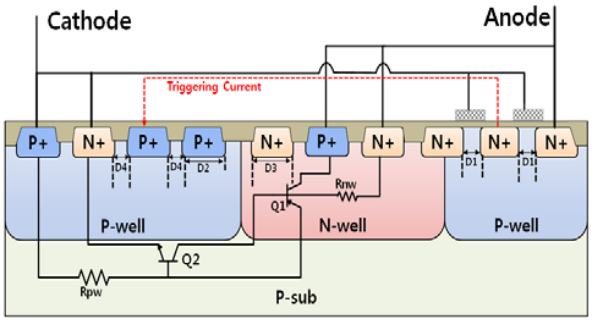


Fig. 2 Cross section view for the proposed SCR-based ESD protection device

Mechanism for the proposed device is the following: voltage at anode increases due to ESD current which inflows from anode terminal. Electric potential for N+ diffusion area and P-Well of ggNMOS increases, and electric potential of N-Well in SCR is also increasing. Electron-Hole Pair is created by avalanche breakdown because of drain at ggNMOS and high electrical field of P-Well. Therefore, a path for parasitic NPN of ggNMOS is created. In this case, the 1st trigger voltage and holding voltage for the proposed device is created. Hole current created after avalanche breakdown raises electric potential of P-Well. And electric potential of P-Well is raised higher than that of N+ source diffusion area of ggNMOS. The created hole current is discharged into diffusion area of P+ tap through N+ source diffusion area of ggNMOS. Because of this, hole current inflowing to SCR is more and more decreasing in electric potential between P-Well and N-Well.

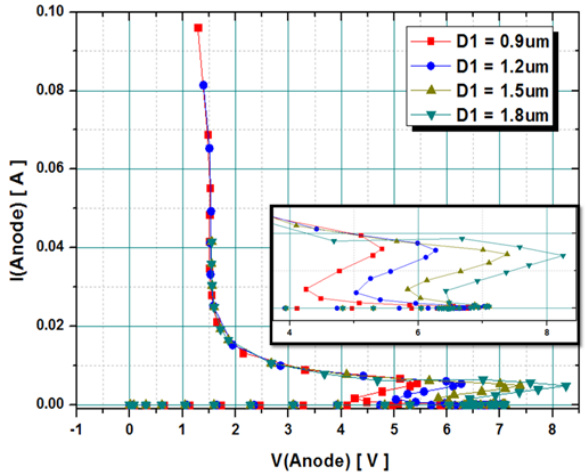
When electric field of N-Well and P-well in SCR that is reversed junction reach at threshold, avalanche breakdown occurs. Electron-Hole Pair is created by avalanche breakdown. The current of created holes moves to P-Well area, and electric potential for P-Well exceeds internal electric field for P-Well/N+ cathode junction, and then junction becomes forward bias. And parasitic NPN bipolar (Q2) is turned on. When parasitic NPN bipolar (Q2) is turned on, the current of parasitic NPN bipolar (Q2) causes voltage drop at Rnw, and PNP bipolar (Q1) is also turned on. If parasitic NPN/PNP are all turned on, the 2nd trigger voltage and holding voltage for this device is created. The current of PNP bipolar (Q1) causes voltage drop at Rpw, and this helps NPN bipolar (Q2) to be turned on. Here, the current of PNP bipolar (Q1) discharges ESD current by latch-up that doesn't have to provide bias to NPN bipolar (Q2) anymore. In addition, Electron-Hole Pair after avalanche breakdown flows through diffusion areas for floating N+ and P+. As the base width of NPN/PNP bipolar is increasing, current gain is lowered due to increase of recombination rate at base.

In order to analyze characteristics of trigger voltage and holding voltage for the proposed device, this paper has set design variables, D1, D2, D3 and D4. A design variable D1 is the length of gate ggNMOS located at the right side, and it is related to trigger voltage. Design variables, D2 and D3 is lengths for diffusion areas of floating P+ and floating N+ respectively, and they are related to holding voltage. Lastly, a design variable D4 is a distance between diffusion areas of N+ cathode and P+ tab, and it is related to holding voltage.

III. Simulation Results

Fig. 1 (b) shows a graph representing the conventional SCR-based ESD protection circuit through a MOS-triggered SCR-based ESD protection circuit and the TCAD simulation of the electrical characteristic. For this simulation, the structure was designed with TSUPREM4 of SYNOPSYS, and electrical characteristics were analyzed with MEDICI.

Fig. 3 shows TCAD simulation characteristic curve for each design variable of the proposed device. Fig. 3 (a) indicates a graph when a design variable D1 is changing from 0.9um to 1.8um. A design variable D1 indicates change in the gate length of ggNMOS located in the right side. Although fluctuation in holding voltage is not so much high as the length of gate increases, trigger voltage increases. And, as the gate length of ggNMOS is increasing, current gain of parasitic NPN bipolar is reduced and therefore, holding voltage is increasing. Because of this, the 2nd trigger voltage becomes identical to holding voltage of ggNMOS. As a result of this holding voltage increase, the 2nd trigger voltage increases. Fig. 3 (b) is a graph when design variables, D2 and D3 are changed from 1.5 um to 7.5um. As a design variable D2 is increasing in its length, the base width of parasitic NPN bipolar is increasing.



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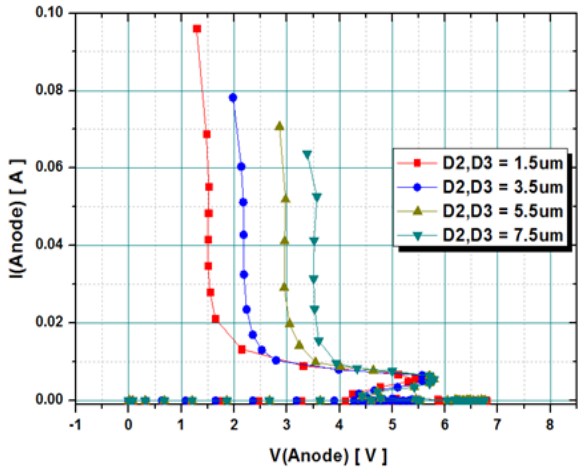

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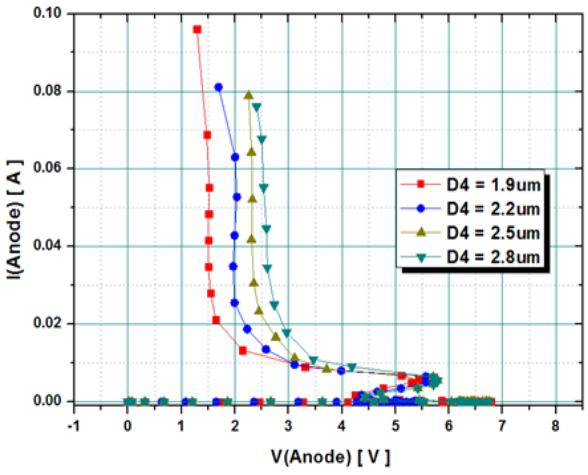

(c)

Fig. 3 TCAD simulation I-V curves in variations in D1 (a), D2 and D3 (b) and D4 (c) for the proposed device protection device

As a design variable D3's length is increasing, the base width of parasitic PNP bipolar is increasing. Therefore, current gain for parasitic NPN/PNP bipolar is reduced, which in turn holding voltage increases by approximately 2V from 1.51V to 3.5V. Fig. 3 (c) is a graph when a design variable D4 has change of 0.3um in its length from 1.9um to 2.8um. A design variable D4 is a distance between N+ cathode and P+ tab. As the length of D4 is increasing, the effective base width of parasitic NPN bipolar (Q2) is extending. In other words, as D4 increases, the current gain for parasitic NPN bipolar (Q2) is decreasing and the holding voltage of SCR is increasing. It increased by approximately 1.1V from 1.5V to 2.6V. But on-resistance is increased because of additional resistance in discharge path by D2, D3 and D4 variables. The measurement results for trigger voltage, holding voltage and 2nd breakdown current depending on each design variable are shown in Table I.

TABLE I
ELECTRICAL CHARACTERISTICS FOR EACH DESIGN VARIABLES FOR THE PROPOSED ESD PROTECTION DEVICE

Design parameter		Trigger Voltage	Holding Voltage
D1	0.9um	5.42	1.52
	1.2um	6.26	1.54
	1.5um	7.38	1.55
	1.8um	8.25	1.56
D2,D3	1.5um	5.4	1.51
	3.5um	5.6	2.2
	5.5um	5.7	2.9
	7.5um	5.79	3.5
D4	1.9um	5.4	1.5
	2.2um	5.6	1.9
	2.5um	5.7	2.3
	2.8um	5.72	2.6

IV. CONCLUSION

This paper proposed SCR-based ESD protection device with reduced high trigger voltage based on structural change that has been a problem found at conventional SCR. Also, this paper improved latch-up problem by increasing low holding voltage. Electrical charactersitics is analyzed through TCAD simulation. Trigger voltage for the proposed device has been increased from 5.42V to maximum 8.25V as a design variable D1 increases. Holding voltage is raised from 1.51V to 3.5V as design variables D2, D3 is increasing and also raised from 1.51V to 2.6V as a design variable D4 is increasing. Through design variations, they are effectively optimized for low voltage application that lower trigger voltage of 5.79V and higher holding voltage of 3.5V compared with conventional SCR that has trigger voltage of 26V and holding voltage of 1.5V.

In conclusion, the proposed device has low trigger voltage and high holding voltage. It is expected that proposed SCR-based ESD protection device can improve the reliability of integrated circuit for low voltage application.

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