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Realization of Fractional-Order Capacitors with Field-Effect Transistors

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***Abstract*—**A novel and efficient approach to realize fractional-order capacitors is investigated in this paper. Meanwhile, a new approach which is more efficient for semiconductor implementation of fractional-order capacitors is proposed. The feasibility of the approach has been verified with the preliminary measured results.

***Keywords*—**Fractional-order, field-effect transistors**,** RC transmission lines.

I. Introduction

IN recent years, many applications of fractional-order capacitors have been proposed [1]-[5]. On the electrical side, the behaviors of traditional capacitors and inductors are governed by the first-order differential equations. Hence, any system constructed with such n^{th}-order elements is described by an n^{th}-order system of differential equations. With Laplace transform, it also generates n^{th}-order terms to represent the equation. The applications of fractional-order operations such as fractional derivatives and integrals (FDIs) have motivated the theory of chaos and their corresponding research on viscoelasticity / damping [6]-[10], and chaos / fractals [11]-[14] as well as the state-of-the-art areas such as biology [15], electronics [16], control [17]-[19], and signal processing [20]-[21].

Four decades ago, the feasibility of realizing a fractional-order capacitor has been investigated [22]-[23]. A finite element approximation of the special case $Z = 1/C(j\omega)^{1/2}$, was reported in [24]. This finite element approximation relies on the possibility of emulating a fractional-order capacitor via semi-infinite self-similar RC trees. The technique was later developed further [25]-[27] in order to approximate any $Z = 1/C(j\omega)^{\pm\alpha}$, in which α is arbitrary and the device with such an impedance was termed "fractance device".

Although these fractional-order element realization approaches were developed, all of them are based on an approximation method, which implies that a certain amount of discrete components are required to implement the fractional-order impedance device. Until more recently, the implementation of two-terminal fractional device was reported in [28]-[29]. In which the implemented probe was based on a metal-insulator liquid interface and was employed in [29] to realize a fractional-order differentiator circuit. The approach may develop the real fractional element whereas it is difficult to implement with integrated circuits. In this paper, we therefore renew the development of discovery of the fractional-order capacitor and take advantage of the nonlinear characteristics of FETs to simulate the RC transition lines as the fractional-order capacitors [30].

To the best of our knowledge, this is the first time that FETs are announced to be employed as the fractional-order elements. Moreover, in this paper we will investigate the large-signal frequency response and also we will propose a new approach to implement fractional-order capacitors.

II. RC Transmission Line with FETs

The conducting channel of a FET operating at triode region can be modeled as a nonlinear RC transmission line as shown in Fig.1[30], in which the resistance and capacitance per unit of line length, $R(v)$ and $C(v)$ are functions of the voltage v. The instantaneous values of voltage and current are given by

$$i_{x,t} = -\frac{1}{R(v_{x,t})}\frac{\partial v_{x,t}}{\partial x} \tag{1}$$

and

$$\frac{\partial i_{x,t}}{\partial x} = -\frac{\partial}{\partial t}\int_0^{v_{x,t}} C(v_{x,t})dv_{x,t} \tag{2}$$

For an insulated gate FET, the resistance $R(v)$ and capacitance $C(v)$ can be derived as follows,

$$R(v) = \frac{L}{\mu C_t (v - V_0)} \tag{3}$$

$$C(v) = \frac{C_t}{L} \tag{4}$$

Note that L is the length of the channel, μ is the mobility of carriers in the channel, C_t is the total gate-channel capacitance, and V_0 is the threshold voltage (pinch-off).

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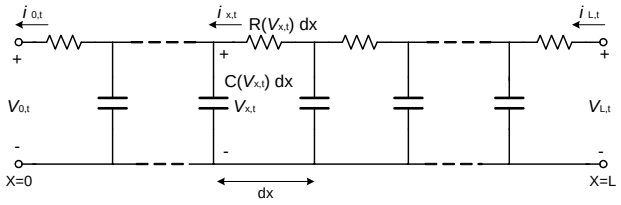
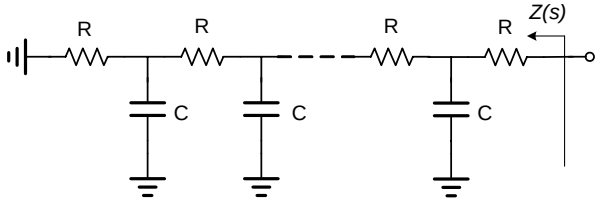
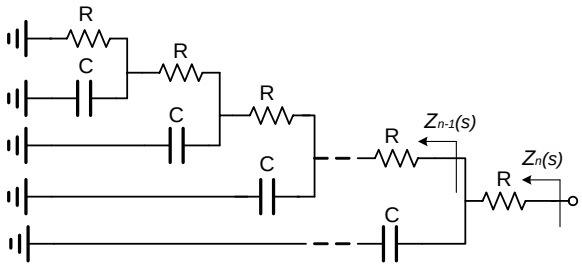


Fig. 1 Lumped equivalent circuit of a nonlinear RC line

Large-signal transient response analysis presented in [30] demonstrated the same steady-state behavior as that of the RC line itself, which the series distributed resistance was modeled with n lumped resistors and the shunt distributed capacitance was also modeled with n-1 limped capacitors. As a result, by the employment of a large number of resistors and capacitors for the lumped equivalent circuit and letting the node x=0 grounded, we can obtain the impedance Z(s) at node x=L as shown in Fig. 2(a). Also by rearranging the circuit, a recursive circuit structure can be obtained as shown in Fig. 2(b).



(a)



(b)

Fig. 2 Lumped equivalent circuit of a FET with one terminal grounded

Notice that for a large number of R and C, the impedance $Z_n(s)$ is approximately equal to $Z_{n-1}(s)$. Therefore, for $Z_n(s) = Z_{n-1}(s) = Z(s)$, we can obtain

$$\left(Z(s)\,//\,\frac{1}{sC}\right)+R=Z(s) \tag{5}$$

By letting $\frac{4}{sRC}>>1$ yields

$$\begin{aligned} Z(s) &= \frac{1}{2}\left(R+2\sqrt{\frac{R}{C}}\cdot\frac{1}{s^{1/2}}\right) \\ &= \frac{1}{2}\left[R+2\sqrt{\frac{R}{C}}\omega^{-1/2}\exp\left(-j\pi/4\right)\right] \end{aligned} \tag{6}$$

where $s = j\omega$. Obviously, by dividing the nonlinear RC transmission line into an infinite number of sections, we can obtain a fractional-order capacitance as indicated in Equation (6).

A preliminary Hspice simulation has been performed with a single FET M1 operating at triode region. The configuration shown in Fig. 3 is employed to investigate the fractional-order grounded capacitor. We also let the drain as port 1 and the grounded-source as port 2 with the biased voltage at the gate.

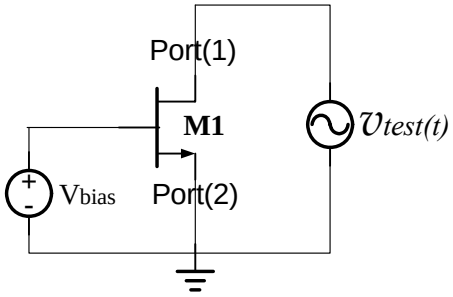


Fig. 3 Configuration of a FET operating at triode region acts as a fractional-order grounded capacitor

Fig. 4(a) and (b) show the simulated results with the biased voltages V_{GS}=1V and 2V, respectively. Obviously, from the S_{11} plots the resistance and capacitive reactance of the impedance Z(s) decrease with an increase of frequency, which can be explained with Equation (6).

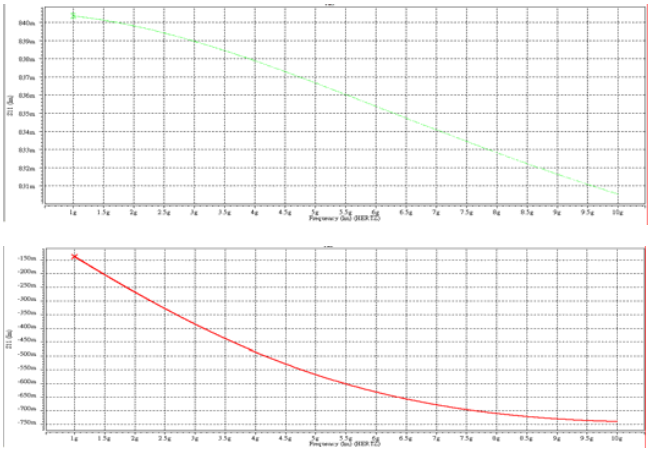
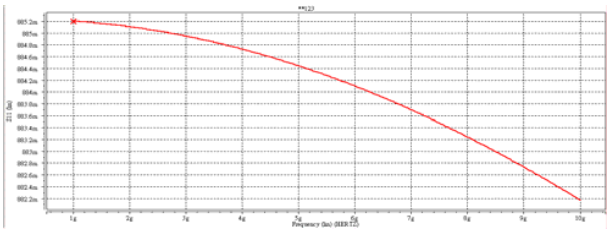


Fig. 4 (a) S_{11} plots of magnitude (upper plot) and phase (lower plot) for V_{GS}= 1V



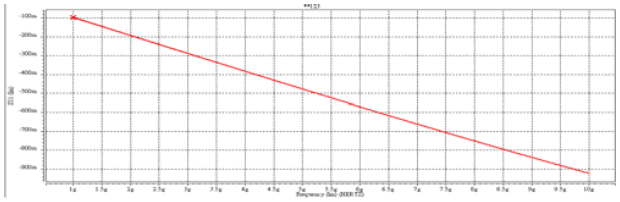


Fig. 4 (b) S_{11} plots of magnitude (upper plot) and phase (lower plot) for V_{GS}= 2V

III. Implementation of Fractional-Order Capacitors with Field-Effect Transistors

To gain more insight, from Equation (6) the resistance and capacitive reactance of the impedance Z(s) decrease with an increase of frequency. Fig. 5 shows the measured S_{11} for the device of enhancement-mode pHEMT FET, which the frequency range of the plot in a 50-Ω system is from 1.9GHz to 4.5GHz for the biased voltage of V_{GS}=0.8V with the same configuration shown in Fig. 3. For the gate-to-source biased voltage, the resistance and capacitive reactance of the impedance Z(s) decrease with an increase of frequency. Due to packaging inductive effect, the reactance becomes positive for the operating frequency over 4.5GHz.

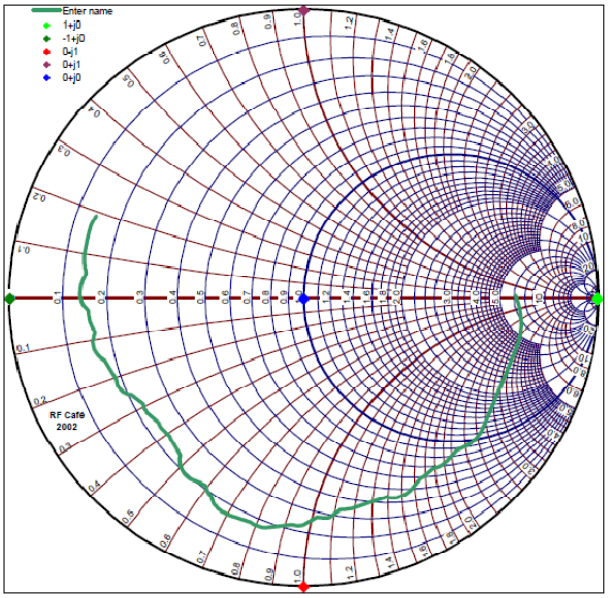


Fig. 5 S_{11} plot with signal frequencies from 1.9GHz to 4.5GHz for gate-to-source voltage V_{GS}=0.8V

Moreover, the resistance R and capacitance C can be investigated with the parasitic resistance of the conductive channel and the gate-to-channel capacitance for different V_{GS}. For a higher V_{GS}, due to the higher biased voltage, the channel resistance will be lower. Fig.6 (a) and (b) show the resistance and reactance of the measured impedances for three different biased voltages, respectively. Due to the additional packaging parasitic reactance, the imaginary-part is a bit higher than real-part of the measured results whereas the resistance Re(Z(s)) and capacitance Im(Z(s)) of the fractional-order impedance decrease with an increase of frequency. Moreover, for a higher biased voltage V_{GS} the channel resistance will be lower and in turn, from Equation (6) the impedance will be lower.

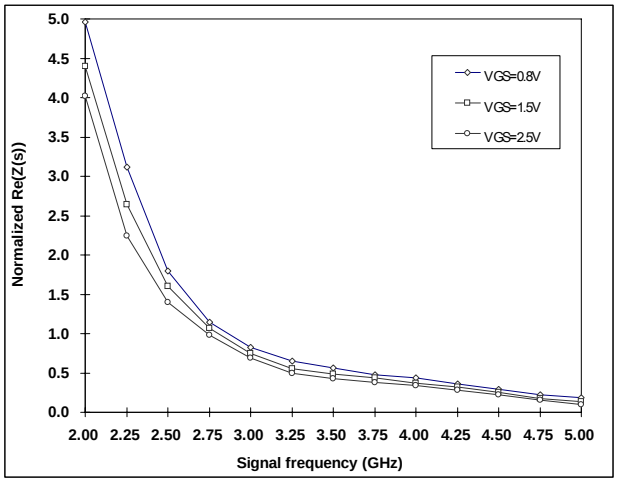


Fig. 6 (a) Normalized real-part of fractional-order impedance versus frequency for different gate-to-source biased voltages

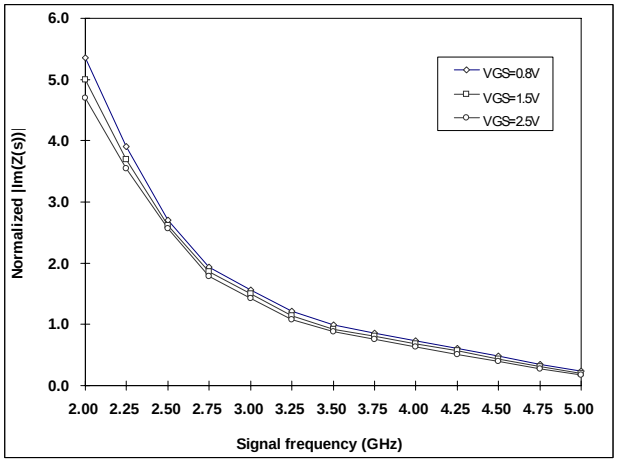


Fig. 6 (b) Normalized absolute value of imaginary-part of fractional-order impedance versus frequency for different gate-to-source biased voltages

IV. Conclusion

This paper has explored the feasibility of monolithic realization of fractional-order capacitors. We obtain a good agreement between the mathematics derivation and measured results. Obviously, the advantage of this approach is the possibility to realize the fractional-order devices and some high-performance systems with integrated circuits.

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