Pulse Generator with Constant Pulse Width

Hanif Che Lah, Wee Leong Son, Rozita Borhan

Abstract—This paper is about method to produce a stable and accurate constant output pulse width regardless of the amplitude, period and pulse width variation of the input signal source. The pulse generated is usually being used in numerous applications as the reference input source to other circuits in the system. Therefore, it is crucial to produce a clean and constant pulse width to make sure the system is working accurately as expected.

Keywords—Amplitude, Constant Pulse Width, Frequency Divider, Pulse Generator.

I. INTRODUCTION

OUTPUT pulses produced by a conventional pulse generator are often very much dependent on the input signal source width. Noise and imperfection of the input signal also contribute to the variation of the input signals. These are important elements which affect the result produced by the conventional pulse generator. To make the matter worse, the generated non-constant width pulse is generally used as a reference input source to other circuits in measurement. Thus, it is very important to have a constant output pulse width in order to make sure that the performance of the circuits or any system for that matter are not being jeopardized by the inconsistencies of the generated pulse.
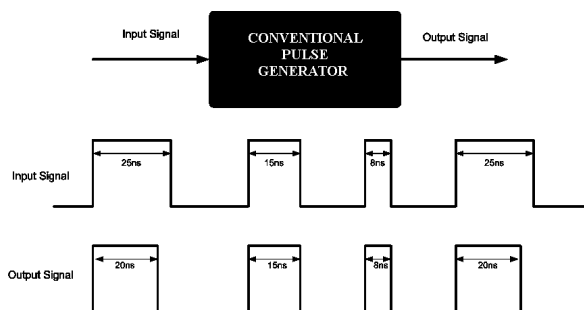

Fig. 1 Conventional Pulse Generator and its waveforms

Fig. 1 shows a conventional pulse generator with its waveform. The output signals produced have different width pulses.

This paper will discuss a method of producing a pulse generator that generates a constant output pulse width as shown in Fig. 2; regardless whether the input signal is very noisy, digital or analog form or even having different amplitudes or period as an input pulse width. Fig. 2 also shows a signal waveform coming in which is very noisy and varied in

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pulse width, but the output coming out is a consistent pulse width throughout which is 20ns. Such circuit has been developed in house, generating a constant pulse width output as desired.
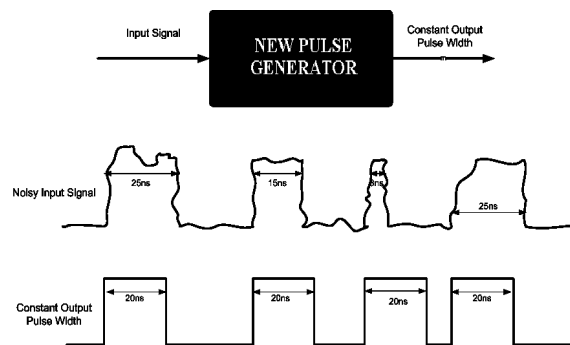

Fig. 2 New invention of the pulse generator with its waveforms

II. THE IMPLEMENTATION

The implementation in general, is about a pulse generator circuit, more particularly, to a pulse generator that produces output pulses of constant pulse width regardless of the variation of the input to the pulse generator.

Most methods only received digital signal as their input source. They also used some latches or post charged unit in operation of the pulse generator which is different with method that we are discussing here [1]-[6].

The proposed circuit comprises of a signal detector, frequency divider, integrator circuit and a pair of single-short with time-delay circuits. The function of the signal detector is to generate a clean signal from an alternating input signal source that include noisy signal either an analog or digital input signals. The frequency divider consists of a D-type flip flop where the function is to provide a frequency division of two for the input signals and to avoid the overlapping of the output pulse signals generated by the pulse generator. The single-shot with time-delay circuits are used to detect a rising edge of an incoming signal regardless of pulse amplitude and pulse width variation. The single-shot circuits output a single-short pulse while time-delay circuits fixed/adjust the single-short pulse width. Integration of the output pulses from both of the single-shot with time-delay circuit will produce a train of constant pulse width signal.

This implementation also relates to a pulse generator circuit where the main purpose is specifically to generate and produce a constant 20 ns output pulse width. In a control system it is quite often desired to generate a constant pulse width in response to an applied alternating input signal. A pulse generator adopting the frequency divider technique can avoid the overlapping of the outputs. Fig. 3 shows the block diagram

of the pulse generator circuit. It comprises of four main components which are the signal detector, frequency divider circuit, a pair of one-shot with time-delay circuit and integrator circuit.
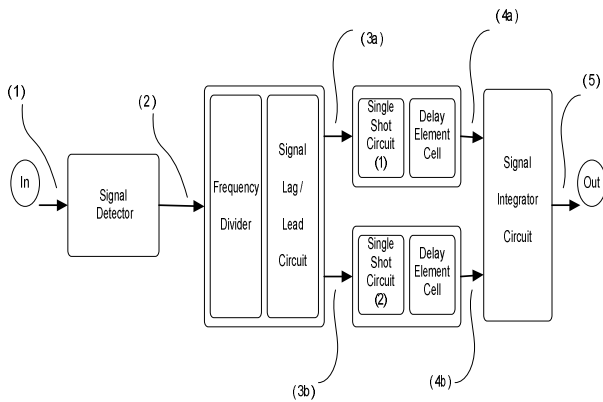

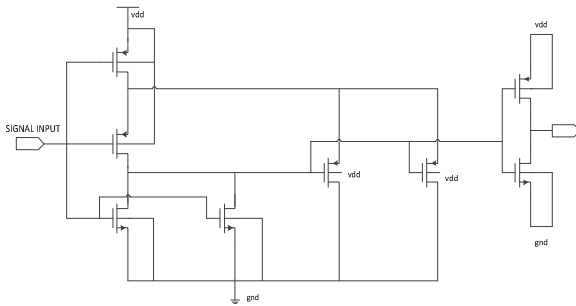Fig. 3 The Pulse Generator Block Diagram

A. Signal Detector Circuit

Fig. 4 Signal Detector Schematic Diagram

Fig. 4 shows the schematic diagram of the Signal Detector Circuit.This circuit is useful in generating a clean output signal from noisy and variable incoming input signal.
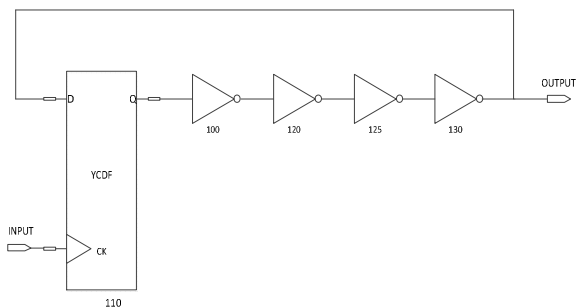
B. Frequency Divider Unit

Fig. 5 Frequency Divider Schematic Diagram

Fig. 5 shows a block diagram of a frequency divider unit that divides an input frequency by two. The input signal is applied to the clock input of the D-type flip flop which transitions the logical state of the Q output to be equal to the logical state of the D input when the input signal transition from low to high. Inverterisapplied to the D input a signal that is opposite in logical state to the Q output, so that the Q output change logical state in response to the rising edge at the input signal. This results in an output signal with a frequency one half of the input signal frequency. The frequency divider produces two output signals which are out1 and out2. Inverters are applied to invert the signal from out1. The frequency divider technique is used to refrain the overlapping of the output signals.
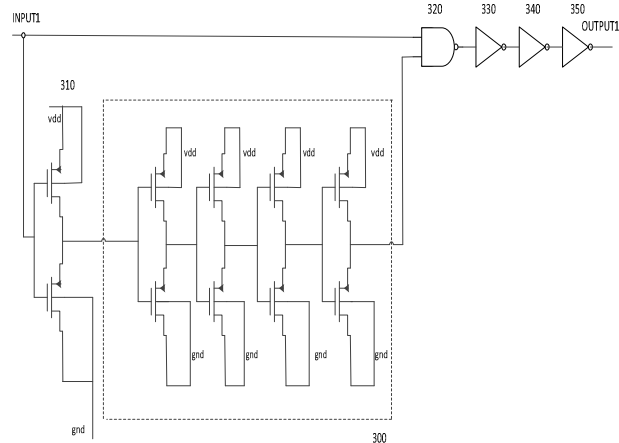
C. Single-Shot With Time-Delay Circuit

Fig. 6 One Shot Circuit Schematic Diagram with Timing Delay

The circuit diagram in Fig.6 shows the one-shot with delay circuit. This circuit produces a positive logic edge-trigger pulse width. It consists of a time-delay circuit, a NAND gate and inverters.The one-short with time-delay circuit has an inverter to generate an inverted input signal **INPUT1**. A time-delay circuit is for delaying the inverted input signal for a predetermined time. The NAND gate receive the input signal **INPUT1** and the output of the time-delay circuit to generate pulse signal **OUTPUT1**.The output pulse signal has a pulse width corresponding to the predetermined value of time. Inverters are connected in series as buffers.
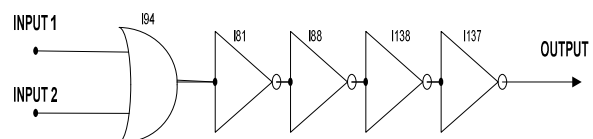
D. Integrator Circuit

Fig. 7 Integrator Schematic Diagram

Fig.7 also shows the integrator circuit which consists of an OR gate and four inverters which are connected in series. The first input to the OR gate comes from the output pulse of the first one-shot circuit **INPUT1**; while the second input of the OR gate comes from thesecond one-short circuit **INPUT2**. The output of this OR gate serves as the output of the pulse generator. Inverters are connected in series as circuit driver for the output pulse.

III. RESULT OF THE IMPLEMENTATION

Fig. 8 shows schematic diagram of the complete integration of the Pulse Generator Circuit. It shows all the components needed to implement the whole system.
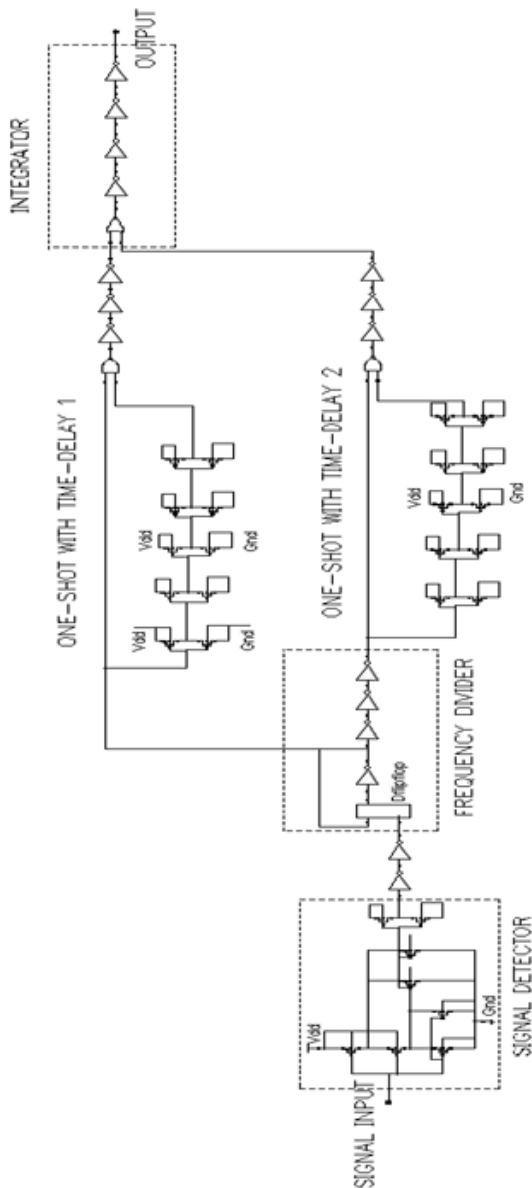

Fig. 8 Pulse Generator Schematic Diagram

Fig. 9 shows the waveform from the implementation. The input signal is being fed into a signal detector to generate a clean output sinusoidal pulse signal. Incoming input pulse signal are divided by a factor of 2 by the frequency divider.
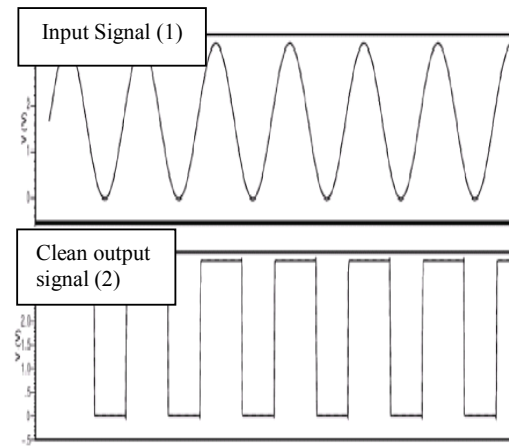

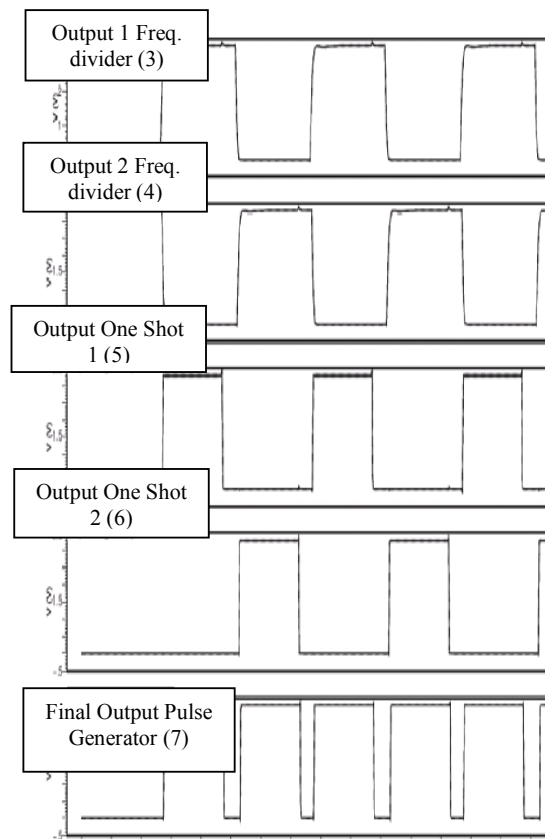Fig. 9 Input signal waveform and incoming pulse signal

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Fig. 10 Signal waveform being split and integrated

In Fig. 10, signals are split and phase shifting has been applied to form two signals, one is lagging and the one is leading. Both signals are non-overlapping. Single shot circuit will trigger pulse signal when rising edge is detected. This method will generate the pulse according to the time delay required. Fig. 10from the last waveform shows the output

signals are being integrated. The waveform produced is a clean and constant pulse width from the pulse generator.

IV. CONCLUSION

From the implementation and result, it is proven experimentally that a clean and constant output pulse width has successfully been produced. This circuit has also been fabricated in 0.35u CMOS Technology together with security system application and worked successfully as expected.

Fig. 11 shows the layout drawing of the Pulse Generator together with the whole system in a small circle. The left corner of the drawing is the zoom out version of the said drawing. This particular pulse generator will receive a noisy random photon signal and produce a constant pulse width which acts as an Initialization Vector (IV), which is bit-extracted for security communication application.The accuracy of the pulse signal produced will very much determine the performance of the said security system.
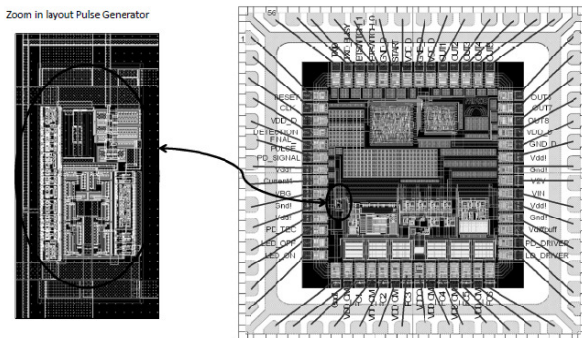

Fig. 11 Layout Drawing of the Tapeout Pulse Generator

At present, 20ns pulse width is produced. For future work, it would be interesting to produce a mixture of a constant pulse width, width are intentionally mixed to disguise between genuine bit or dummy bit particularly to strengthen the security communication system.

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