Program Memories Error Detection and Correction On-Board Earth Observation Satellites

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Abstract—Memory Errors Detection and Correction aim to secure the transaction of data between the central processing unit of a satellite onboard computer and its local memory. In this paper, the application of a double-bit error detection and correction method is described and implemented in Field Programmable Gate Array (FPGA) technology. The performance of the proposed EDAC method is measured and compared with two different EDAC devices, using the same FPGA technology. Statistical analysis of single-event upset (SEU) and multiple-bit upset (MBU) activity in commercial memories onboard the first Algerian microsatellite Alsat-1 is given.

Keywords—Error Detection and Correction; On-board computer; small satellite missions.

I. INTRODUCTION

EARTH observation missions using small satellites in LEO provide fast and cheap access to space [1]-[4]. To make a start-up in space technologies in Algeria, the National Center for Space Technology (CNTS) has initiated a small satellite project named Alsat-1. Alsat-1 is the first step in CNTS's plan to develop Algeria's national space infrastructure [2]. It is part of a wider international collaboration to launch the first disaster monitoring constellation of Earth observation satellites. The primary goal of the mission is to provide daily imaging worldwide for the monitoring and mitigation of natural and man-made disasters as well as dynamic Earth observation.

Alsat-1 was launched into a 686 km sun-synchronous orbit in November 2002. This microsatellite carries specially-designed Earth imaging cameras which provide 32-meters resolution imaging in 3 spectral bands (green, red, and near infrared) with an extremely wide imaging swath of 600 km on the ground that enables a revisit of the same area anywhere in the world at least every 4 days with just a single satellite. Images are stored in an 8-Gbit solid-state data recorder for high capacity onboard storage of image data and transmission to ground via an 8-Mbps S-band downlink.

The Alsat-1 main on-board computer (OBC) is an Intel 80C386EX based system that was designed, built and tested at Surrey Satellite Technology Limited (SSTL), a company owned by the University of Surrey in Guildford, UK. The OBC plays a dual role for Alsat-1, acting as the key component of the payload computer as well as the command and control computer for the microsatellite. It has also been adopted by several other satellite projects.

Fig. 1 shows the system block-diagram of the OBC. It is a general purpose computer for space applications. It features 4 MBytes of program memory which is protected by error detection and correction (EDAC) and 32 KBytes of firmware storage EPROM. The board also supports multiple data inputs and can store a maximum of 128 Mbytes of data. This memory is normally referred to as the ramdisk. Compared to the program memory there is no hardware protection on the ramdisk, instead a soft EDAC is used (Reed Solomon code).

In space applications it is well known that in Low Earth Orbit (LEO) stored digital data suffers from SEUs. These upsets are induced naturally by radiation. Bit-flips caused by SEUs are a well-known problem in memory chips and error detection and correction techniques have been an effective solution to this problem. For the secure transaction of data between the CPU of the on board computer and its local RAM, the program memory has generally been designed by applying the Hamming code or with Triple Modular Redundancy (TMR), which is a hardware implementation that includes replicated memory circuits and voting logic to detect and correct a faulty value.
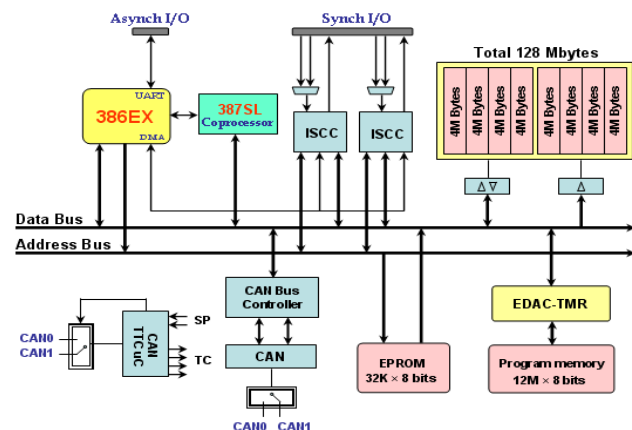

Fig. 1 Block diagram of the Alsat-1 primary OBC.

These error correction techniques are well-known and widely used. They allow single correction of one error bit per stored word. For computers on board a satellite, there is however a definite risk of two error bits occurring within one byte of stored data; either from the impact of a particularly

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energetic SEU, or from a second SEU creating a second error [3]-[5].

In a recent work, a real time low complexity codec has been described and implemented in FPGA technology for application in the Alsat-1 solid state data recorders [3].

This paper aims to present a new architecture of an on-board EDAC device for future Earth observation small satellite missions in low Earth orbits and its implementation in FPGA technology. The performance of the proposed EDAC device is measured and compared with two different EDAC devices, using the same FPGA technology. This paper also presents a statistical analysis of single-event upset (SEU) and multiple-bit upset (MBU) activity in commercial memories onboard Alsat-1. The in-orbit observations show that the typical SEU rate at Alsat-1's orbit is one error bit in one million bits per day, where 80% of these SEUs cause single-bit errors and the remaining SEUs result in double-bit and multiple-bit errors.

II. ERROR DETECTION AND CORRECTION

TMR based EDAC

Since Alsat-1 is placed in a Low Earth Orbit of 686 km, elevated levels of radiation caused by the lack of atmosphere increase the probability of SEUs. A single-event upset, or SEU, is a non-destructive error which usually affects logic cells in such a way that it can cause a bit in a memory device to change logic states. This phenomenon is caused by a false charge created by the transit of a single ionizing particle through a memory chip. There are various methods of error detection and correction, but one of the most commonly used is TMR.

A well-known technique for providing tolerance against single hardware component failures is triplication of the component, called triple modular redundancy (TMR). It is a widely used method of protecting a program memory from both hard and soft failures. The implementation involves using three identical program memories containing the same data. The output from each memory is then processed by a voter circuit, which outputs the majority of the three inputs. As long as two of the memories are functioning properly, the output will be valid.

The integrity of the program memory is important for proper operation of the OBC. A single-bit error in one memory location can cause the 80C386 to enter an endless loop or corrupt important scientific data. For the secure transaction of data between the CPU of the OBC and its local RAM, the memory is protected by a TMR-EDAC circuit. The EDAC is implemented in two Actel A1020B 2000 gates FPGA as shown in Fig. 2. Disadvantages of the TMR are the large memory overhead of three times the required memory and the large number of I/O pins required on the EDAC logic. The 4 Mbytes of memory requires an additional 8 Mbytes to implement the TMR. Each individual memory bank of the TMR can be accessed by the CPU. This allows the TMR to be tested and exercised while in orbit.
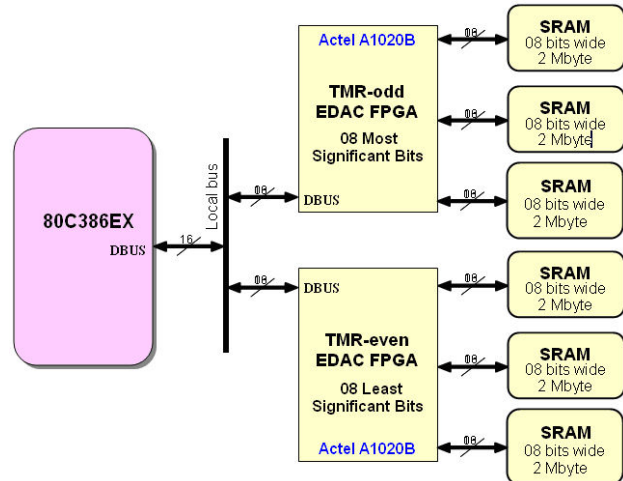

Fig. 2 Block diagram of the EDAC-TMR Device and its memory.

The individual banks can be accessed by changing two bits of the 386EX parallel port.

Recently, in-orbit observations of SEU in the SRAM memories of the OBC for the Alsat-1 in a LEO of 686 km have been presented in [6]. The memories are based on eight Samsung SYS 84000 parts of 4 M-byte each in size. In Fig. 3, the yearly average of the number of SEU/day is plotted for the period from January 2003 to December 2008. This figure shows the increase of the upset rates with the increasing time. In 2003 and 2008, the average SEU rate is 66 SEU/day and 110 SEU/day, respectively. Between November 2002 and December 2008 a total of 4940 byte errors were observed in the eight memory devices. Fig. 4 shows the number of double-bit and multiple-bit errors that has been occurred during the period from 2003 to 2008.

From these observations, the typical SEU rate at Alsat-1's orbit is one error bit in one million bits per day, where 80% of these SEUs cause single-bit errors and the remaining SEUs result in double-bit and multiple-bit errors.
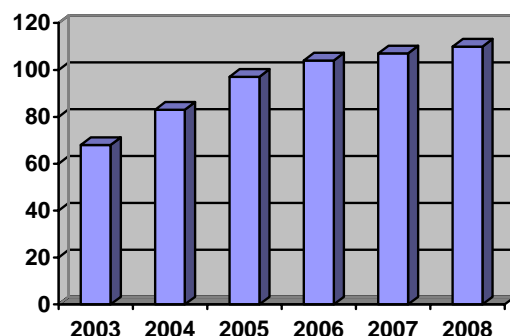

Fig. 3 Plot of the yearly average of the number of SEU/day versus time from 2003 to 2008.
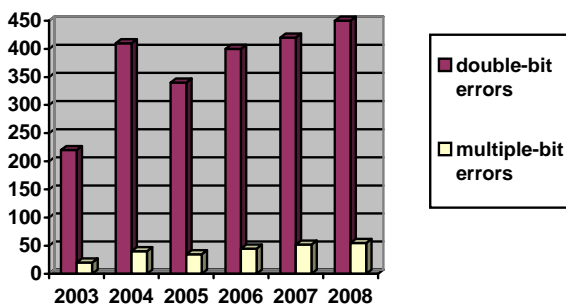
Fig. 4 Plot of the number of double-bit and multiple-bit errors versus time from 2003 to 2008.

Fig. 5 shows the location of upsets accumulated from 01/01/2003 to 01/12/2008 on the Alsat-1 spacecraft. More than 80% of the SEUs occur in the SAA and the others are induced by the Galactic Cosmic Rays in the high latitude regions.
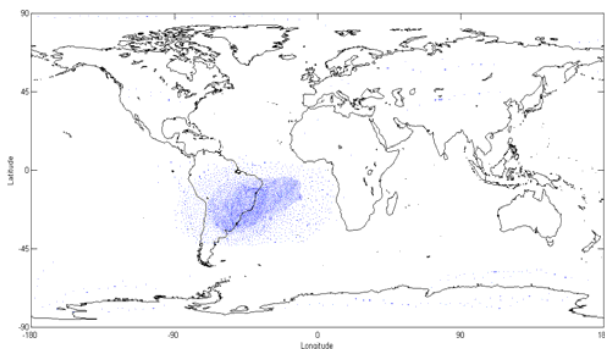

Fig. 5 Orbital position of the OBC386 Ramdisk memory upsets.

Quasi-Cyclic EDAC

One class of codes for which very low complexity encoding schemes have been demonstrated are Quasi-cyclic codes [7]-[8]. They are the most powerful available short block codes having the half-rate structure (n, n/2). A code is quasi-cyclic if for any cyclic shift of a codeword by c places, the resulting word is also a codeword.

The quasi-cyclic code has a minimum distance of 5. It is also linear. The code has a structure (16, 8) for allowing the most efficient use of byte-size RAM. These codes allow a correction of two error bit per stored word. A quasi-cyclic code with a structure (16, 8) and with the requisite minimum distance is described in detail in [5].

The EDAC device as an encoder the quasi-cyclic codec reads an 8-bit data vector m from the 386EX microcontroller to generate a parallel 8-bit parity vector P. The data vector is stored unaltered in RAM (refereed to us the data memory). Simultaneously the encoder stores the parity vector into parallel RAM (refereed to us the parity memory). The initial

4 Mbytes of data memory requires an additional 4 Mbytes of parity memory to implement the quasi-cyclic EDAC [4].

The first step in the decoding process is to compute the syndrome. The syndrome consists of 8 symbols and the values are computed from the read code vector. The syndrome depends only on the error vector, and is independent of the original code vector. The error detection block receives the calculated syndrome and tries to determine the error magnitude and location. Single, multiple, and triple bit errors can be introduced to the corrected data vector. When the ER port is 00, no single, two, or greater bit error is detected. In other words, the examined data has no error. When the ER port is 01, it indicates single bit error occurred within the 16-bit code word. When the ER port is 10, a two bit error has occurred within the code word. In these two cases, the error can be corrected. When the ER port is 11, errors beyond the detection capability can occur within the code word and no error correction is possible. The implementation of the quasi-cyclic EDAC method is described in detail in [3]-[4].

A new proposed EDAC system for future Earth observation small satellite missions in LEO

In this section, an on-board real-time EDAC system for future Earth observation small satellite missions is proposed. It is based on the combination of the two previous described methods: TMR and Quasi-cyclic EDAC methods.

A very simple method for implementing EDAC for SEU mitigation in an FPGA design is to replicate redundant instances of the entire Quasi-cyclic EDAC module and vote the final outputs of the modules. This is a very effective means of SEU mitigation that is easy to implement and can be performed entirely within a single device as long as the module does not utilise more than a third of the total device. In order to avoid total FPGA device failure, triple device redundancy and mitigation is proposed. This approach has the highest reliability for detecting single and multiple event upsets, multiple transient upsets, and any other functional interrupts including total device failure.

To implement the quasi-cyclic EDAC device, the choice is based on Field Programmable Gate Array (FPGA) technology, which is being the least expensive and also available in space-qualified versions. A major advantage of FPGA is power consumption and radiation tolerance in satellite applications.
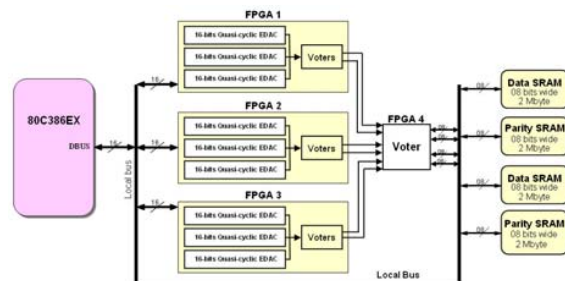

Fig. 6 Block diagram of the proposed EDAC system

The implementation of the EDAC device uses three Actel FPGAs for the encoding and decoding of the two bytes of data, and one FPGA for the majority voter circuit. This FPGA implementation is designed by technology-independent VHDL and synthesized by Synplify synthesis tool.

Fig. 6 shows a functional block diagram of the proposed EDAC system for application in the Alsat-1 OBC. Two (16,8) quasi-cyclic EDAC modules were used in parallel to handle the 16 data bits of the 80C386EX microcontroller. Each (16,8) quasi-cyclic EDAC module has been triplicated and a voter is added to vote the final outputs of the modules. A total of six (16,8) quasi-cyclic EDAC modules were used in each FPGA device.

By using the proposed EDAC system, the reliability of the SRAM is greatly increased. The 386EX micro controller uses 16-bit data words combined with 16-bit parity words. During memory read and write cycles, the codec can automatically detect and correct single-bit and double-bit errors. If any one of the SRAM chips should fail (data or parity memory), the program code can be mapped to run out of the EDAC device by using the other memory, or vice versa. In the case of FPGA device failure, the program code can be mapped to run out of the failed EDAC device by using one of the others FPGA devices. In this case the quasi-cyclic EDAC method is used without TMR.

III. EXPERIMENTAL RESULTS

The proposed EDAC system design was implemented in VHDL as described in the previous section. A powerful FPGA design and development software "Actel Libero" was used for compilation, fitting, and simulation of the design in an Actel FPGA. The design has been verified both functionally and with the timing model generated when fitting in a FPGA.

The proposed EDAC based on TMR and the quasi-cyclic EDAC is needed for computers on board a satellite when there is a definite risk of two error bits occurring within one byte of stored data and which cannot be corrected by TMR. Implementation of this EDAC is transparent to the computer: there are no interrupts and no additional computation. The overall system cost is a 100% increase in stored data, which is significantly smaller than when using TMR in a comparable context (the overall system cost is a 200% increase in stored data when using TMR). The increase in delay time, from implementing the proposed EDAC code in a typical application, is small.

To measure the performance of the proposed EDAC, a comparison between the delay times in four different EDAC devices is performed using the same FPGA technology. The first EDAC is based on the Hamming code, the second one is based on TMR technique, the third one is based on the quasi-cyclic code, and the fourth one is the proposed one. On this basis for the Actel A54SX08, a typical delay in encoding is significantly greater (2 ns for the TMR FPGA to 10 ns for the Hamming EDAC to 12 ns for the quasi-cyclic EDAC and 15 ns for the proposed EDAC); while the delay in decoding increases from 10 ns to 36 ns. For the OBC operation, this is not a significant increase in overhead, compared to a relatively long access time (typically 100 ns) of the usual low-power memory employed.

IV. CONCLUSION

This paper has presented a follow-up of some EDAC systems on-board Alsat-1 microsatellite. A powerful and efficient error correcting technique is proposed and implemented in FPGA technology. The EDAC is based on the combination of TMR and Quasi-cyclic EDAC techniques for the routine error protection of SRAM program memory for satellites in low Earth orbit. This scheme is sufficient to handle the typical SEU rate at this LEO environment, which is one bit in one million bits per day. The device is mostly transparent to the routine transfer of data between CPU and its local RAM. In-orbit observations of single and multiple event upsets are presented for the period between November 2002 and December 2008. In this period of time a total of 4982 byte errors were observed in the memory devices. From these observations, 80% of these SEUs cause single-bit errors and the remaining SEUs result in double-bit and multiple-bit errors. More than 80% of the SEUs occur in the SAA and the others are induced by the Galactic Cosmic Rays in the high latitude regions.

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