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Practical Simulation Model of Floating-Gate MOS Transistor in Sub 100nm Technologies

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***Abstract*—**As the Silicon oxide scaled down in MOSFET technology to few nanometers, gate Direct Tunneling (DT) in Floating gate (FGMOSFET) devices has become a major concern for analog designers. FGMOSFET has been used in many low-voltage and low-power applications, however, there is no accurate model that account for DT gate leakage in nano-scale. This paper studied and analyzed different simulation models for FGMOSFET using TSMC 90-nm technology. The simulation results for FGMOSFET cascade current mirror shows the impact of DT on circuit performance in terms of current and voltage without the need for fabrication. This works shows the significance of using an accurate model for FGMOSFET in nan-scale technologies.

***Keywords*—**CMOS transistor, direct-tunneling current, floating-gate, gate-leakage current, simulation model**.**

I. Introduction

THE CMOS technology has been scaled down drastically in last decade to meet the industry demand. This scaling reduced the power dissipation, increased the speed and reduced the fabrication cost. However, the reduction of feature size has led to a dramatic shrink in silicon-oxide thickness (T_{ox}) to few nanometers (nm). This in turn forces the voltage suppliers to below 1-V. unfortunately, the transistor's threshold voltage (V_T) has not reduced by the same rate. Therefore, low-voltage (LV) analog circuit design technique capable of reducing V_T such as multiple input floating-gate (FG) MOS transistor (FGMOST) is still very valuable.

Having multiple inputs at the gate of FGMOST is one of the important advantages that provide the ability to tune the threshold voltage and reduce the headroom voltage to the minimum and makes it suitable for LV applications [1]-[3]. As a result of shrinking feature size, gate leakage current (GLC) presents many challenges at the transistor's performance. When T_{ox} is less than 3 nm, direct tunneling (DT) GLC becomes a dominant problem that can increases the power dissipation and degrades the FGMOST performance. FGMOST simulation models in the literature [4]-[6] are not viable for nm scale technologies; especially for analog design. This paper focuses on the impact of DT on nm FGMOST on circuit performance and the importance of having an accurate model.

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II. FGMOS Structure and Operation

A FGMOS is very similar to standard MOS transistor but it differs in a way that it has no resistive connections to its gate and the inputs are capacitive connected to the FG. FGMOS usually fabricated using double poly structure where the first poly is the FG and the second poly is the control gate as shown in Fig. 1 (A). The FG voltage is the weighted sum of all coupled inputs voltages connected to the gate as shown in Fig. 1 (B). With no DC path to ground at the gate and having multiple inputs has resulted into several changes in the DC characteristics from the standard MOSFET. Assuming there is no leakage current at the gate, the FG voltage is given by [4] :

$$V_G = \sum_{i=1}^{n} \frac{C_i}{C_T} V_i + \frac{Q_{FG}}{C_T} \quad (1)$$

$$C_T = \sum_{i=1}^{n} C_i + C_{gs} + C_{gd} \quad (2)$$

$$V_{THFG} = \frac{C_T}{C_1} V_T - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n \quad (3)$$

where n is the number of inputs voltages at the gate, C_i are the input capacitors connected at the gate, V_i are input voltages, C_{gs} and C_{gd} are the parasitic capacitors, Q_{FG} refers to the charge trapped in FG during fabrication, V_T is the standard MOS transistor threshold voltage and V_{TFG} is the threshold voltage of the FGMOST.

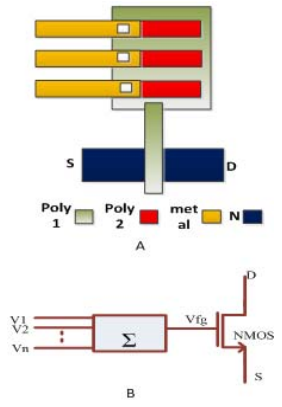

Fig. 1 (A) N-type FGMOS using double poly structure (B) equivalent circuit for floating gate transistor

FGMOSFET behaves as a programmable threshold voltage device where the effective threshold voltage V_{THFG} can be reduced to zero or to a negative value compared to standard MOS threshold. This tuning capability enabled the FGMOSFET to be the best choice for low voltage

applications. Fig. 2 illustrates the tuning capability of the FG transistor with two inputs by increasing one and sweeping the other.

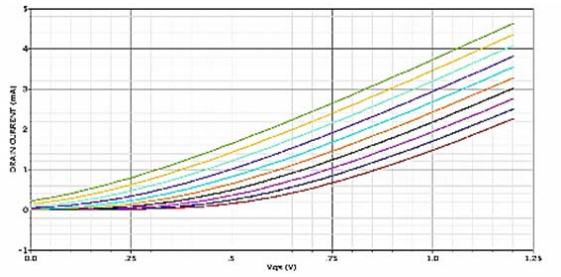

Fig. 2 FGMOS threshold voltage programmability when V_{DS} swept from 0V to 1V

III. Nano-Scale Technology Challenges

There are some problems had faced the analog designers when using FGMOST in nano-scale technologies. The first problem is the DT gate leakage current results from the direct tunneling of carriers (electrons and holes) from the gate through the very thin oxide to the bulk and source/drain regions. This leakage current degrades the FGMOST performance. It should be included in the simulation model. In the following sections previous simulation models for FGMOST and the GLC are discussed.

A. Gate Direct Tunneling in Sub 100-nm Technologies

Gate DT current results from tunneling of carriers (electrons and holes) from the gate through the oxide to the bulk and source/drain regions.

DT gate current is a strong exponential function of silicon oxide thickness (T_{ox}) and the potential across it with respect to the transistor dimensions in a way that DT increase exponentially as T_{ox} decrease and when the gate voltage increase. In [7] an empirical gate leakage model was incorporated in 100nm BSIM3v3 (level 49) and was suggested for circuit simulation where the DT gate leakage adjusted to fit 0.13um technology. The gate to source current (I_{gs}) and gate to drain current (I_{gd}) were described using voltage dependent current sources (VCCS) between gate to source and gate to drain as shown in Fig. 3. Equations (4) and (5) were extracted from simulation results and they show the dependency of I_{gs} and I_{gd} on T_{OX}, V_{gs} and V_{gd} respectively.

$$I_{gs} = \frac{127.04 \times L_{eff} \times e^{(5.606.25 \times V_{gs} - 10.6 \times T_{ox}^{-2.5})}}{2} \quad (4)$$

$$I_{gd} = \frac{127.04 \times L_{eff} \times e^{(5.606.25 \times V_{gd} - 10.6 \times T_{ox}^{-2.5})}}{2} \quad (5)$$

Fig. 4 illustrates another simulation model suggested in [8]. The model includes three terminals with the parasitic capacitors Cgs, Cgd and Cgb with the gate tunneling. The gate current in the model partitioned to Igs, Igd and Ich and they were represented by VCCS.

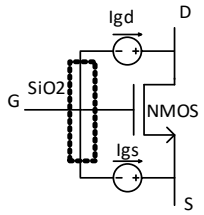

Fig. 3 DT gate current micro model proposed in [7]

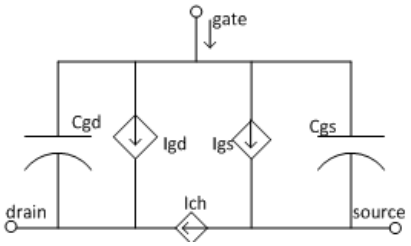

Fig. 4 Micro model for gate tunneling for circuit simulation proposed in [8]

Fig. 5 shows a micro model for the gate DT leakage current proposed in [9]. The model used a voltage dependent current sources as a function of the terminal voltages and the partitioning of the channel current (Igs, Igd) using variable resistors. The resistors and the gate current can be found in (6) and (7).

$$I_{gc} = I_{gs} + I_{gd} \quad (6)$$

$$R_{cd} = \frac{V_{cd}}{I_{cd}} \ , \ R_{cs} = \frac{V_{cs}}{I_{cs}} \quad (7)$$

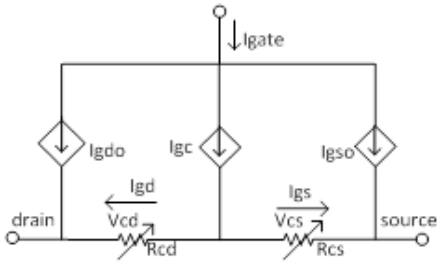

Fig. 5 Gate DT model for circuit simulation suggested in [9]

B. Simulation Model

Due to the nature of FGMOST (no DC path to ground), a dedicated simulation model is needed. A simulation model was suggested by [4] in which a standard MOSFET with multiple inputs capacitively coupled to FG was used. A large resistor and voltage-control-voltage-source (VCVS) were added to MOSFET to provide a DC path to ground as shown in Fig. 6.

In the FG simulation model proposed in [5], a resistor is connected in parallel with each input capacitor as shown in Fig. 7. These resistors were selected in a way that the RC product of each pair is equal. Furthermore, these resistors must be very large in order not to have any effect at AC simulation.

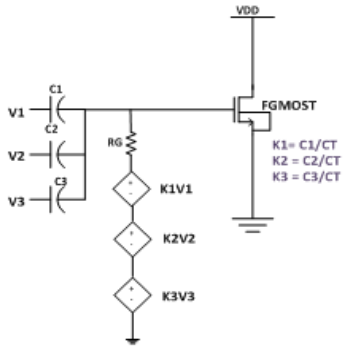

Fig. 6 Ramirez-Angulo model [4] for simulation of the FGMOS

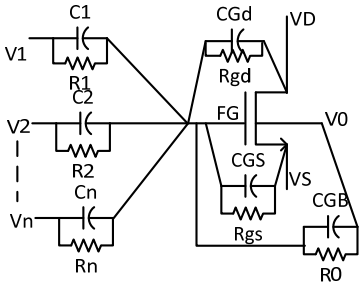

Fig. 7 FGMOS simulation model in [5]

The previous models were suggested to model the functionality of FGMMOS and to solve the simulation convergence problem. However, the DT effect in FG devices had not been explored enough.

In [10], the author investigates the impact of DT on FGMOS performance and proposed a new model for circuit in sub 100nm technologies. It was found that FG voltage decreases gradually as a function of time as can be found in (8)-(10). The reduction in gate voltage results from the direct tunneling of electrons or holes from gate to the source and from the gate to the drain respectively. The FG voltage change rate is directly related to the gate current and the input capacitance ratio seen at the gate.

$$I_{Leakage} = C_T \cdot \frac{dV_{FG}}{dt} \tag{8}$$

$$\mathrm{V_{FG}} = \frac{C_1}{C_T} V_1 + \frac{C_2}{C_T} V_2 + \cdots \frac{C_n}{C_T} V_3 \mp \mathrm{V_{leakage}} \tag{9}$$

$$\mathrm{V_{THFG}} = \frac{\mathrm{C_T}}{\mathrm{C_1}}\mathrm{V_T} - \frac{\mathrm{C_2}}{\mathrm{C_1}}\mathrm{V_2} - \frac{\mathrm{C_3}}{\mathrm{C_1}}\mathrm{V_3} - \frac{\mathrm{C_n}}{\mathrm{C_1}}\mathrm{V_n} \mp \frac{\mathrm{C_T}}{\mathrm{C_1}}\mathrm{V_{leakage}} \tag{10}$$

Fig. 8 illustrates the model implemented in TSMC90nm. The model includes two cells from analog hardware description language AHDL library and one block using Verilog A code to describe the gate tunneling. This model can be used for transient and DC simulations by adding initial condition to the leakage current integrator. Equations (11)-(13) represent DT current and gate effective voltage.

$$I_G = A \cdot e^{B.V_{fg}} \tag{11}$$

$$\mathrm{V_{leakage}} = \frac{1}{\mathrm{C_T}} \int_0^t (A \cdot e^{B.V_{fg}})\, dt \tag{12}$$

$$'V_{fg} = V_{fg} - V_{leakage} \tag{13}$$

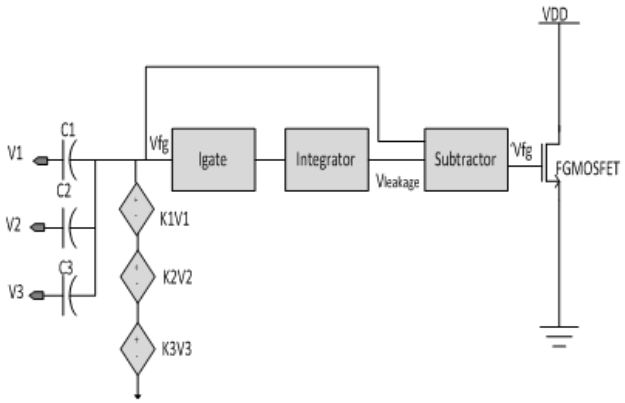

Fig. 8 The proposed FGMOST's simulation model in [10]

IV. Simulation Results

Current mirror (CM) is one of the simplest yet the important building blocks in integrated circuit design. It is used to copy or multiply the input current precisely to other circuits as shown in Fig. 9 (A). Cascode current mirror is used to improve the output impedance in CM where multiple FG stacked together as shown in Fig. 9 (B).The output current is a function of the transistor aspect ratio (W/L). The CM output current can be found in (11) and (12) respectively.

$$I_{out} = K\, I_{ref} \tag{11}$$

$$\mathrm{k} = \frac{\mathrm{I_{out}}}{\mathrm{I_{ref}}} \frac{\mathrm{W_2/L_2}\,(1+\lambda \mathrm{V_{DS2}})}{\frac{\mathrm{W_1}}{\mathrm{L_1}}\,(1+\lambda \mathrm{V_{DS1}})} \tag{12}$$

In order to examine and compare the performance of FG devices implemented in sub 100nm, a comparison carried out between a FG simulation model that counts for the DT and another simulation model that does not accounts for DT gate current. FG cascode CM was implemented in TSMC 90nm and the simulation carried out using CAD tools from Cadence / Spectre to simulate the circuit. Fig. 10 shows the dimensions (W/L) for the FG cascode CM that's used in as test bench in the comparison.

The simulation result for the FG cascode CM using Ramirez-Angulo simulation model in [4] is shown in Fig. 11. As can be seen, the required voltage to reach the required current was 227mV. Next, the same FG base CM was implemented using a simulation model proposed in [10]. This model accounts for DT in FGMOS in sub 100nm technologies. The simulation result for the output characteristic of CM was shown in Fig. 12.

We can observe that, applying the same DC voltage to the FG 227mV wasn't enough to generate the required output current 5mA. Higher gate voltage was needed 280 mV to get the required output current. This is very realistic and agrees with what reported before for gate leakages in FG devices in

[10]. This increasing in voltage was needed to compensate for gate voltage reduction that results from gate current as it is seen in (10).

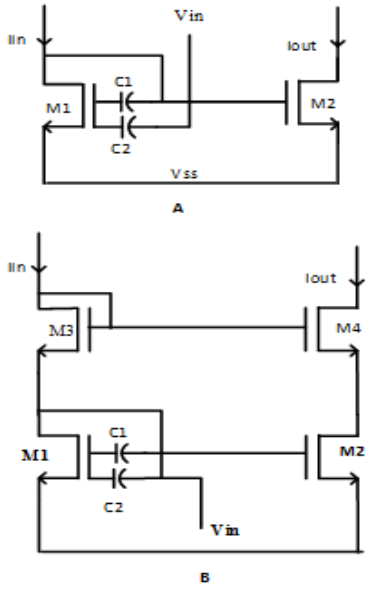

Fig. 9 FG current mirror (A) simple FG cell (B) cascade cell

V_{DD}	I_{ref}	M_1	M_2	M3	M4	I_{out}
1.2V	50uA	W=50um L=1um	W=500um L=1um	W=80um L=1um	W=80um L=1um	5mA

Fig. 10 FG current mirror transistors dimensions

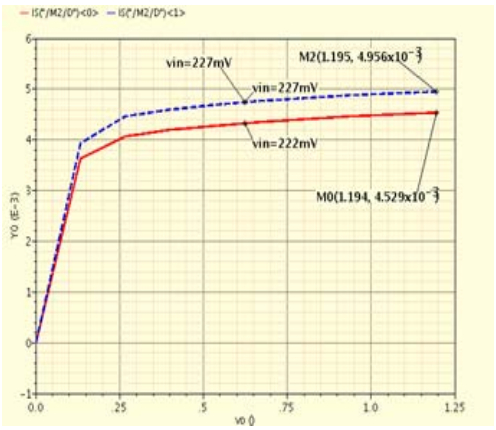

Fig. 11 The output current verse output voltages for FG cascode current mirror implemented with Ramirez model

The FG cascode CM using Ramirez model didn't account for that DT therefore, the result was not accurate. The importance of these results arises from the need to have an accurate and realistic simulation results for FGMOSFET in deep nanotechnologies without the need to fabricate.

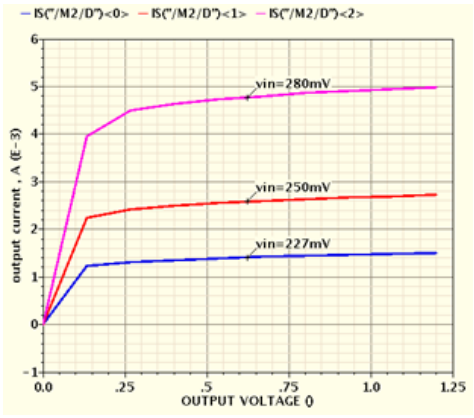

Fig. 12 The output current against output voltage for FG cascode current mirror implemented with the model in [10]

V. Conclusion

In this paper, a discussion has been presented to show the importance of using an accurate model for FGMOSFET in nano-scale technologies. Different models for FGMOSFET available in the literature have been compared. The simulation results had shown the gate DT impacts on circuit performance in terms of current and voltage.

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