Power MOSFET Models Including Quasi-Saturation Effect

Abdelghafour Galadi

Abstract—In this paper, accurate power MOSFET models including quasi-saturation effect are presented. These models have no internal node voltages determined by the circuit simulator and use one JFET or one depletion mode MOSFET transistors controlled by an "effective" gate voltage taking into account the quasi-saturation effect. The proposed models achieve accurate simulation results with an average error percentage less than 9%, which is an improvement of 21 percentage points compared to the commonly used standard power MOSFET model. In addition, the models can be integrated in any available commercial circuit simulators by using their analytical equations. A description of the models will be provided along with the parameter extraction procedure.

Keywords—Power MOSFET, drift layer, quasi-saturation effect, SPICE model, circuit simulation.

I. INTRODUCTION

THE unipolar power MOSFET transistor integrates in its structure the high voltage drift region (Fig. 1). Breakdown voltage of the power MOSFET is determined by the thickness and the doping level of the drift epitaxial layer [1]. Unfortunately, this drift region introduces an intrinsic feedback gate-drain capacitance and a nonlinear resistance depending on gate and drain voltages. Unlike the conventional MOSFET, in power MOSFET devices we note a diminishing of drain current level at high gate and drain voltages, as shown in transfer and output characteristics (Figs. 2 and 3). This well-known phenomenon called quasi-saturation [2]-[4] occurs due to the carrier velocity saturation in the high voltage drift region. The quasi-saturation effect appears in various power MOSFET structures like standard, trench and superjunction power MOSFET devices [5], [6]. Therefore, quasi-saturation effect must be taken into account in the modeling of power MOSFET devices.

The carrier velocity saturation, the JFET effect at high drain voltages and the mobility degradation, in accumulation and inversion layers at the surface of silicon [7], make the modeling of power MOSFET more complex. In literature, various power MOSFET models were proposed [8]-[14]. These models use a subcircuit consisting of an equivalent circuit of the power MOSFET structure. The subcircuit combines a traditional MOSFET transistor, representing the channel region, in series with resistance or JFET transistor representing the drift region.

Two approaches were used to describe the subcircuit: compact model [8]-[11] and macromodel [8], [12]-[14]. The

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most proposed compact models, based on MOS surface potential [8], [10], [11], need technological and geometrical parameters which are not revealed by the most power MOSFET manufacturers. Recently, a compact power MOSFET model using experimental extraction parameters was proposed [9]. This model is based on an internal drain node calculated iteratively using the drain current equations and drift resistance equation [9]. Despite the parameter extracting technique using the available datasheets, the exponential parameter equations and iterative determination of internal drain node [9] can introduce longer analysis time and convergence problem in simulations.

Macromodels can be useful thanks to their simulator independency and their high flexibility by using standard SPICE models. Different macromodel configurations including quasi-saturation effect were published using bias dependent resistance or JFET transistor in series with dependent voltage source to model the nonlinear drift resistance [8], [12]-[14]. The main disadvantages of these macromodels are the large number of the components and the additional fitting nonphysical elements using nonlinear equations. On the other hand, the standard macromodels available in website of the most power MOSFET manufacturers introduce very large errors compared to measurements (Fig. 3) [15]. This models use a simple conventional SPICE level 1 or level 3 MOSFET model to describe the electrical behavior of the power MOSFET.
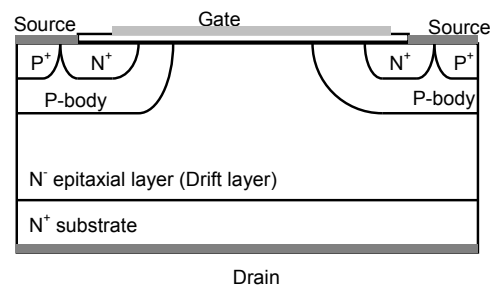

Fig. 1 Conventional power VDMOSFET structure

In this paper, two models including quasi-saturation effect are presented. The proposed models are based on physical structure of the power MOSFET without using internal node voltages. The model parameters are based on simple parameter extraction procedure using experimental data. It will be shown that the error percentage in the simulated drain current will be reduced from 30% to 9% using the proposed models instead of the standard model. Therefore, the proposed models match the

experimental results without any problem of convergence. In this modeling, the device samples used to validate the models are the STP36NF06L N-channel standard power MOSFET, the HUF76419S3ST_F085 N-channel trench power MOSFET and the SPW24N60C3 superjunction N-channel power MOSFET [16].

In Section II, the equivalent circuit models and the drain current equations in linear and saturation regions will be presented. Section III is devoted to the procedure of parameter extraction and Section IV describes the simulation results obtained with the model compared to measurements. Finally, conclusion is presented at the end of text.
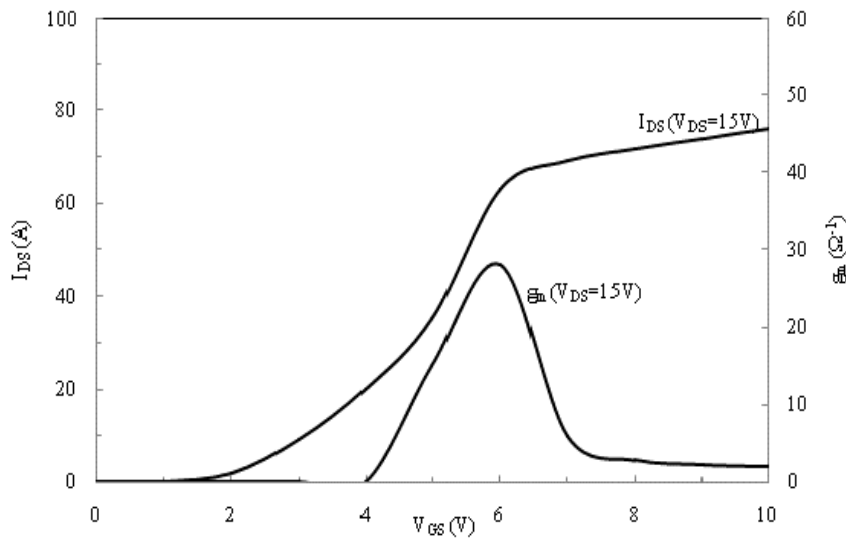

Fig. 2 Measured I_{DS}-V_{GS} and g_m-V_{GS} characteristics of a 60 V N-channel standard power MOSFET transistor at V_{DS}=15V
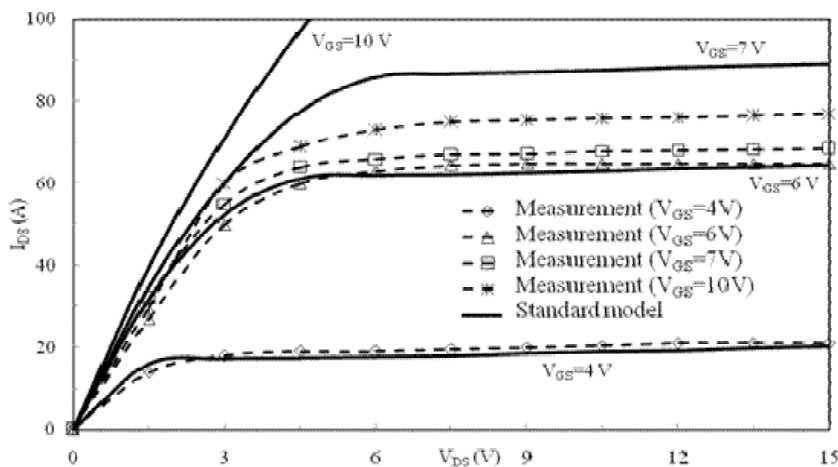

Fig. 3 Measured output characteristics in comparison to the standard power MOSFET model of a 60 V N-channel standard power MOSFET transistor

II. MODEL DESCRIPTION

The proposed models use channel intrinsic MOSFET in series with JFET or N-channel depletion mode MOSFET to model the drain current in the on-state of the power MOSFET structure as shown in Figure 4. One "effective" gate voltage is added to equivalent circuit to take into account the small variation of the drain current with the gate voltage at the quasi-saturation regime. The body diode represents the intrinsic P-source/N⁻-drift/N⁺-substrate diode. This diode is very useful because it will be used to take into account the breakdown voltage of the power MOSFET by the "BV" SPICE diode parameter and the forward behavior in the case of negative drain-source voltage.

The models are based on physical structure of the power MOSFET device (Fig. 1) and it can be used to model various types of power MOSFET devices. In these models, channel region is modeled by using alpha power-law MOSFET model [17], [18] while the drift region is represented by a JFET or N-channel depletion mode MOSFET (NDMOSFET) transistors.
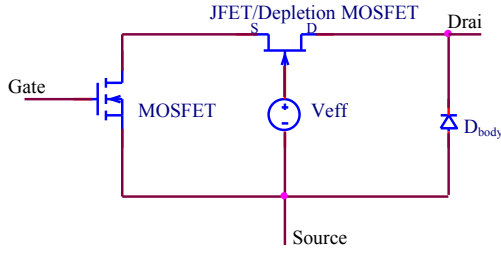
Fig. 4 Subcircuit model

In accordance with the power MOSFET structure (Fig. 1), the drain of the JFET/NDMOSFET is the same as the drain of the power MOSFET. The source of the JFET/NDMOSFET is the same as the internal drain node of the intrinsic MOSFET representing the channel region.

The voltage-controlled voltage source V_{eff}, between the source of the power MOSFET and the gate of the JFET/ NDMOSFET, is added to circuit to take into consideration the small voltage drop across the intrinsic channel region at the quasi-saturation regime ($V_{GS} \geq V_{GSC}$). In accordance with the power MOSFET structure (Fig. 1), the voltage drop across the channel region is equal to gate-source voltage of the JFET/ NDMOSFET transistors. JFET/NDMOSFET transistors represent the drift nonlinear resistance with taking into account mobility degradation and carrier velocity saturation.

For low gate voltages ($V_{GS} < V_{GSC}$), the drain current is governed by the intrinsic MOSFET transistor. To avoid the transition region problem related to standard MOSFET SPICE models, the use of the nth power law MOSFET model is preferred because of the accuracy and the high flexibility of this model [17], [18]. In nth power law MOSFET model, the drain current equations can be expressed as [17]:

$$
I_{DS} = \begin{cases} 0 & \text{if} \quad V_{GS} \leq V_{TM} \\ I_{D0}\left(2 - \dfrac{V_{DS}}{V_{DSAT}}\right)\dfrac{V_{DS}}{V_{DSAT}} & \text{if} \quad V_{DS} < V_{DSAT} \\ I_{D0} = I_{DSAT}(1 + \lambda_M V_{DS}) & \text{if} \quad V_{DS} \geq V_{DSAT} \end{cases} \tag{1}
$$

$$
I_{DSAT} = B\left(V_{GS} - V_{TM}\right)^n \tag{2}
$$

$$
V_{DSAT} = K\left(V_{GS} - V_{TM}\right)^m \tag{3}
$$

where V_{GS}, V_{DS} and V_{DSAT} are gate-source, drain-source and drain-source saturation voltage, respectively. V_{TM} is the threshold voltage and I_{DSAT} is the saturation drain current. K and m model parameters control the linear region while B and n control the saturation region of operation in output characteristics. The parameter λ_M is added to take into consideration the channel length modulation which measures the output conductance in saturation region.

When the gate voltage is high ($V_{GS} \geq V_{GSC}$), quasi-saturation effect occurs and the drain current is controlled by the nonlinear drift resistance representing by the JFET/ NDMOSFET transistors (Fig. 4). The channel resistance is small compared to the drift resistance [3] therefore the drain-

source voltage V_{DS} of the power MOSFET is considered to be the V_{DS} of the JFET/NDMOSFET transistors. In case of using JFET transistor to model the drain nonlinear resistance, the drain current is defined by the following equations:

$$
I_{DS} = \beta V_{DS}\left(2(V_{eff} - V_p) - V_{DS}\right), \qquad V_{DS} < V_{GS} - V_p \tag{4}
$$

$$
I_{DS} = \beta\left(V_{eff} - V_p\right)^2, \qquad V_{DS} \geq V_{GS} - V_p \tag{5}
$$

β (BETA) and V_p are the JFET transconductance coefficient (A/V^2) and the pinch-off voltage respectively. The two JFET SPICE model parameters β and V_p can be extracted using drain current equation for $V_{GS} = V_{GSC}$ in linear and saturation regions in the quasi-saturation regime assuming the JFET gate-source voltage $V_{GSJ} = V_{eff} = 0$.

The "effective" gate voltage V_{eff}, corresponding to the voltage controlled voltage source, represents the voltage drop across the intrinsic channel MOSFET when quasi saturation regime occurs. At first approximation, the V_{eff} is assumed to be a linear dependent voltage source controlled by the gate voltage. Therefore, the equation that governs V_{eff} can be written as:

$$
V_{eff} = gV_{GS} + V0 \tag{6}
$$

The equation parameters g and V0 can be extracted using the measurements drain current at quasi-saturation regime. By choosing $V_{eff} = 0$ when the quasi-saturation regime occurs ($V_{GS} = V_{GSC}$), the following relation can be added to extract the two "effective" gate source voltage parameters:

$$
V0 = -gV_{GSC} \tag{7}
$$

Breakdown voltage of the power MOSFET is considered by the "BV" SPICE parameter of the Dbody diode. The static other diode parameters (i.e. saturation current Is, emission coefficient N and Ohmic resistance Rs) can be extracted by using the source-drain forward characteristic of the power MOSFET as given in datasheet.

III. PARAMETER EXTRACTION

The critical gate voltage V_{GSC} parameter is extracted from the transfer characteristic at high drain voltage (saturation region at the peak of the transconductance g_m) as shown in Fig. 2.

A. Channel MOSFET Parameter Extraction

The channel MOSFET model parameters are extracted and specified from measured output characteristics with respect to the extraction procedure introduced in [17].

B. JFET/NDMOSFET Parameter Extraction

For the JFET, two parameters are required: the transconductance β and the pinch-off voltage V_P. To determine the JFET two model parameters β and V_P, we consider that at the onset of the quasi-saturation regime ($V_{GS} = V_{GSC}$) $V_{eff} = 0$. The slope factor at low drain-source

voltage and the saturation drain current at $V_{GS}=V_{GSC}$ can be written as:

$$\frac{1}{R_d} = -2\beta V_p, \qquad V_{DS} << V_{GS} - V_p \qquad (8)$$

$$I_{DSAT} = \beta (V_p)^2, \qquad V_{DS} > V_{GS} - V_p \qquad (9)$$

R_d is the JFET/NDMOSFET resistance in the linear region (low drain voltage). I_{DSAT} is the saturation drain current in the saturation region for $V_{GS}=V_{GSC}$.

V_p parameter can be determined by using the product of I_{DSAT} by R_d while the transconductance parameter β will be calculated from (8) or (9).

C. The Voltage Controlled Voltage Source Parameter Extraction

The two parameters needed for the determination of the "effective" gate voltage V_{eff}, g and V0, can be extracted by using another curve of the I_{DS}-V_{DS} characteristics at the quasi-saturation regime. If we consider another value of the drain current I_{DSATM}, which is the saturation drain current, obtained for $V_{GS}=V_{GSM}$ ($V_{GSM}>V_{GSC}$). By using (4) and (5), the parameter g can be expressed as follows:

$$g = \frac{\sqrt{\dfrac{I_{DSATM}}{\beta}} + V_p}{V_{GSM} - V_{GSC}} \qquad (10)$$

On the other hand, the V0 parameter can be calculated using (7).

IV. RESULTS

Fig. 3 shows the simulated drain current results obtained with the standard power MOSFET model in comparison to the measurements. The standard power MOSFET model cannot simulate the high gate bias conditions. On the other hand, Fig. 5 shows the simulated, with the proposed model, and the measured output characteristics of the N-channel standard power MOSFET. At low gate voltage, the nth power law MOSFET model matches accurately the experimental results. At the quasi-saturation regime, a good agreement between the simulated and measured results is observed (the average error percentage is less than 6% while the maximum error percent is less than 9%). This modeling is also applied to model the N-channel trench power MOSFET HUF76419S3ST_F085 (Fig. 6) and the N-channel CoolMOS SPW24N60C3. In the two cases, the model matches the experimental results (with an average error percent less than 9% and maximum error percent less than 12%). Unlike the standard power MOSFET models, the error percent introduced by the proposed model remains practically constant with increase of gate-source voltage V_{GS}.

In this work, the maximum simulated error is high at the transition region of operation at the quasi-saturation regime. Model [19] can be used to improve the JFET part model in the quasi-saturation regime. This model describes more accurately the transition region avoiding the first derivative discontinuity problem introduced by the level 3 SPICE model. Furthermore, while the effective gate-source voltage gives accurate simulation results its equation should be reviewed to minimize the error in the transition region. In these models, the parameter extraction procedure is based on empirical parameters without revealing any geometrical or technological manufacturer parameters at silicon level.
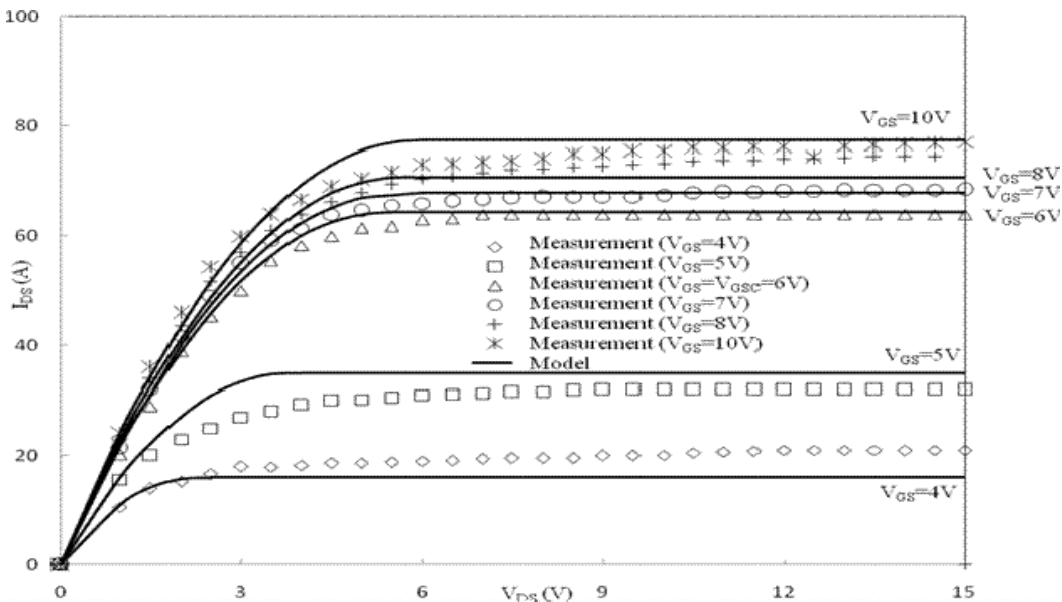

Fig. 5 Measured output characteristics in comparison to the proposed model of a 60 V N-channel standard power MOSFET transistor
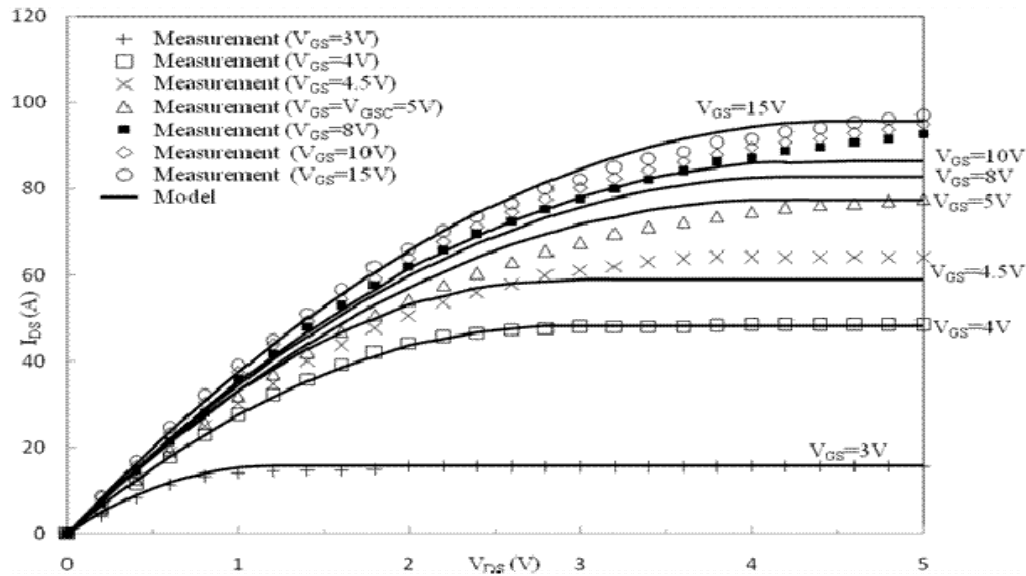
Fig. 6 Measured output characteristics in comparison to the proposed model of a 60 V N-channel trench power MOSFET transistor

V. CONCLUSION

This paper describes two SPICE models for power MOSFET transistor including quasi-saturation effect. The proposed models have no additional internal nodes and provide very fast convergence. The efficiency of these models is demonstrated by the good agreement between the simulated and experimental results in all operating regions of the power MOSFET device. The complete parameter extraction method was described. Finally, the physically based models can be easily implemented in any SPICE-based circuit simulator.

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