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On-Chip Aging Sensor Circuit Based on Phase Locked Loop Circuit

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***Abstract*—**In sub micrometer technology, the aging phenomenon starts to have a significant impact on the reliability of integrated circuits by bringing performance degradation. For that reason, it is important to have a capability to evaluate the aging effects accurately. This paper presents an accurate aging measurement approach based on phase-locked loop (PLL) and voltage-controlled oscillator (VCO) circuit. The architecture is rejecting the circuit self-aging effect from the characteristics of PLL, which is generating the frequency without any aging phenomena affects. The aging monitor is implemented in low power 32 nm CMOS technology, and occupies a pretty small area. Aging simulation results show that the proposed aging measurement circuit improves accuracy by about 2.8% at high temperature and 19.6% at high voltage.

***Keywords*—**Nanoscale, aging, effect, NBTI, HCI.

I. Introduction

CIRCUIT aging is a phenomenon where electrical parameters and physical dimensions deviate from the standard values during the operating process. In modern nanometer CMOS technology, circuit aging is becoming the most important factor resulting in circuit performance degradation. Subsequently, a lot of researchers have studied these problems and they have illustrated the mechanism of transistor aging. For example, negative bias temperature instability (NBTI) and hot carrier injection (HCI) cause shifting in threshold voltage, electro migration (EM) leads to increase interconnect resistance, and time-dependent dielectric breakdown (TDDB) causes catastrophic transistor gate breakdown. Consequently, the reaction–diffusion model is proposed to describe the mechanism of circuit aging, as shown in Fig. 1 [1].

Other research studies have been carried out to develop countermeasures to reduce the effects of circuit aging. For example, [2] proposed PVT-and-aging adaptive word line boosting for 8T SRAM power reduction. Proposed in [3] was an adaptive body bias scheme for reducing the impacts of NBTI and process variations on 6T SRAM cells. Reference [4] describes modeling and hardware results of how the soft-error rate (SER) of a 65-nm silicon-on-insulator SRAM memory cell changes over time because semiconductor aging effects shift the SRAM cell behavior. Reference [5] extended previous research by contributing a sensing scheme that employs on-chip sensors capable of accurately tracking NBTI pMOS current degradations across process, temperature, and varying activity factors. The results in [5] show that a pretty big sensing area with an overall system accuracy of 90% in the case of voltage threshold precision of 2 mV.

As the manufacturing process is scaled down to the nanoscale, effectively monitoring and quantizing circuit aging is becoming a key technology. Proposed in [6], was an on-chip reliability monitor that measures the beat frequency of two ring oscillators, one stressed and the other unstressed, to individually monitor NBTI. This paper proposes a high accuracy aging measurement circuit which using PLL and VCO circuit for monitoring MOSFET circuit aging.

II. Aging Monitor Work Mechanism

Each of the aging mechanisms has different sensitivities to operating conditions and process changes, and can be more critical in certain circuit topologies. NBTI and HCI for NMOS and PMOS transistors are shown in Fig. 2, as well as for an inverter during standard operation.

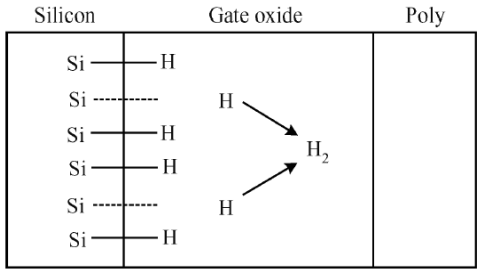
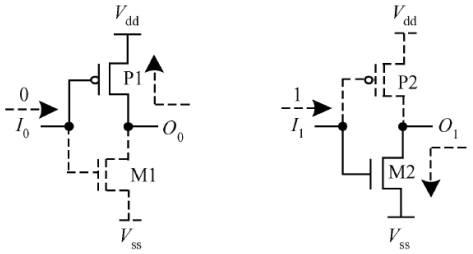


Fig. 1 The reaction–diffusion model



(a) NBTI stress (b) HCI stress

Fig. 2 NBTI and HCI for NMOS and PMOS transistors

Based on the reaction–diffusion model, the V_{th} change describes circuit aging after long term degradation. The following equation describes the dependence of circuit aging and design parameters, during either static or dynamic operation [7].

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$$\Delta V_{th} = K_\vartheta \beta^{0.25} T^{0.25} \left\{ \frac{1-\left[1-\sqrt{\eta(1-\beta)/n}\right]^{2n}}{1-\left[1-\sqrt{\eta(1-\beta)/n}\right]^{2}} \right\}^{0.5} + \delta_\vartheta \quad (1)$$

In (1), ΔVth is the Vth change value and β is the duty cycle. T is the clock period and n is the number of clock cycle. K, and are the constant coefficient. The Vth change will affect the circuit performance. For example, the switching threshold of CMOS inverter VM is defined as the point where Vin=Vout, and its value can be obtained as [8]:

$$V_M = \frac{V_{Tn}+r(V_{DD}+V_{Tp})}{1+r}, r = \sqrt{\frac{-k_p}{k_n}} \quad (2)$$

where VTp is the threshold of PMOS and VTn is the threshold of NMOS; kp and kn are the constant coefficient. And also, the switching threshold decides the frequency of VCO. So, circuit aging will cause VCO frequency degradation. As shown VCO frequency degradation, we can get the corresponding circuit performance degradation from (3):

$$\Delta d(\vartheta) = \alpha \frac{f_1 - f_0}{f_0} P_0 \quad (3)$$

where α is the coefficient, P0 is the original circuit performance, f0 is the original frequency, and f1 is the degenerated frequency. So, VCO frequency degradation can be used to measure the circuit performance degradation.

III. Proposed Aging Monitor Circuit

A. Design of VCO Circuit

This section presents a new aging monitor scheme based on the reference circuit (PLL) and aging generation circuit (VCO). The proposed scheme measures the frequency of a PLL aging affectless device and VCO aging effect device, and they digitalize the difference in the measured frequency. The core circuits for detecting frequency difference due to aging phenomenon consist of an aging generation circuit, a reference circuit, a comparator circuit, and an output circuit, as shown in Fig. 3.

The VCO circuit comprises an oscillator, level shifter, duty cycle, and frequency divider [9]. The architecture of VCO is shown in Fig. 4.

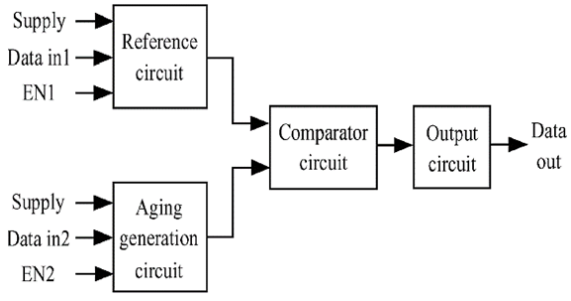

Fig. 3 Block diagram of an aging monitor scheme

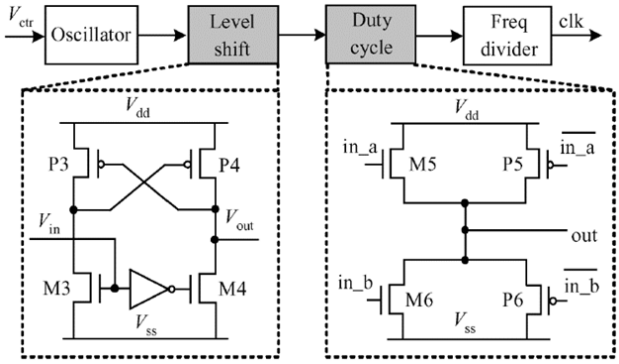

Fig. 4 The schematic of VCO circuit

The oscillator circuit is formed by an odd number of differential delay units, and its output frequency fOSC meets the following equation [10]:

$$f_{osc} = 1/(2MT_D) \quad (4)$$

where T_D is delay time of the delay element and M is the number of that delay elements (in this design, M=9). Because of the process deviation during the production of the chip, the different VCO chips will output different frequencies under the same condition. In the VCO circuit, the level shift converts the output frequency from Vctr to Vdd, and duty cycle circuit keeps the output frequency at 50%.

B. Design of PLL Circuit

A unique property of general PLL is that it captures any variations in operating condition and takes an adaptive measure to produce a stable clock from the VCO [11]. Specifically, a feedback loop is formed between the VCO and a reference clock. Depending on the comparison between the VCO and the off-chip clocks, an optimal control voltage is applied to VCO in order to match the two clocks [12]. The scheme of PLL circuit consist of phase frequency detector (PFD) circuit, charge pump (CP) circuit, low pass filter (LPF) circuit, VCO, and frequency divider [13], as shown in Fig. 5.

C. Design of Aging Monitor Circuit

This section presents an aging monitor based on the before mentioned PLL and VCO circuits. The proposed circuits measure the reference clock of PLL without aging effect MOSFET device and sensor clock of VCO with aging effect MOSFET device, and they digitalize the difference in the measured frequencies. The block diagram of aging monitor consists of one PLL circuit, multiple VCO circuits, control circuit, phase comparator, counter and shift register, as shown in Fig. 6. Clock, EN, CLK and Vctr signals for this experiment are provided externally, and the parameter degradation caused by aging is converted to a digital data with a counter.

The timing sequence of an aging monitor is simplified due to the phase comparator architecture. Once each of the input signals (Measure, PLL_EN and VCO_EN) are triggered, a phase comparator is employed to generate a pulse signal (Enable), as shown in Fig. 7. The width of the Enable pulse is

decided by the beat-frequency between PLL and VCO. The Enable signal in Fig. 7 triggers the counter, which starts to count the fPLL signal, and each OUT signal in the counter can be employed as measure signals due to the aging phenomena. Fig. 7 shows the timing sequence waveforms in the aging monitor during the measurement mode. Td1 is the delay time from measure to VCO enable. Td2 is the start-up time of VCO circuit. Td3 is the working time of aging monitor.

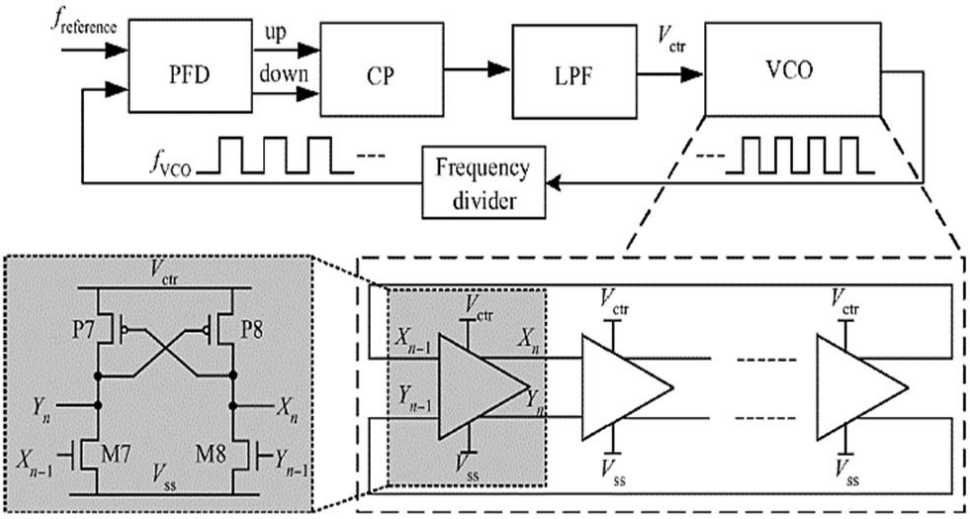

Fig. 5 The schematic of the PLL circuit

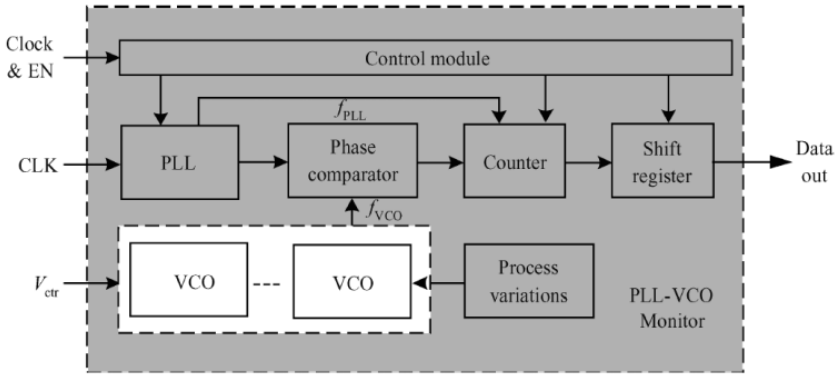

Fig. 6 Block diagram of aging monitor

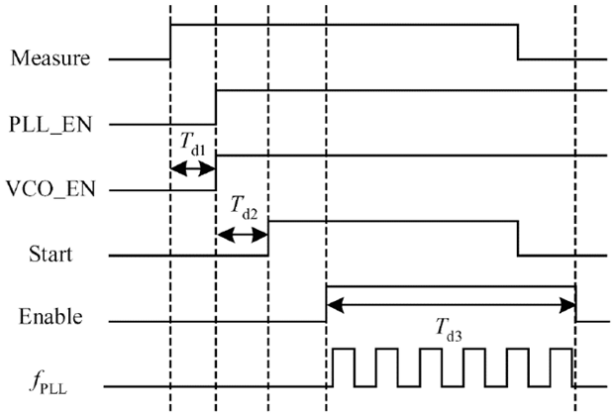

Fig. 7 The timing diagram of the aging monitor

IV. Topology of Aging Monitor Circuit

The proposed monitor has been implemented with a 32 nm low-power CMOS technology. Fig. 8 shows the layout of the aging monitor. The monitor area is 303.28X 298.94 m2. It is designed by a full-custom method using six metal layers (M1, M2, M3, M4, M5 and M6). Metal layers M1, M2, M3, and M4 are used for routing the supply rails. M5 and M6 are used for routing the signal lines.

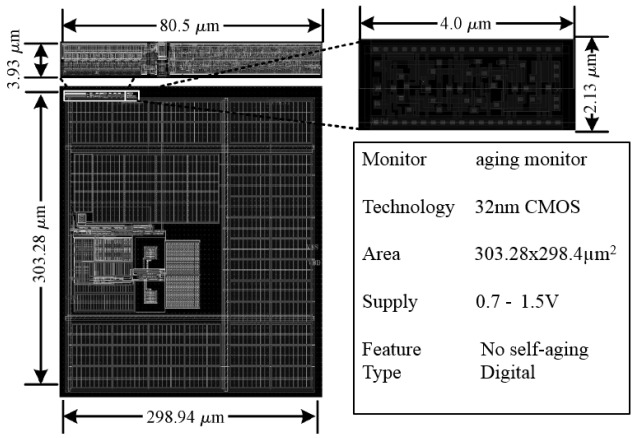

Fig. 8 The layout of proposed aging monitor

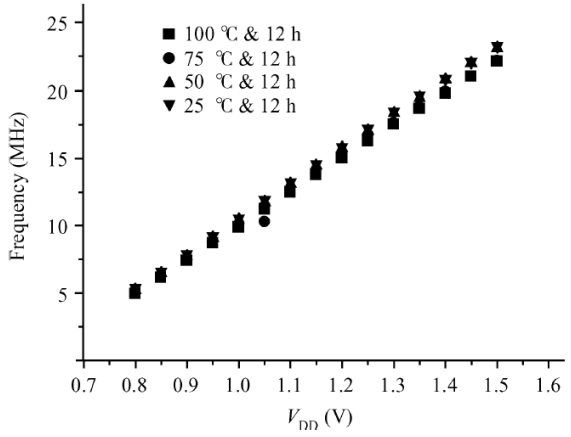

Fig. 9 High temperature VCO frequency aging curve

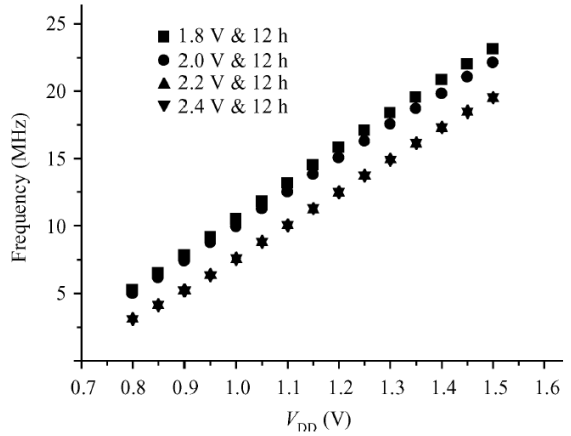

Fig. 10 High voltage VCO frequency aging curve

V. High Temperature Circuit Aging

High temperatures will significantly affect the circuit aging phenomenon because the Si–H bonds are more easily broken at a higher temperature, thereby increasing the concentration of traps in the channel section. The control voltage ranges from 0.8 to 1.5 V with each step 50 mV. The initial output frequency ranges from 4.98 MHz to 23.15 MHz at 270C. After simulations of circuit aging in the environment temperature from 250C to 1000C, the recorded frequencies and the aging curve are shown in Figs. 9 and 10.

VI. Performance Analysis

As shown for frequency degradation, we can get the corresponding circuit performance degradation from (5):

$$\Delta \boldsymbol{d}(\vartheta) = \boldsymbol{\alpha} \frac{\boldsymbol{f_{VCO} - f_{VCO0}}}{\boldsymbol{f_{VCO0}}} \boldsymbol{P_0} \quad (5)$$

where a=1 is the coefficient, P0 is the original circuit performance, and fVCO0 is the original frequency. There might be several Δf=fVCO-fVCO0 of different aging conditions. In such cases, we select the largest one to calculate the performance degradation, which is the worst case aging. High temperature aging test results show that the frequency degradation is about 2.8%. High voltage aging test results show that the frequency degradation is about 19.6%. So, the performance degradation of the test chip is 2.8% P0 under high temperature aging and 19.6% P0 under high voltage aging. In a comparison with the same technology node of the monitor circuit in [6], this work eliminates the circuit self-aging effect by about 19.6%. This study proposes an aging monitor that can accurately characterize and track the aging effect in digital circuits better than the analog circuits in [3].

VII. Conclusions

In this paper, an aging monitor has been proposed for monitoring digital circuit aging performance degradation. The proposed monitor eliminates the circuit self-aging effect, and improves accuracy at high temperature by about 2.8% and at high voltage by about 19.6%. High temperature and high voltage changes, which have a significant impact on circuit performance degradation due to aging, are considered in the simulations.

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