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Novel Sinusoidal Pulse Width Modulation with Least Correlated Noise

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***Abstract*—**This paper presents a novel sinusoidal modulation scheme that features least correlated noise and high linearity. The modulation circuit, which is composed of a quantizer, a resonator, and a comparator, is capable of eliminating correlated modulation noise while doing modulation. The proposed modulation scheme combined with the linear quadratic optimal control is applied to a single-phase voltage source inverter and validated with the experiment results. The experiments show that the inverter supplies stable 60Hz 110V AC power with a total harmonic distortion of less than 1%, under the DC input variation from 190 V to 300 V and the output power variation from 0 to 600 W.

***Keywords*—**Pulse width modulation, feedback dithering, linear quadratic control, inverter.

I. Introduction

SINUSOIDAL pulse width modulation (SPWM) [1], widely applied to an inverter for DC-to-AC conversion [2, 3] or motor drive [4, 5], is a technique to convert a sinusoid to a multi-level switched waveform by performing amplitude modulation and pulse width modulation [5-7]. Two most concerned issues for SPWM are its switching frequency and signal quality. The switching frequency determines the switching loss of the inverter, and the signal quality is related to the amount of noise, harmonics, and tones present at the output of the inverter.

This work focuses on the second design issue, attempting to derive a novel SPWM to enhance its signal quality. The proposed design is mainly derived from the feedback dithering concept recently developed in [8]. Figure 1 displays the block diagram of the proposed modulation. The modulation is performed by a dithered quantizer, where the dither is generated by feeding back the modulation noise n through a resonator and a comparator. The feedback dithering automatically randomizes the noise and eliminates the correlated noise present at the output, so as to attenuate in-band noise and make the modulator behave like a linear gain added with uncorrelated noise.

II. Feedback Dithering Modulation

Figure 1 shows the block diagram of a feedback dithering modulator that is designed to perform SPWM. The modulator consists of a quantizer and a recently developed feedback dithering circuit [8]. The quantizer quantizes a sinusoidal signal to a prescribed set of levels, say {–1, 0, 1} for normalized three-level modulation. A binary dither δ that is generated by the feedback dithering circuit intends to randomize the quantization pattern and eliminate correlated noise.

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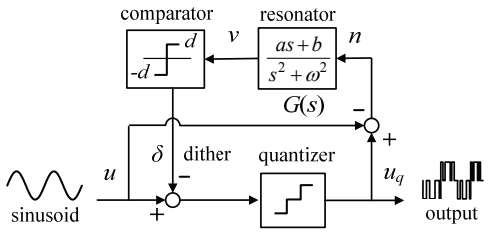

Fig. 1 Feedback dithering modulation

The feedback dithering circuit, made from a resonator G and a comparator, is responsible for minimizing the correlation between modulation noise n and sinusoidal input u. First, the resonator G performs correlation estimation, and its resonant frequency ω is the same as the frequency of the sinusoidal input u. Under the assumption of zero initial conditions, the output of resonator G in Fig. 1 is

$$v(t) = \int_0^t A\sin(\omega\tau + \theta)n(t-\tau)\,d\tau\,, \tag{1}$$

where $A\sin(\omega t+\theta)$ is the impulse response of G. In the steady state, the resonator's output level can be used to estimate the magnitude of the cross-correlation function $R(t)$ of sinusoidal input u and modulation noise n,

$$R(t) = \lim_{T\to\infty}\int_0^T u(\tau)n(\tau + t)\,d\tau\,. \tag{2}$$

Obviously $R(t)$ is zero when $v(t)$ is bounded. Thus, to achieve complete decorrelation $R(t) = 0$, the dither signal δ should be designed to influence the quantization so that the resulting modulation noise n will minimize and bound the resonator output level. The choice of the instantaneous value of dither signal δ obeys the following simple rule

$$\delta(t) = d\,\mathrm{sgn}\,v(t)\,, \tag{3}$$

where $\operatorname{sgn} v = 1$ when $v \geq 0$, else $\operatorname{sgn} v = -1$. With sufficiently large amplitude d, the binary dithering ascertains positive modulation noise $n(t)$ when $v(t) < 0$ and negative $n(t)$ when $v(t) > 0$, hopefully to diminish the resonator output v.

III. Stability and Performance Analysis

The feedback dithering modulator in Fig. 1 is operated in the sliding mode [9] with the sliding surface being $v = 0$, constantly steering the resonator output v to zero. Suppose that the state space representation of the resonator is

$$\begin{cases} \dot{x} = Ax + Bn \\ v = Cx \end{cases} \tag{4}$$

where the modulation noise n is related to the quantization error $e = u_q - (u - \delta)$ and the dither signal $\delta = d \operatorname{sgn} v$ by

$$n = u_q - u = e - \delta . \tag{5}$$

By (4) and (5) together with the assumption $CB > 0$ (i.e., leading coefficient a of G in Fig. 1 is positive), we have

$$\begin{aligned} v\dot{v} &= vC\dot{x} \\ &= v(CAx + CBe - CB\delta) \\ &= CBv[(CB)^{-1}CAx + e - d \operatorname{sgn} v) \\ &= CB\,|v|\left\{\operatorname{sgn} v[(CB)^{-1}CAx + e] - d\right\} < 0 , \end{aligned} \tag{6}$$

where the dither amplitude d is selected to meet the condition

$$d > |(CB)^{-1}CAx + e|, \text{ for all time.} \tag{7}$$

Inequality (6) ascertains the diminishing of v. Under the assumption that the coefficients a and b of resonator $G(s)$ in Fig. 1 are positive (i.e., G is of relative degree 1 and has a Hurwitz numerator polynomial), inequality (7) suffices to guarantee the stable operation of the sliding mode $v = 0$. Note that, without quantizer overload, the quantization error e is bounded by half the quantization step size. It implies that the required dither amplitude d can be set a smaller value when the quantization resolution gets higher.

When used in the power electronics applications, the modulator should have a limited switching frequency to avoid excess switching loss caused by the high-frequency switching of power transistors. This can be done by replacing the instantaneous quantizer in Fig. 1 by a clocked quantizer that quantizes a signal at each rising edge of a clock and holds constant in the remaining clock period. In this case, the resonator output v will not be perfectly zero. As shown in Fig. 2, v will swing in some vicinity of zero, with its amplitude limited by its maximum increment in a clock period T:

$$|v| < \max_t \int_t^{t+T} CB\left\{d - \operatorname{sgn} v\,[(CB)^{-1}CAx + e]\right\} < \Delta v_{\max} , \tag{8}$$

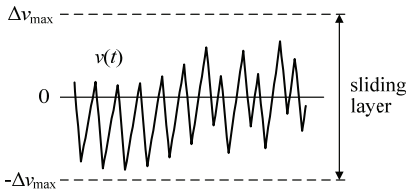

Fig. 2 The feedback dithering modulator steers the resonator output v toward zero in each rising edge of the clock, thereby constraining the resonator output v in a sliding layer $|v| < \Delta v_{\max}$, where $\Delta v_{\max}$ is a least upper bound of the maximum increment of v in a clock period.

where, by (7),

$$\Delta v_{\max} = 2CBdT . \tag{9}$$

The higher the quantization resolution (lower required d) and the higher the clock rate (lower T), the lower the resonator output level. The frequency content of the modulation noise n is related to the resonator output v by

$$N(\omega) = G^{-1}(j\omega)V(\omega) . \tag{10}$$

where $N(\omega)$ and $V(\omega)$ are the Fourier transforms of n and v, respectively. The feedback dithering modulator performs decorrelation by diminishing the resonator output and spectrally shaping the noise via G^{-1}. The deep null of G^{-1} near the signal frequency eliminates the correlated noise.

Example 1. Consider three-level modulation of a normalized 60-Hz reference signal $0.8\sin(2\pi 60t)$ for a full-bridge inverter. Two modulation schemes are considered. One is the sine-triangle PWM strategy [1, Ch. 4], the other the feedback dithering modulation scheme. The frequency of the triangular carrier for the sine-triangle PWM is 11 kHz. The feedback dithering modulation is simulated with the following design parameters

dither amplitude: $d = 0.55$;

$$\text{resonator: } G(s) = \frac{300s + 3000}{s^2 + (2\pi \times 60)^2} . \tag{11}$$

Both modulator outputs are sampled and held at the same rate of 60 kHz using a clocked comparator or quantizer. Figure 3 displays the power spectra of the three-level output waveforms. As expected, the feedback dithering modulation eliminates the noise near the 60Hz signal frequency, to achieve least correlated noise. Using the signal-to-noise-and-distortion ratio (SNDR) within 1 kHz as a performance measure, we have 27 dB and 39 dB of SNDR for the sine-triangle PWM and the feedback dithering modulation, respectively.

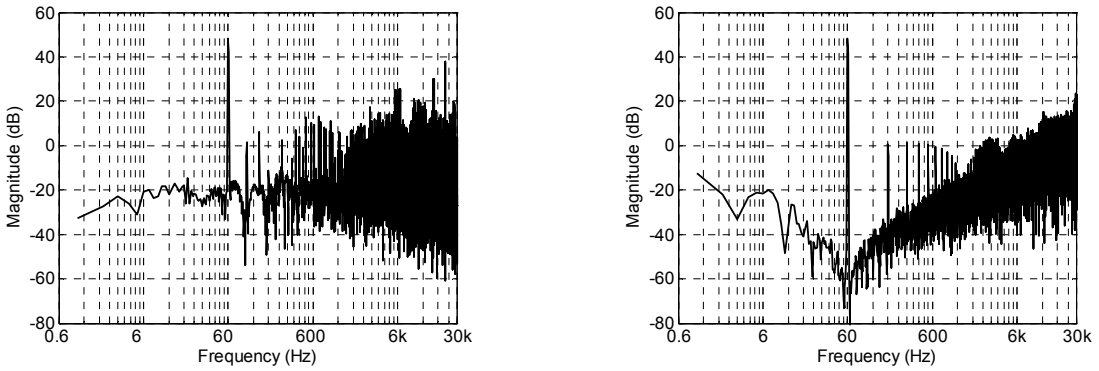

Fig. 3 Power spectra of three-level waveforms modulated by (a) sine-triangle PWM and (b) feedback dithering modulation

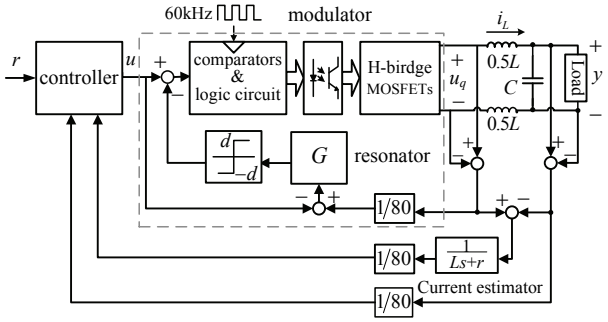

Fig. 4 Functional diagram of single-phase inverter

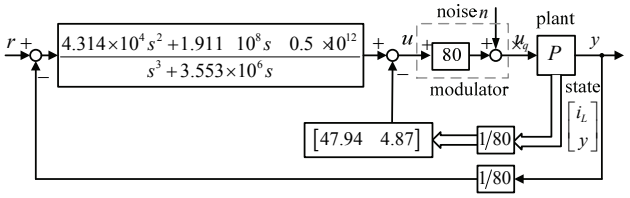

Fig. 5 LQR control system, in which a linear gain block and an additive uncorrelated noise source are used to model the modulator, and the plant models the LC-filter-plus-load dynamics

IV. Application: Single-Phase Inverter

The proposed feedback dithering modulation is applied to a single-phase voltage source inverter, intended to convert a 200V DC power to a 60Hz 110V AC power. Figure 4 shows the block diagram of the proposed design. It consists of three parts: a controller, a modulator and an LC filter plus load. The design strategy is to modulate the waveform with least correlated noise so that the modulator can be modeled as a linear gain added with a bounded uncorrelated noise, and the feedback controller can thus be designed and optimized using only linear feedback theory.

A. Modulator Design

The core of the inverter is the modulator, which consists of the feedback dithering circuit and a three-level clocked quantizer. The clocked quantizer is formed with a combined circuit of comparators AD8561, D-type flipflops TTL74F74, switching logic and dead-time circuit, optocouplers HCPL-3180 and predrivers IR2110, and a full bridge of power MOSFETs IRFP460, performing three-level quantization at a rate of 60 kHz and with the dead time of switching set to 1.6 μs. The dither amplitude and the resonator of feedback dithering are chosen the same as those in (11).

B. Controller Design

The controller is designed using the frequency-shaped linear quadratic regulator method [10]. The plant to be controlled is the dynamics from the switched waveform u_q to the output y, constituted by the output LC filter (L=2.5 mH and C=10 μF) and a load [11]. The plant is lowpass with a cutoff frequency roughly of 1 kHz. The modulator is modeled as a linear amplifier added with uncorrelated noise. The controller is optimized by minimizing the following quadratic cost functional with the additive uncorrelated modulation noise neglected.

$$\min_{U} \int_{-\infty}^{\infty} |W(j\omega)[Y(\omega)-R(\omega)]|^2 + |U(\omega)|^2 \, d\omega ,$$

where Y, R, and U are the Fourier transforms of output y, reference r, and unquantized control u, respectively. To attenuate low-frequency noise and eliminate the fifth harmonic at 300 Hz, the weighting function is chosen as

$$W(s) = \frac{0.5\times 10^{12}}{s[s^2 + (2\pi \times 300)^2]}$$

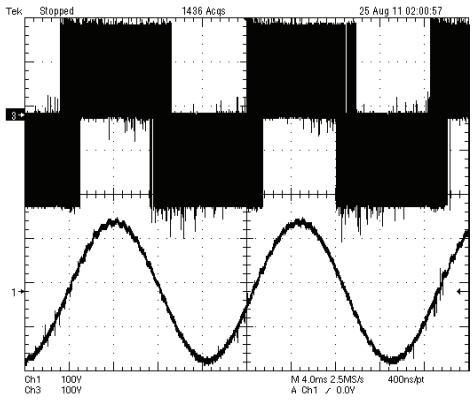

Fig. 6 Switched waveform u_q (above) and output waveform y (below)

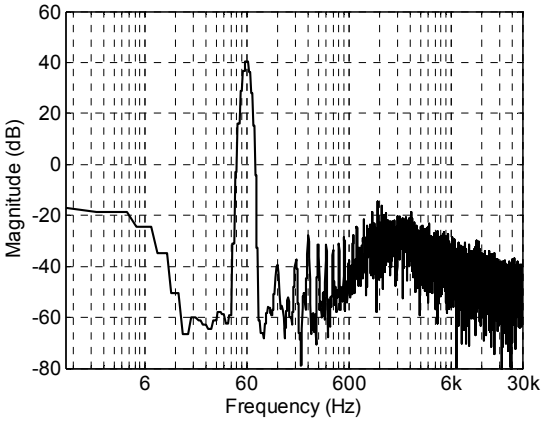

Fig. 7 Power spectrum of output waveform y

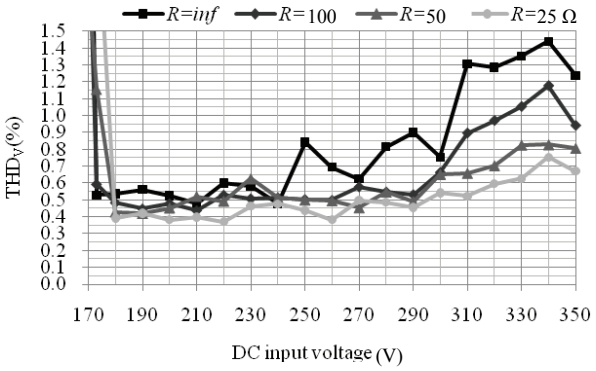

Fig. 8 THD versus DC input voltage graph for various resistive loads

The resulting optimal LQR control is shown in Fig. 5, formed by a linear combination of output feedback and state feedback. The control law is implemented in an analog RC op-amp circuit [12]. The state variables of the plant are the current through the inductor and the voltage across the capacitor. The inductor current is not directly measured; it is estimated by passing the voltage across the inductor through a lossy integrator that models the lossy inductance of the inductor [10], as shown in Fig. 4.

C. Performance Measurements

Figure 6 shows the oscilloscope measurement of the switched waveform u_q and the output waveform y of the inverter with a 200V DC input source and a resistive load of 25 Ω. The power spectrum of y is plotted in Fig. 7, which shows significant attenuation of noise and tones at low frequencies. A slight rise near DC is caused by the spectral leakage of a small DC offset present at the circuit. The achieved total harmonic distortion (THD) [1, Ch. 2] is 0.38%. For comparison, the proposed modulator is replaced by the sine-triangle PWM in Example 1 while the controller remains the same; in this case, the THD of the inverter is degraded to 1.5%.

To test the robustness, the inverter with the proposed design is measured under different DC input variations and load variations. Figure 8 summarizes the experimental results. It shows that, under the DC input variations from 180 to 300 V and the load variations from 25 to infinity Ω (or equivalently output power variations from 0 to 600 W), the inverter maintains a THD of less than 1%. The designed inverter has an excellent comparable performance to those of the reported inverters [2, 3].

V. Concluding Remarks

A feedback dithering modulation scheme is presented with emphasis to least correlated noise. Interestingly, the proposed modulation may be thought of as one kind of carrier-based modulation [1], by viewing the dither δ in Fig. 1 as a carrier signal. However, the major difference with the conventional carrier-based schemes is that the "carrier" is generated by the feedback of the modulation noise, rather than from an additional signal source. There are many potential advantages to generating a carrier in this manner, and the following two are most noteworthy and await further investigation.

1) *Feedback Elimination of unwanted noise and harmonics*: The modulation is capable of eliminating the modulation noise in a frequency band of interest. With proper design of feedback filter G, the modulator may attain least correlated noise and also wideband elimination of unwanted noise and harmonics.
2) *Compensation for dead time and other non-idealities*: Due to the feedback of the modulation noise, the modulator is capable of compensating for the imperfect switched waveform due to DC input variations, dead time, hysteresis, or other circuit non-idealities.

The further investigation and a more detailed comparison with the conventional PWM schemes, in terms of the above two properties, and other aspects, will be reported elsewhere.

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