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Modeling, Analysis and Simulation of 4-Phase Boost Converter

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***Abstract*—**This paper designs the four-phase Boost Converter which overcomes the problem of high input ripple current and output ripple voltage. Digital control is more convenient for such a topology on basis of synchronization, phase shift operation, etc. Simulation results are presented for open-loop and closed-loop for four phase boost converter. This control scheme is applicable for PFC rectifiers as well. Thus a comparative analysis based on the obtained results is performed.

***Keywords*—**Boost Converter, Bode plot, PI Controller, Four phase.

I. Introduction

BOOST DC-to-DC converters have very good source interface properties. The input inductor makes the source current smooth and hence these converters provide very good EMI performance. On account of this good property, the boost converter is also the preferred converter for off-line UPF rectifiers. One of the issues of concern in these converters is the large size of the storage capacitor on the dc link. The boost converter suffers from the disadvantage of discontinuous current injected to the load. The size of the capacitor is therefore large. Further, the ripple current in the capacitor is as much as the load current; hence the ESR specification of the tank capacitor is quite demanding. This is especially so in the emerging application areas of automotive power conversion, where the input voltage is low (typically 12V) and large voltage boost (4 to 5) are desired.

In the UPF rectifier applications, the input voltage varies from zero to maximum value twice in every cycle of the ac input voltage. The duty cycle therefore varies in the full range of zero to one. The inductor current varies from zero to rated current twice in every ac cycle of the input current. On account of these wide operating point variations, the design of the power circuit as well as the closed loop controller is a demanding task.

The poly-phase operation of boost converter to overcome the disadvantages of large size storage capacitor in boost converter and off-line UPF rectifiers and a small signal analysis of N converters in parallel to an equivalent second order system in such converters.

In designing DC converters, parameters such as ratio of energy stored in inductor and capacitor to energy delivered to load in one period, maximum current in the switch and the value of the RMS current in the output capacitor have great importance.

One-way of reducing the storage requirement is increasing the switching frequency however this is not practicable in all instances. During the on state of the switch, the capacitor has to supply the load current in the boost converter and this discontinuity of current in the capacitor increases the RMS value of current and also increases the amount of capacitor which is needed for correct operation of the circuit and therefore it results in more dissipation due to ESR of capacitor. In standard designs it is not uncommon to see tank capacitors one or two orders of magnitude higher than the ideally required capacitance A way to overcome this problem is using poly-phase operation with appropriate phase shift in the control circuit of main switches. This is done in such a way that at anytime one of the inductors is supplying the load current. The frequency of ripple current in the output capacitor is n times compared to the single stage and therefore the value of the capacitor required can be reduced. Extracting continuous current from the input for applications such as unity power factor is usually the reason for choosing boost converter configuration. An advantage of using poly-phase converter is in light load operation.

Digital control is more convenient for such a topology on account of the requirement of synchronization, phase shifted operation, current balancing etc. [1]. The operation and design trade-offs of the interleaved boost converter in continuous inductor-current mode in a high power factor pre regulator circuit. By using interleaved converters an overall reduction of boost inductor and EM1 filter volume can be achieved, together with reduced switching losses [2], [3]. Another converter family generated by connecting N-identical boost converters in parallel is presented. The proposed control uses interleaving techniques based on a binary state transition diagram [4]. Unity power factor boost converter with phase shifted parallel IGBT operation for medium power applications [5]. The impact of digital control in high-frequency switched-mode power supplies (SMPS), including point-of load and isolated DC-DC converters, microprocessor power supplies, power-factor-correction rectifiers, electronic ballasts, etc., where switching frequencies are typically in the hundreds of kilohertz to megahertz range [6]. Predictive digital current programmed control for valley, peak or average

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current. The control laws are derived for the three basic converters: buck, boost, and buck–boost [7]. A digital current mode control technique for dc-dc converters. It has been shown that we can implement anyone of the average, peak and valley current mode controls by adjustment of the sampling instant of the inductor current with respect to the turn on instant of the switch [8]. A new concept in the design of switched-mode power conversion circuitry is presented. Because of its extreme simplicity, flexibility, and efficiency it has the potential to replace some conventional electrical power processing methods currently in use [9]. A new current sharing method which is based on current mode controlled DC–DC converters and achieved the current sharing by forcing all inner current loops to have the same current reference. [10].

The parallel operation of voltage regulator modules (VRMs) for high-end microprocessors requires a current-sharing (CS) circuit to provide a uniform load distribution among the modules [11]. A boost converter was built and tested under the static and dynamic PFC operation condition as well as DC-DC operation condition [12]. A novel, zero-voltage switched (ZVS) PWM boost converter that combines soft-switching with constant frequency operation [13], [14]. A new family of ZVS-PWM Active-clamping DC-to-DC Boost converters is presented. The technique presents ZVS commutation without additional voltage stress and a significant increase in the circulating reactive energy throughout the converters so the efficiency and the power density become advantages when compared to the hard-switching boost converter [15], [23]. A circuit technique that reduces the boost-converter losses caused by the reverse recovery characteristics of the rectifier is presented. The losses are reduced by inserting an inductor in the series path of the boost switch and the rectifier to control the di/dt rate of the rectifier during its turn-off. The energy from the inductor after the boost switch turn-off is returned to the input or delivered to the output via an active snubber [16], [19]. K. Mark Smith et al. [17] have conducted a comparison study to characterize the loss mechanisms, component stresses, and overall efficiencies of a group of voltage-mode soft switching pulse width modulation (PWM) methods. They found that only those methods that softly switch the auxiliary switch minimize redirection current and recover the auxiliary circuit energy over most of the load range. An active snubber cell is to contrive zero voltage-transition (ZVT) pulse width-modulated (ZVT-PWM) converters. Except for the auxiliary switch, all active and passive Semi-conductor devices in a ZVTPWM converter operates at zero-voltage-switching (ZVS) turn on and turn off [18]. Tae-Woo Kim et al. [20] have proposed an Improved ZVT-PWM boost converter. The main switch of the conventional ZVT-PWM converter is always switched at zero voltage. But the auxiliary switch is turn-off with switching loss due to hard switching condition. The proposed converter is reducing the turn-off switching loss of the auxiliary switch by using additional circuit. A Zero-Voltage-Transition (ZVT) Boost converter using a soft switching auxiliary circuit is presented. The improvement over existing topologies lies in the structure and position of the auxiliary circuit capacitors and the subsequent reduction in the main switch resonant current [21]. Bo Feng et al. [22] have proposed a PFC converter employing compound active clamping technique. It can effectively reduce the loss caused by diode reverse recovery. The parasitic oscillation caused by the parasitic capacitance of the boost diode is eliminated. The maximum voltage stress of switches and the soft-switching region with relation to the resonant inductor and resonant capacitance are investigated.

A systematic development of a unified signal flow graph model for an interleaved boost converter with coupled inductor system operating in continuous current mode is presented. This signal flow graph approach provides a means to directly translate the switching converter to its graphic model, from which steady-state and dynamic behavior of the converter can be studied [24], [26].

An output ripples analysis of multiphase dc-dc converters that having an output LC filter and derived analytical expressions for the output voltage ripple of two- and three-phase dc-dc converters. Influence of the coupling coefficient of the output filter inductor on the output ripple is investigated. A comparative evaluation of single-phase, two-phase, and three-phase dc-dc converters is also presented [25].

A converter has been proposed which consists of two interleaved and inter-coupled boost converter cells. The boost converter cells have very good current sharing characteristics even in the presence of relatively large duty cycle mismatch. They designed it to have small input current ripple and zero boost-rectifier reverse-recovery loss. They also presented the operating principle, steady-state analysis, and comparison with the conventional boost converter. [27]

A new single-phase high power-factor rectifier, which features regulation by conventional pulse width modulation (PWM), soft commutation, and instantaneous average line current control is presented. A new zero-current switching PWM (ZCS-PWM) auxiliary circuit is configured in the presented ZCS-PWM rectifier to perform ZCS in the active switches and zero-voltage switching (ZVS) in the passive switches [28].

A digital current-mode controller for dc-dc converters has been introduced. The current-mode loop is sensor-less, relying on constants and internal loop states, removing the need to sense controlled voltages or currents for the inner loop. They also implemented a fast current-mode control mechanism by utilizing dead-beat control. [29]

Different digital control techniques, including predictive control and dead-beat control technique are compared. Advantages and disadvantages of each method are analyzed by them and their benefits to EVs/HEVs are investigated. They also discussed a predictive digital control method that works well in both continuous and discontinuous mode [30].

II. Mathematical Model of Boost Converter

A. Boost Converter

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

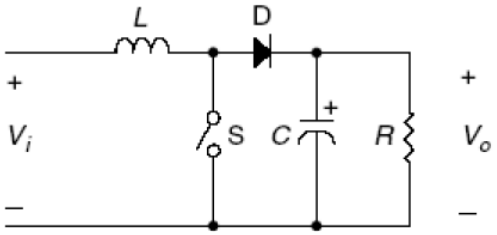

Fig. 1 Basic boost Converter

The circuit that models the basic operation of the boost converter is shown in Fig. 1. The input voltage in series with the inductor acts as a current source. The energy stored in the inductor builds up when the switch is closed. When the switch is opened, current continues to flow through the inductor to the load. Since the source and the discharging inductor are both providing energy with the switch open, the effect is to boost the voltage across the load. The load consists of a resistor in parallel with a filter capacitor. The capacitor voltage is larger than the input voltage. The capacitor is large to keep a constant output voltage and acts to reduce the ripple in the output voltage.

B. Need for Poly Phase Operation

In designing DC converters, parameters such as ratio of energy stored in inductor and capacitor to energy delivered to load in one period, maximum current in the switch and the value of the RMS current in the output capacitor have great importance and it is necessary to be considered.

One-way of reducing the storage requirement is increasing the switching frequency however this is not practicable in all instances. During the on state of the switch, the capacitor has to supply the entire load current in the boost converter; this discontinuity of current in the capacitor increases the RMS value of current and also increases the amount of capacitor which is needed to keep the ripple voltage low. The power dissipation in the ESR of the capacitor is also high. In standard designs it is not uncommon to see tank capacitors one or two orders of magnitude higher than the ideally required capacitance A way to overcome this problem is using poly-phase operation with appropriate phase shift in the control circuit of main switches.

C. Proposed Converter

Fig. 2 shows such a poly-phase boost converter (N=4). Table I shows the conduction intervals of the four switches in the converter. It is seen that at any time at least one of the converters is supplying the load in addition to the capacitor. The frequency of ripple current in the output capacitor is N times compared to the single stage and therefore the value of the capacitor required can be reduced. The same circuit topology is also applicable to UPF rectifiers.

In such a scheme, the following advantages are obvious. Output capacitor is rated for lower ripple current and higher ripple frequency.

- Source current has higher ripple and at higher frequency.
- Another no obvious advantage is that the poly-phase converter may be operated with less number of stages when the load current is low. This will lead to operation under CCM at light load as well as better efficiency.

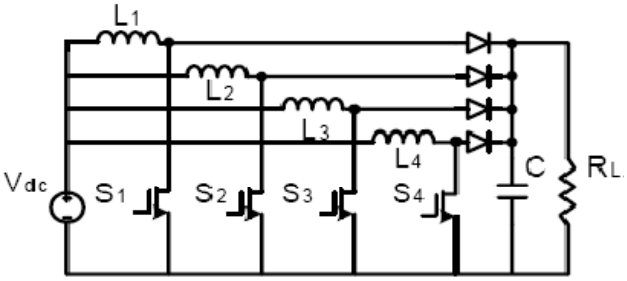

Fig. 2 Four-phase boost Converter

D. Average Model of the Converter

The converter alternates between the two-switched states at high frequency. We wish to represent the converter through a single equivalent dynamic representation, valid for both the ON and OFF durations. If we consider that the variation of the dynamic variables over a switching period, then

$$x = \dot{x_{avg}} T_s = \dot{x}_d T_s + \dot{x_{dTs}} dT_s + \dot{x_{(1-d)T_s}} (1-d) T_s \quad (1)$$

where, X_{avg} is the average rate of change of dynamic variables over a full switching period. The above equivalent description is valid if XdTs and X (1-d) Ts are constant during the ON and OFF duration respectively. This will be valid assumption if the ON and OFF durations are much less compared to the natural time constants of the respective circuits. For the averaged dynamic variables:

$$\dot{x_{avg}} = Ax + BV_g + eV_T + nV_D \quad (2)$$

The steady state solution is obtained by equating the rate of change of dynamic variables to zero. For the sake of simplicity, the converter is taken as ideal.

$$\dot{x} = Ax + BV_g \quad (3)$$

$$V_o = \frac{q}{x} \quad (4)$$

$$\dot{x} = \left(\frac{\frac{di_1}{dt}}{\frac{dV_c}{dt}} \right); q = [0\ 1] \quad (5)$$

$$A = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{-1}{RC} \end{bmatrix}; B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}; \quad (6)$$

The steady state solution is:

$$X = \frac{A^{-1}}{(\frac{B}{V_g})} \quad (7)$$

$$A^{-1} = \frac{LC}{(1-D)^2} \begin{bmatrix} \frac{-1}{RC} & -\frac{1-D}{L} \\ \frac{1-D}{C} & 0 \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} I_1 \\ V_0 \end{bmatrix} = \begin{bmatrix} \frac{V_g}{R(1-D)} \\ \frac{V_g}{1-D} \end{bmatrix} \quad (9)$$

E. Small Signal Model of the Converter

The steady state representation of the averaged system given by the above equations though linear is not time invariant. This is because the gain matrices A, b etc. is functions of time through 'd' embedded within. Therefore it is necessary to linearize the system equations.

Such a linearized model will enable us to define the different transfer functions for the converter and apply linear system theory to design closed loop controllers for the converters. We may neglect the terms containing VT and VD for this purpose. Such a step will be valid since these quantities are small (compared to Vg and Vo) and hence small variations in these small terms will only have a second order effect on the overall system. The dynamic equations are thus:

$$\dot{x} = [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]V_g \quad (10)$$

$$V_0 = [q_1 d + q_2(1-d)]x \quad (11)$$

Considering that the inputs d and vg are varying around their quiescent operating points D and Vg respectively.

$$d = D + \hat{d}; v_g = V_g + \widehat{v_g}; \quad (12)$$

These time varying inputs in d and vg produce perturbations in the dynamic variables x (X +$\hat{x}$) and vo (Vo +$\widehat{v_o}$).

$$X + \hat{x} = \left[A_1(D+\hat{d}) + \dot{A_2}(1-D-\hat{d})\right](X+\hat{x}) + [B_1(D+\hat{d}) + B_2(1-D-\hat{d})(V_g + \widehat{v_g}) \quad (13)$$

$$V_o + \widehat{v_o} = \left[q_1(D+\hat{d}) + q_2(1-D-\hat{d})\right](X+\hat{x}) \quad (14)$$

The above equations may be expanded and separated into dc (steady state) terms, linear small signal terms and non-linear terms. When the perturbations in d and Vg are small, the effect of the non-linear terms will be small on the overall response and hence may be neglected.

The small signal dynamic model of the converter is obtained as:

$$\hat{x} = A\hat{x} + B\widehat{V_g} + f\hat{d} \quad (15)$$

$$V_o = q\hat{x} + (q_1 - q_2)X\hat{d} \quad (16)$$

$$A = A_1 d + A_2(1-D); B = B_1 D + B_2(1-D); \quad (17)$$

$$q = q_1 D + q_2(1-D) \quad (18)$$

$$f = [(A_1 - A_2)X + (B_1 - B_2)V_g] \quad (19)$$

F. Transfer Function of the Boost Converter

Various Transfer Function of Boost Converter that can be obtained are:

$$\frac{\hat{I}(s)}{\widehat{v_g}(s)} = \frac{1}{R(1-D)^2} \frac{1+sCR}{[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}]} \quad (20)$$

$$\frac{\hat{I}(s)}{\hat{d}(s)} = \frac{V_g}{R(1-D)^3} \frac{2+sCR}{[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}]} \quad (21)$$

$$\frac{\widehat{v_o}(s)}{\widehat{v_g}(s)} = \frac{1}{(1-D)} \frac{1+sCR}{[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}]} \quad (22)$$

$$\frac{\widehat{v_g}(s)}{\hat{d}(s)} = \frac{V_g}{(1-D)^2} \frac{1+sCR}{[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}]} \quad (23)$$

III. Digital Control of 4-Phase Boost Converter

A. 4-phase Operation

In poly-phase boost converter each stage has an independent current mode control loop, which uses the same reference current. The reference current in turn is generated by the outer voltage control loop. For correct operation of poly-phase boost converter each PWM gate signal is required to have 90 degrees phase shift respect to the previous one. In order to generate these signals a synchronization circuit is needed. Though practicable, the analog realization leads to certain limitations.

Fig. 3 shows the architecture of digital control, which has been used here for the 4-phase boost converter. A PI controller based on the error signal from the outer voltage loop builds the reference current. The inductor current in each of the converters or a representative sample of the inductor currents is compared with current reference.

Accordingly the individual duty ratios or a single common duty ratio is imposed in the switches.

It is obvious that in digital implementation modularity of the system is preserved.

Adding extra stages or changing the switching frequency needs only a modification in the software.

Generation of the four phase shifted PWM signals can be done in two ways.

Method A: Programming general purpose timers with period of switching frequency and initializing four different counter registers with 0, 90, 180, 270 degrees phase shift respect to the timer period register.

Method B: The switching pattern of different switches for different values of duty cycles which is stored as lookup table in memory has been shown in Table I. On time duration of the switch is determined by D′ and similarly (1-D′) determines the off time duration where, D′ is given by D′=ND−floor (ND)

Then PWM signals can be generated on general-purpose input output pins.

The different possibilities of ON and OFF situations of switches for 4-phase Boost Converter is shown in Table I.

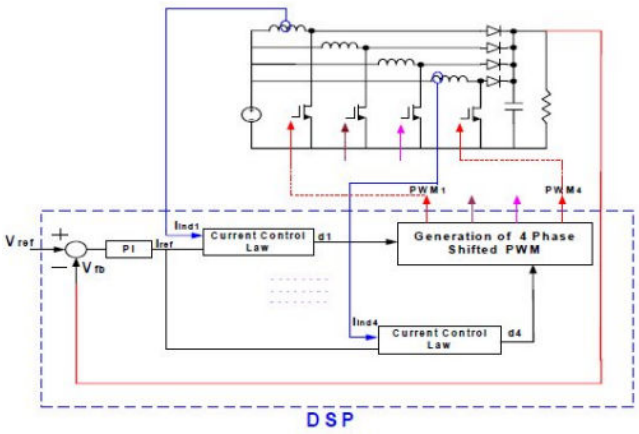

Fig. 3 Digital Circuit Realization of the 4-phase Boost

B. Digital Current Control Law

The required duty ratio for the next switching cycle is predicted based on the sample current and the input and output voltages but not the previous duty ratio as shown in Table I. Fig. 4 shows the inductor current waveform. The sampled inductor current I (n) at time nTs can be expressed as a function of the previous sampled value I (n-1) and the applied duty ratio d(n).

$$i(n) = i(n-1) + \frac{V_{in}[n]T_s}{L} + \frac{(V_{in}-V_o)d'[n]T_s}{L} \quad (24)$$

By using $d' = 1-d$ if we solve the above equation for predicted duty cycle

$$d[n] = \frac{L}{V_o T_s}(i_c - i_s[n-1] + 1 - \frac{V_{in}}{V_o}) \quad (25)$$

where ic=is[n]

It means in each cycle the inductor current follows the reference ic and try to make the difference zero such that in steady state

$$d[n] = 1 - \frac{V_{in}}{V_o} \quad (26)$$

This method is simple and has good results. In the second method all the currents are sampled such that each stage has an independent current control loop so different duty cycle values, which are almost same, can be found and will be applied to corresponding compare registers. If some slight differences are observed which may cause difference in current sharing of parallel stages it can be rectified through adjusting the parameters because we have independent closed loop controls. Similarly by finding the average of different duty cycles, the error may be applied to force the current sharing.

Now it is obvious that single sampling has the advantage of simplicity and consequently it is more suitable for higher switching frequency because only one current is sampled and is processed in fewer amount of time. This method is good if the component values (for example the inductor values in different stages) are almost equal such that no significance difference in current sharing is observed.

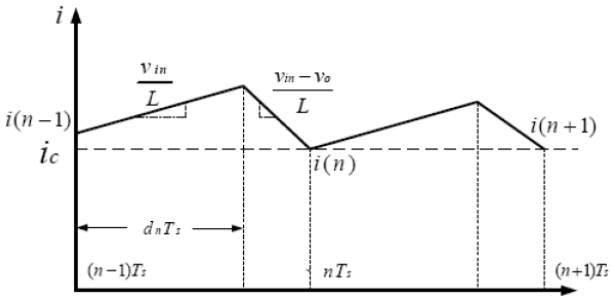

Fig. 4 Inductor Current Waveform under Valley Current Control

It is essential to note that some techniques, which have been explained here, like adjusting the parameters in each control loop and applying the average duty value, can only be achieved in digital control implementation. Another technique, which does not exist in analog implementation, is turning off of some of the converters at light load operation, which cause DCM operation of the converter. According to the level of load current, one, two or three of the converters may be switched of and in this case generation of the phase shifted PWM may change. For example for four converters in parallel one can turn off two or three of the stages without even changing the generation of phase shifted PWM signals. Of course for turning off of one stage or any other numbers in general in N converters in parallel the required amount of phase shift varies and it can be predetermined and stored in memory.

IV. Design of PI Controller

A. Converter Parameters

Po = 35 W
Vin = 12 V
Vo = 32 V
Fs = 100 KHz
D = 1-Vin/Vo = 0.625
ΔIin = 0.2(20%)
ΔVo = 0.01(1%)
R = Vo*Vo/Po = 29.257 Ω
L = (Vin*D*Ts)/ΔIin = 128.5714μH
C = (D*Ts*Vo)/(R*ΔVo) =21.3623μF

B. MATLAB Program for Bode Plot of Boost Converter

```
Vi=12;
Vo=32;
Po=35;
Fs=100e3;
deli=0.2;
delv=0.01;
D=1-Vi/Vo;
```

```
Ts=1/Fs;
R=Vo^2/Po;
L=D*(1-D)^2*R*Ts/deli;
C=D*Ts/(R*delv);
num=[1/(1-D)];
den=[L*C/(1-D)^2 L/(R*(1-D)^2) 1];
H=tf(num,den);
bode(num,den);
grid on;
```

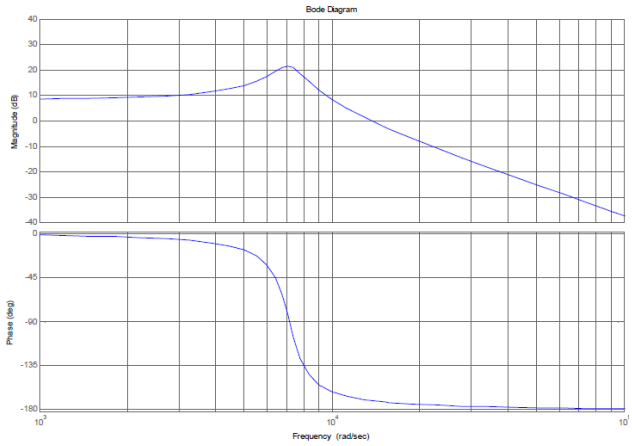

Fig. 5 Bode Plot of Boost Converter

Values of Ki and Kp can be calculated from bode plot

$$K_p = \frac{cos\theta}{A} \quad (27)$$

$$K_i = -\frac{\omega sin\theta}{A} \quad (28)$$

$$\theta = \gamma_d - \gamma_u \quad (29)$$

where γ_d is called Desired Phase Margin; γ_u is called Phase Margin of Uncompensated System

V. Simulink Circuits

Single phase Boost Converter and Four-phase Boost Converter are simulated both in Open as well as Closed Loop Configurations using MATLAB/SIMULINK.

Waveforms for Output Voltage, Output Voltage Ripple, Input Current, Input Current Ripple, Capacitor Current and Steady State Capacitor Current are obtained both for Single Phase and Four Phase Boost Converter (Open Loop and Closed Loop Configurations).

Simulink model of Single phase Boost Converter in Open Loop Configuration is shown in Fig. 6

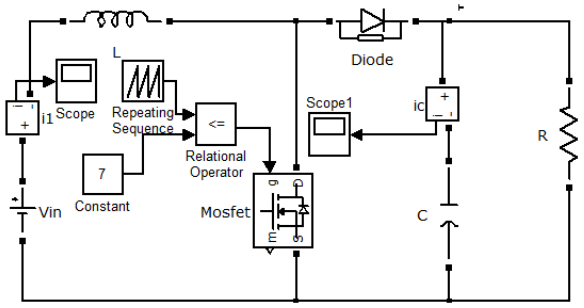

Fig. 6 Simulink Model for Single Phase Boost Converter (open loop)

Simulink model of Four-phase Boost Converter in Open Loop Configuration is shown in Fig. 7.

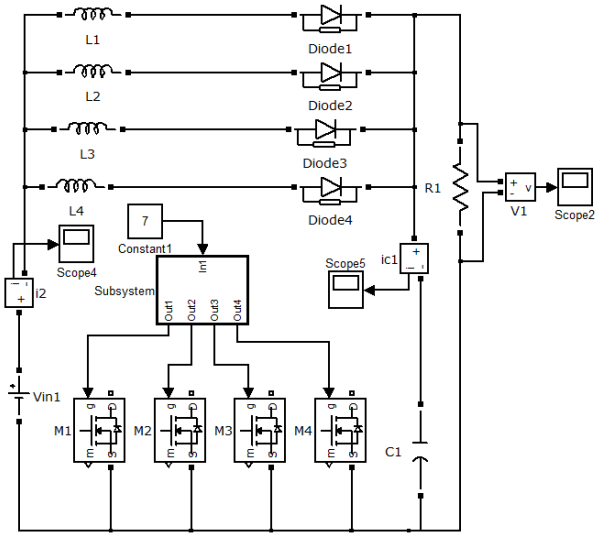

Fig. 7 Simulink Model for Four Phase Boost Converter (open loop)

Simulink model of Generation of Four-phase Shifted Pulse is shown is Fig. 8.

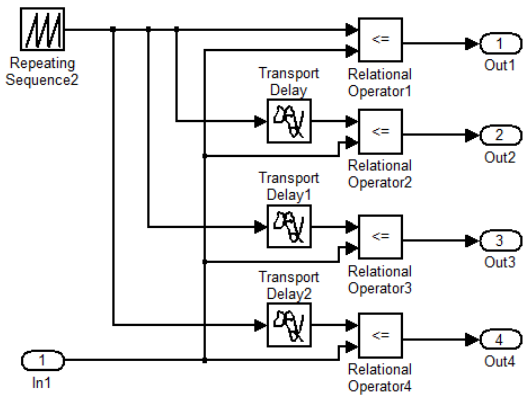

Fig. 8 Generation of Four Phase Shifted Pulses using Simulink

Simulink Model of Single Phase Boost Converter for Closed Loop Configuration is shown in Fig. 9

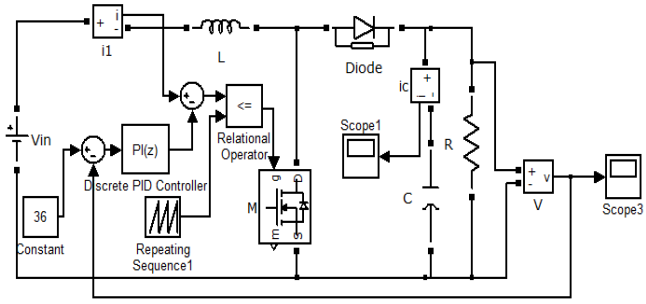

Fig. 9 Simulink Model for Single Phase Boost Converter (Closed Loop)

Simulink Model of Four Phase Boost Converter for Closed Loop Configuration is shown in Fig. 10.

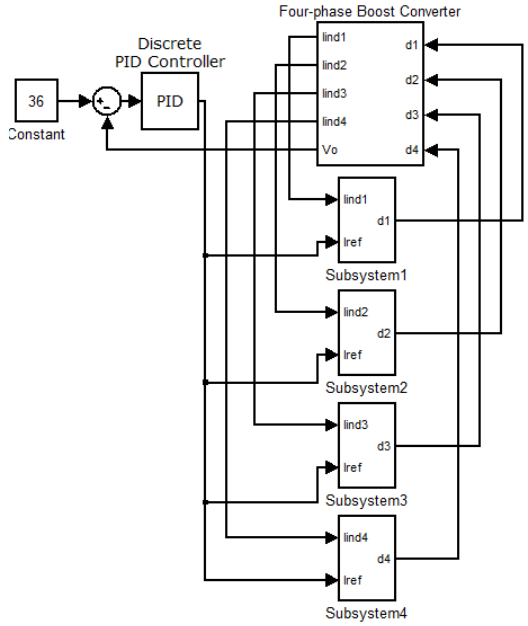

Fig. 10 Simulink Model for Four Phase Boost Converter (Closed loop)

Simulink Model of Subsystem 1 to Subsystem 4 is shown below.

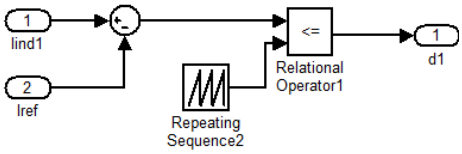

Fig. 11 Simulink Model of Subsystem1

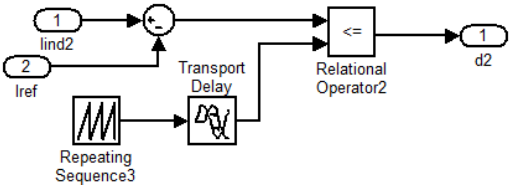

Fig. 12 Simulink Model of Subsystem2

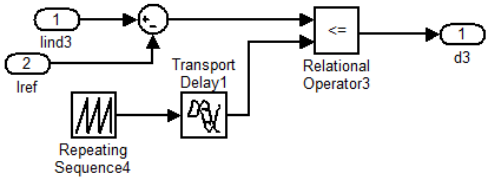

Fig. 13 Simulink Model of Subsystem3

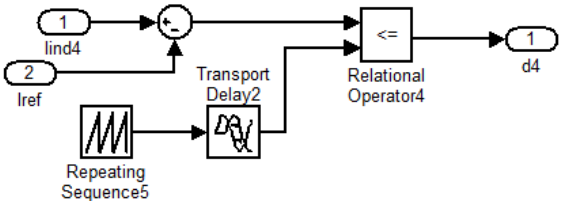

Fig. 14 Simulink Model of Subsystem4

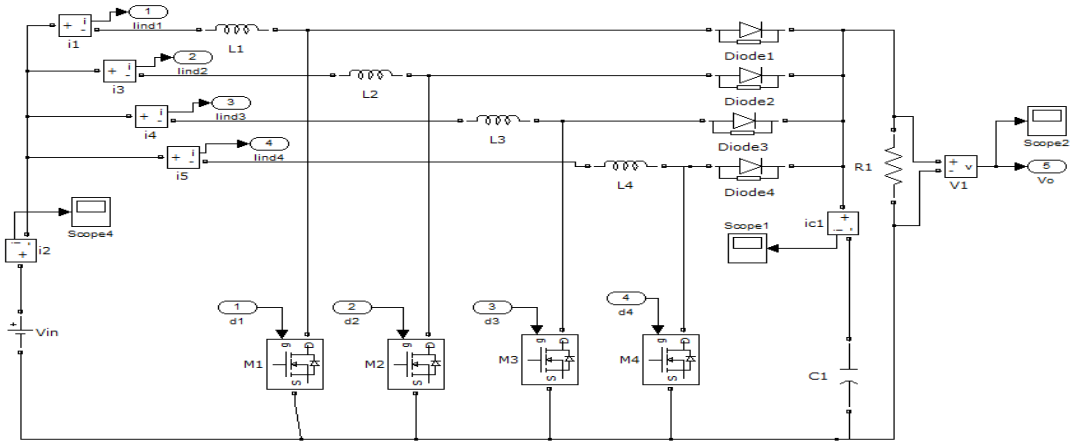

Fig. 15 Subsystem of 4-phase Boost Converter

Simulink Model of Sub system of Four-phase Boost Converter is shown in Fig. 15.

Comparison of Output Voltage Ripple for Single phase and Four-phase Converters in Open Loop Configuration is shown in Figs. 16 and 17.

Comparison of Input Current Ripple for Single phase and Four-phase Converters in Open Loop Configuration is shown in Figs. 18 and 19.

Comparison of Output Voltage Ripple for Single phase and Four-phase Converters in Closed Loop Configuration is shown in Figs. 20 and 21.

Comparison of Input Current Ripple for Single phase and Four-phase Converters in Closed Loop Configuration is shown in Figs. 22 and 23.

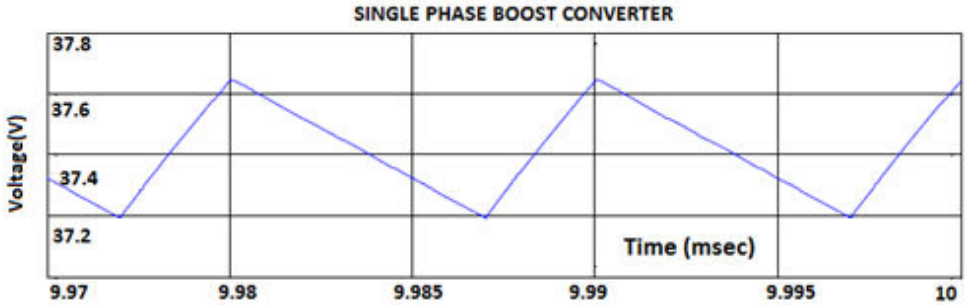

Fig. 16 Simulink Model for Single Phase Boost Converter (open loop)

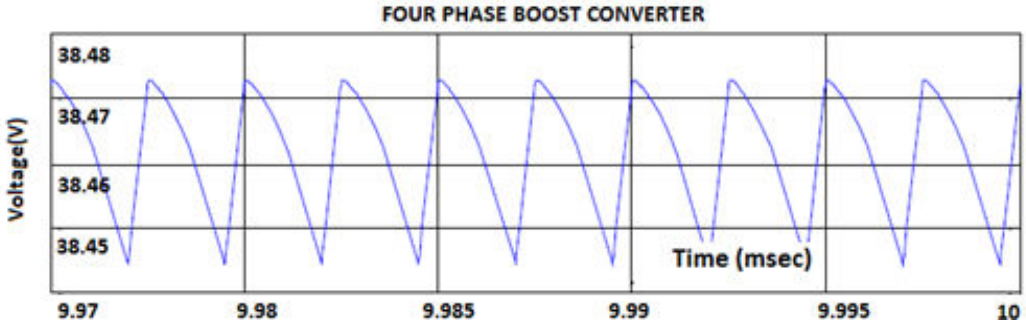

Fig. 17 Simulink Model for Four Phase Boost Converter (open loop)

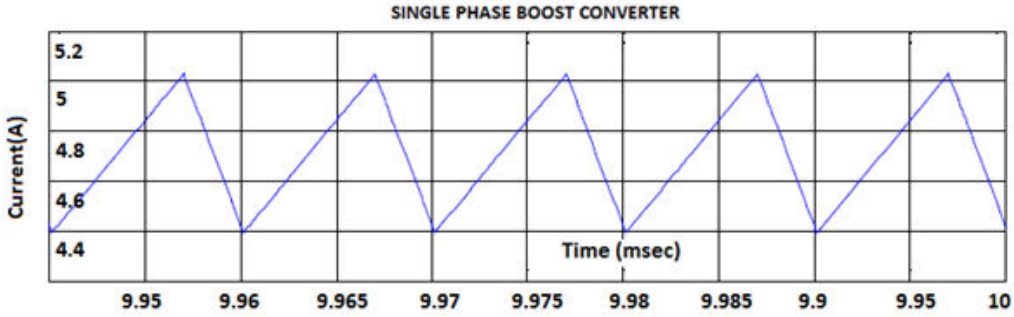

Fig. 18 Simulink Model for Single Phase Boost Converter (open loop)

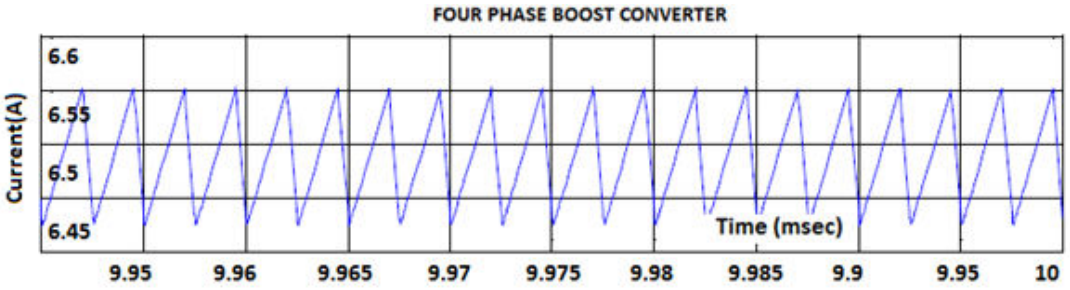

Fig 19 Simulink Model for Four Phase Boost Converter (open loop)

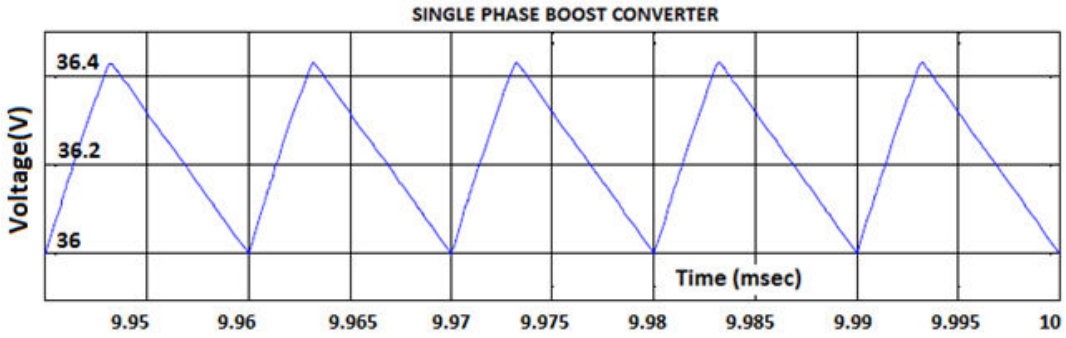

Fig. 20 Simulink Model for Single Phase Boost Converter (open loop)

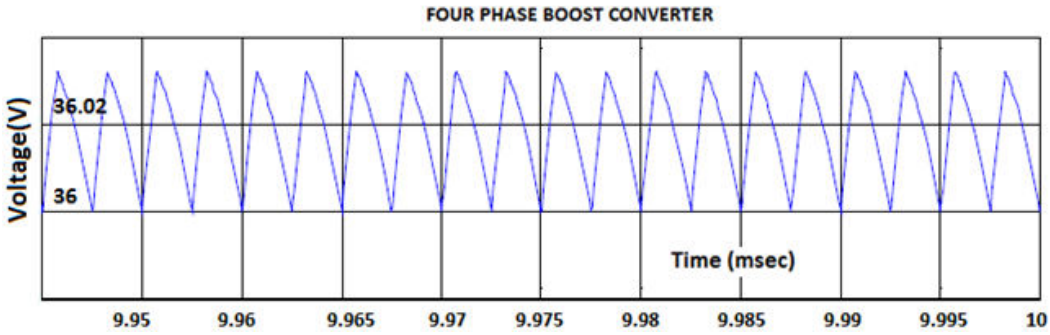

Fig. 21 Simulink Model for Four Phase Boost Converter (open loop)

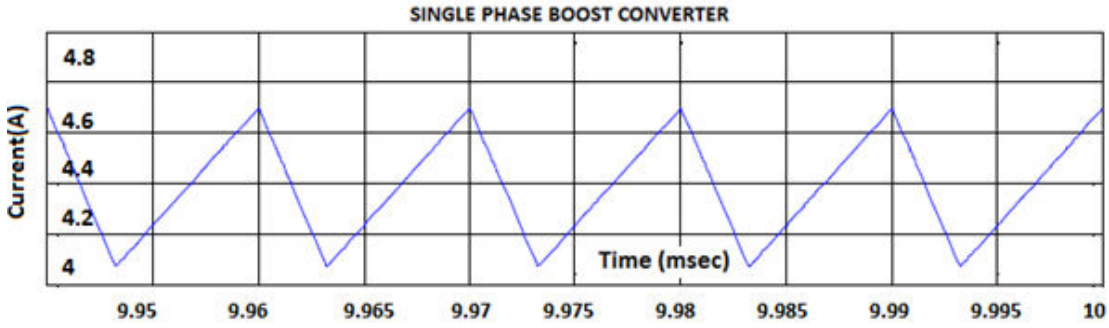

Fig. 22 Simulink Model for Single Phase Boost Converter (Closed loop)

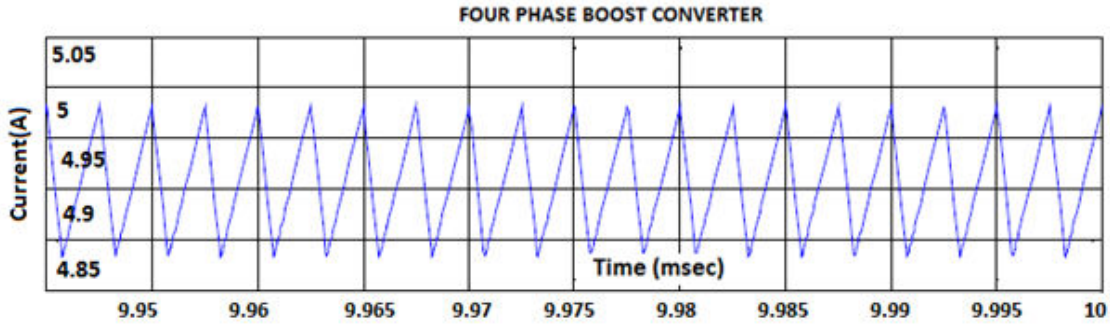

Fig. 23 Simulink Model for Four Phase Boost Converter (Closed loop)

TABLE I
DIFFERENT POSSIBILITIES OF ON & OFF SITUATIONS OF SWITCHES

Intervals	Switch	0≤D≤1/4	1/4≤D≤1/2	1/2≤D≤3/4	3/4≤D≤1
$0\leq t\leq T_S/4$	ON	1000	1001	1011	1111
	OFF	0000	1000	1001	1011
$Ts/4\leq t\leq T_S/2$	ON	0100	1100	1101	1111
	OFF	0000	0100	1100	1101
$Ts/2\leq t\leq 3T_S/4$	ON	0010	0110	1110	1111
	OFF	0000	0010	0110	1110
$3Ts/4\leq t\leq T_S$	ON	0001	0011	0111	1111
	OFF	0000	0001	0011	0111

VI. CONCLUSION

A modified method for determining the duty cycle corresponds to current control has been developed. The size of Four-boost converters in parallel is almost same as a single boost converter of the same total power because the size of main parts-inductors-almost remains same. Smaller RMS current in the energy-storage capacitor, lower input ripple current and lower output ripple voltage or smaller size of the tank capacitor are those important points, which have been considered.

Moreover digital realization in control results in better performance and advantages, which cannot be achieved by Analog method. Programmability, modularity and flexibility in design and different operating conditions are major points, which have been addressed.

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