

Micropower Fuzzy Linguistic-Hedges Circuit in Current-Mode Approach

E. Farshidi

Abstract—In this paper, based on a novel synthesis, a set of new simplified circuit design to implement the linguistic-hedge operations for adjusting the fuzzy membership function set is presented. The circuits work in current-mode and employ floating-gate MOS (FG-MOS) transistors that operate in weak inversion region. Compared to the other proposed circuits, these circuits feature severe reduction of the elements number, low supply voltage (0.7V), low power consumption (<200nW), immunity from body effect and wide input dynamic range (>60dB). In this paper, a set of fuzzy linguistic hedge circuits, including *absolutely*, *very*, *much more*, *more*, *plus minus*, *more or less* and *slightly*, has been implemented in 0.18 mm CMOS process. Simulation results by Hspice confirm the validity of the proposed design technique and show high performance of the circuits.

Keywords—Current-mode, Linguistic-Hedge, Fuzzy Logic, low power

I. INTRODUCTION

FUZZY logic generalized from the theory of fuzzy set originated by Zadeh [1]. It has been successfully applied in fuzzy logic controller (FLC) by Mamdani [2] to solve the various control problems [3], pattern recognition [4-8] and expert systems [9, 10]. Hardware realization of FLC (fuzzy chips) has been widely employed in a variety of disciplines such as control systems and image recognition. In an FLC, the inference engine plays role of a kernel. To accomplish better results of accuracy at the inference, a great number of fuzzy rules are needed, but the greater number of fuzzy rules leads to the greater hardware [11]. To solve this problem, linguistic-hedge set has been proposed [11], which results low hardware, high accuracy and dynamically modifying the shape of membership functions [12, 13]. Zadeh [11] proposed the fuzzy linguistic hedges to modify the membership function of the fuzzy set. Fuzzy linguistic labels are mainly used to represent the relationship of a fuzzy set with respect to one linguistic variable, such as, young in age, hot in temperature. The linguistic hedges are fuzzy operations used to modify the membership function of the fuzzy set so that the fuzzy set, for instance, very hot or more or less hot can be generated. In addition, the concept of extended hedge algebras and their application in approximate reasoning was discussed by Ho [14]. In principle, the essential part of the fuzzy logic controller is a set of linguistic control rules with the concepts

of fuzzy implication and the compositional rule of inference. Following this technique some current-mode circuit designs in the mixed-signal circuit design approach were proposed [12, 13, 15]. In these proposals, each separate linguistic-hedge operation has been performed by geometric-mean and squarer-divider functions. For design of these functions stacked or up-down translinear loops have been employed [12, 13, 15]. The main drawbacks of these proposed circuits are as follows: firstly, the extra needed functions for each linguistic-hedge operation lead to a large number of transistors and high power consumption; secondly, in these circuits, the MOS transistors are operating in strong inversion, thus employing low supply voltage restricts dynamic range [16]; and finally, in the circuit of stacked translinear MOSFET loops, the body effect decrease the accuracy [16]. Compared to the stacked loop, the influence of body effect in up-down translinear loop is smaller but circuit complexity of up-down translinear loop is higher and biasing current and voltage is needed [16].

In this paper, a new design to overcome the above problems is presented [17]. Using a novel synthesis, the circuits of linguistic-hedge operations employing the I-V relationship of the FG-MOS transistors by a simplified function is presented. In the presented synthesis, each linguistic-hedge operation will be implemented by one FG-MOS and two MOS transistors. Therefore, the circuit complexity for each operation is much less than those reported before [12, 13, 15]. In these circuits, the source of transistors is connected to the substrate; therefore, the proposed circuits are immune to the body effect. Also due the fact that the transistors are operating in weak inversion, the proposed circuits feature low-power, low-voltage and wide dynamic range. The fuzzy linguistic hedge circuits, including *absolutely*, *very*, *much more*, *more*, *plus minus*, *more or less*, and *slightly* have been implemented in 0.18 mm CMOS process and simulated. With the proposed hedge circuits and fuzzication unit [18], multi-input maximum/minimum circuit [19], and defuzzification unit [20], a real-time signal processing adaptive fuzzy logic controller based on linguistic hedge can be developed to modify the membership function.

The paper is organized as follows. In section 2 the basic concept of fuzzy linguistic-hedges is presented. Section 3 explains principle of current-mode linguistic-hedges. In section 4 the proposed circuit design for linguistic-hedge operations is discussed. Simulation results are presented and discussed in section 5 and concluding remarks are provided in section 6.

E. Farshidi is with the Electrical Engineering Department, University of Shahid Chamran, Ahvaz, Iran, 61357-8313 (e-mail: farshidi@scu.ac.ir).

II. BASIC CONCEPTS

A. Fuzzy Sets

Basically, the fuzzy set theory employs the membership function to interpret uncertain situations and imprecise information. A fuzzy set, which uses vague boundaries to distinguish members of a given set from nonmembers, is a generalization of a crisp set. A fuzzy set A of a universe of discourse X is characterized by a membership function μ_A , i.e.

$$\mu_A(x): X \rightarrow [0, 1] \tag{1}$$

where each element x of X has a number $\mu_A(x)$ in the interval $[0, 1]$, and $\mu_A(x)$ represents the grade of membership of x in A .

In general, a fuzzy set A may be represented as:

$$A = \frac{\mu_1}{x_1} + \frac{\mu_2}{x_2} + \dots + \frac{\mu_n}{x_n} \tag{2}$$

in which μ_i ($i = \{1, 2, \dots, n\}$) is the grade of membership of x_i in A . It should be noted the + sign in (2) denotes the arithmetic sum [1].

B. Fuzzy Linguistic Hedges

In fuzzy set theory, the information can be described linguistically. Fuzzy linguistic-hedge operations are used to represent the relationship of a fuzzy set with respect to one linguistic variable, such as, young in age; hot in temperature [11]. The linguistic-hedges are fuzzy operations to shape the membership function of the fuzzy set. Dilation intensification type and Concentration type are two main categories of linguistic-hedge operations.

1) *Dilation*: Applying a dilation operation to a fuzzy set A results in the increasing in the magnitude of the grade of membership of x in A , which is relatively small for those x with a high grade of membership in A and relatively large for those x with low membership. The hedge operation of “dilation” defined by Zadeh is [11]:

$$DIL(x) \equiv x^\alpha \quad \alpha < 1 \tag{3}$$

in which, α is rational power of the dilation operation. Some relative hedge operations such as minus, more or less, and slightly can be defined as follow:

$$minus \quad x = x^{0.75} \tag{4}$$

$$more \ or \ less \quad x = x^{0.5} \tag{5}$$

$$slightly \quad x = x^{0.25} \tag{6}$$

2) *Concentration*: the effect of concentration is opposite to that of dilation. The hedge operation of “concentration” defined by Zadeh is [11]:

$$CON(x) \equiv x^\alpha \quad \alpha > 1 \tag{7}$$

in which, α is rational power of the concentration operation. Similarly, a few relative hedge operations such as absolutely, very, much more, more, and plus can be defined as follow:

$$absolutely \quad x = x^4 \tag{8}$$

$$very \quad x = x^2 \tag{9}$$

$$much \ more \quad x = x^{1.75} \tag{10}$$

$$more \quad x = x^{1.5} \tag{11}$$

$$plus \quad x = x^{1.25} \tag{12}$$

C. Fuzzy Logic Controller

In fuzzy logic theory, human expert experience or know-how knowledge, represented as IF-THEN rules, is used to construct the fuzzy control system. So far, the fuzzy logic controller is the most successful application field for fuzzy logic. Primarily, a fuzzy logic controller consists of a fuzzifier module, a fuzzy inference engine, a knowledge base, and a defuzzifier module as shown in Fig. 1. The fuzzifier module is used to translate the input signal into the fuzzy representation, and the defuzzifier module is used to translate the inferential fuzzy results into crisp result to the output.

The fuzzy production rules, whose conditions of the antecedent and the conclusion are represented by linguistic variables, are mainly used to represent the decision-making procedure in knowledge base. The expert knowledge is usually expressed as:

$$\begin{aligned} & \text{IF (a set of conditions are satisfied) THEN} \\ & \text{(a set of consequences can be inferred).} \end{aligned} \tag{13}$$

The antecedent and the consequence of these IF-THEN rules have something to do with the fuzzy linguistic terms, so they are often referred to as fuzzy conditional statements. In this terminology, a fuzzy control rule is a fuzzy conditional

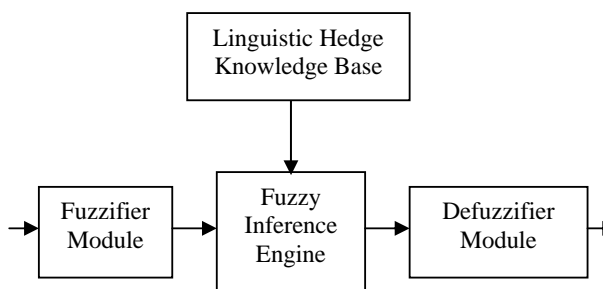


Fig. 1 The block diagram of the fuzzy logic controller

statement, where the antecedent is a condition in its

application domain and the consequence is a control action for the system under control. Above all, the fuzzy control rule provides a convenient way for expressing control policy and domain knowledge. Furthermore, several linguistic variables may be included in the antecedents and the conclusions of these rules at the same time. Consider a multivariable fuzzy control system with three inputs and three outputs. The linguistic description of the system control rules can be expressed as [12]:

$$\begin{aligned}
 & \text{IF } X_{1(i)} \text{ and } X_{2(i)} \text{ and } X_{3(i)} \text{ THEN } Y_{1(i)} \text{ and } Y_{2(i)} \text{ and } Y_{3(i)} \\
 & \quad \text{or} \\
 & \quad \vdots \\
 & \text{IF } X_{1(i)} \text{ and } X_{2(i)} \text{ and } X_{3(i)} \text{ THEN } Y_{1(i)} \text{ and } Y_{2(i)} \text{ and } Y_{3(i)} \\
 & \quad \text{or} \\
 & \quad \vdots \\
 & \text{IF } X_{1(n)} \text{ and } X_{2(n)} \text{ and } X_{3(n)} \text{ THEN } Y_{1(n)} \text{ and } Y_{2(n)} \text{ and } Y_{3(n)}
 \end{aligned} \tag{14}$$

where $X_{\kappa(i)}$ is the fuzzy value of the κ -th input variable defined in the universe of discourse U^k , $k \in \{1,2,3\}$ and $Y_{j(i)}$ is the fuzzy values of the j -th output variable defined in the universe of discourse W^j ($j \in \{1,2,3\}$).

Assume that the outputs depend only on the inputs and linguistic description of the control rules can be rewritten as [12]:

$$\begin{aligned}
 & \text{IF } X_{1(i)} \text{ and } X_{2(i)} \text{ and } X_{3(i)} \text{ THEN } Y_{j(i)} \\
 & \quad \text{or} \\
 & \quad \vdots \\
 & \text{IF } X_{1(i)} \text{ and } X_{2(i)} \text{ and } X_{3(i)} \text{ THEN } Y_{j(i)} \\
 & \quad \text{or} \\
 & \quad \vdots \\
 & \text{IF } X_{1(n)} \text{ and } X_{2(n)} \text{ and } X_{3(n)} \text{ THEN } Y_{j(n)}
 \end{aligned} \tag{15}$$

where $j \in \{1,2,3\}$. The three-input three-output system can be decomposed into three three-input one output systems. Regarding the three-input one-output system, the fuzzy relation of this system defined by Zadeh [1] can be expressed as:

$$R_1 = \max_{u^1 u^2 u^3 w} [\min(X_1, X_2, X_3, Y_1)] \tag{16}$$

If the present inputs are X_1, X_2 , and X_3 , then the present output Y_1 can be determined by the compositional rule of inference [1]:

$$Y_1 = (X_1, X_2, X_3) \circ R_1 \tag{17}$$

III. CURRENT-MODE FUZZY LINGUISTIC-HEDGES

In mathematical model, the grade value of the membership function is defined within [0, 1]. By rearranging the definition of the function in order to hardware implementation of the hedge circuits, each linguistic label in this work is represented by a continuous current signal within [0nA, 100nA] to indicate the degree of membership belonging to the corresponding fuzzy sets in the universe of discourse. Also, the membership degree of the fuzzy set modified by the linguistic-hedge has to be maintained within [0nA, 100nA]. According to reference [21], the current signal representation of the linguistic-hedge is:

$$I_{\mu^\alpha}(x) = I_\mu^\alpha \cdot I_H^{1-\alpha} \tag{18}$$

where I_μ and I_{μ^α} are current-signal representation of the membership value μ with respect to the fuzzy set x and the linguistic-hedge operator μ^α , respectively. Also, I_H is used to normalize the operation result within the range of logic "1". For implementation of the linguistic-hedge operations, the I-V relationship of FG-MOS transistors that operate in weak inversion [21] are employed. A FG-MOS transistor with N input voltages consists of a floating gate electrode extended over the channel and N input gates located over the floating gate. In other words, the FG-MOS transistor is a MOS transistor with an isolated gate that capacitively coupled to the inputs. Fig. 2 shows the symbol diagram and equivalent circuit of the transistor with 2 input voltages. The drain current of a N-type FG-MOS transistor in weak inversion region is given by [21]:

$$I_d = I_s \exp\left(\frac{V_{FG}}{nU_T}\right) \tag{19}$$

where U_T stands for the thermal potential, I_s is a device dependent coefficient, n represents the subthreshold slope and V_{FG} is voltage of floating gate electrode

Applying charge conservation law, the voltage at the floating gate with 2 equal input capacitances, which is used in this work, is obtained by:

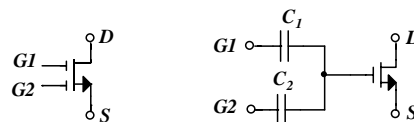


Fig. 2 Symbol diagram (left) and equivalent circuit of FG-MOS (right)

$$V_{FG} = w_1 V_1 + w_2 V_2 + \frac{C_{gd}}{C_t} V_{gd} + \frac{C_{gs}}{C_t} V_{gs} + \frac{C_{gb}}{C_t} V_{gb} + \frac{Q_{fg}}{C_t} \quad (20)$$

V_i is the i -th input gate voltage ($i \in \{1, 2\}$), C_t is the sum of capacitors that are connected to the floating-gate, C_{gd} , C_{gs} , C_{gb} are the parasitic capacitors between the floating gate and the drain, source and bulk, respectively, Q_{fg} is residual charge trapped at the floating gate during fabrication process (This latter charge can be made negligible by using the technique described in [22]) and w_i is input capacitance ratio of i -th input gate, and is defined as:

$$w_i = \frac{C_i}{C_t} \quad (21)$$

in which C_i is the input capacitance between the floating gate and the i -th input gate. From (21) it is evident that the value of input capacitance ratios is equal or smaller than one ($w_i \leq 1$). If the sum of input capacitances is chosen much larger than parasitic capacitances, i.e.,

$$C_1 + C_2 \gg C_{gd}, C_{gs}, C_{gb} \quad (22)$$

then using (20), the voltage at floating gate with 2 input capacitances can be approximated by:

$$V_{FG} = w_1 V_1 + w_2 V_2 \quad (23)$$

Substituting (23) into (19), the drain current of a N-type FG-MOS transistor, with 2 input capacitances, is as follows:

$$I_d = I_s \exp\left(\frac{w_1 V_1 + w_2 V_2}{nU_T}\right) \quad (24)$$

IV. CIRCUIT DESIGN

A. Dilation

Applying (18) and based on (4)-(6) related dilation hedge operations *minus*, *more or less*, and *slightly*, can be defined as [12]:

$$I_{minus} = I_{\mu}^{0.75} = I_{\mu}^{0.75} \cdot I_H^{0.25} \quad (25)$$

$$I_{more\ or\ less} = I_{\mu}^{0.5} = I_{\mu}^{0.5} \cdot I_H^{0.5} \quad (26)$$

$$I_{slightly} = I_{\mu}^{0.25} = I_{\mu}^{0.25} \cdot I_H^{0.75} \quad (27)$$

To exploit the generalized circuit for all dilation hedge operations, a novel synthesis employing FG-MOS transistor is presented. To this end, we begin by breaking out the first two

terms of the weighted summation of (24) and also using the fact that $e^{x+y} = e^x \cdot e^y$, which it results:

$$I_d = I_s \exp\left(\frac{w_1 V_1}{nU_T}\right) \exp\left(\frac{w_2 V_2}{nU_T}\right) \quad (28)$$

By assumption that the first input capacitance ratio is equal to the rational power ($w_1 = \alpha$), and also notice to the $w_1 + w_2 = 1$, the second input capacitance ratio can be expressed as follows:

$$w_2 = 1 - \alpha \quad (29)$$

Substituting (29) into (28) gives:

$$I_d = I_s \exp\left(\frac{\alpha V_1}{nU_T}\right) \exp\left(\frac{(1-\alpha)V_2}{nU_T}\right) \quad (30)$$

It can be shown, by some manipulation of (30), it can be rewritten as:

$$I_d = \left(I_s \exp\left(\frac{V_1}{nU_T}\right) \right)^{\alpha} \left(I_s \exp\left(\frac{V_2}{nU_T}\right) \right)^{1-\alpha} \quad (31)$$

Comparing (31) and (18) shows that, the dilation operation can be implemented if the relations between current signals I_{μ}^{α} , I_{μ} and I_H in (18) and voltage signals V_1 , V_2 and current signal I_d in (31) are as follows:

$$I_{\mu}^{\alpha}(x) = I_d \quad (32)$$

$$I_{\mu} = I_s \exp\left(\frac{V_1}{nU_T}\right) \quad (33)$$

$$I_H = I_s \exp\left(\frac{V_2}{nU_T}\right) \quad (34)$$

Fig. 3 shows the proposed circuit design for all dilation hedge operations according to (30) and (32)- (34). The circuit consists of a FG-MOS transistor and two MOS transistors that operate in weak inversion. In this Figure, FG-MOS transistor M3 is employed for implementation of (30) and (32), and transistors M1 and M2 are used for implementation of (33) and (34), respectively.

Evidently, Fig. 3 can be used for implementation of any current-mode linguistic-hedge operation that its rational power is less than one. Particularly, by considering the values of 3/4, 1/2 and 1/4 for the first input capacitance ratio in Fig. 3, the dilation hedge operations *minus*, *more or less*, and *slightly* can be implemented, respectively.

As Fig. 3 shows, the number of components in the proposed circuit is much less than those reported before [12, 13, 15].

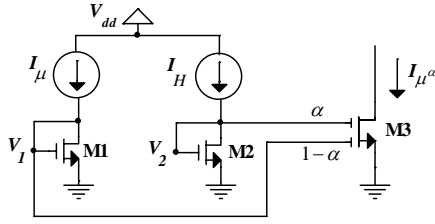


Fig. 3 Proposed circuit diagram of the dilation hedge operations

Also the source of transistors is connected to the substrate, so the body effect is eliminated. In addition, the transistors are operating in weak inversion; therefore these circuits can work in low-power, low-voltage and wide dynamic range. This Figure reveals that, the minimum supply voltage of the circuit is one V_{gs} plus one V_{ds} and since extra biasing current and voltage are not needed, the static power consumption is low. Finally, transistors M1, M2 are common elements for all dilation operations, so these transistors are merged and it results reduction of elements number.

B. Concentration

Using (18) and (8)-(12), related concentration hedge operations *absolutely*, *very*, *much more*, *more*, and *plus* can be defined as [12]:

$$I_{\text{absolutely}} = I_{\mu^4} = I_{\mu}^4 \cdot I_H^{-3} \quad (35)$$

$$I_{\text{very}} = I_{\mu^2} = I_{\mu}^2 \cdot I_H^{-1} \quad (36)$$

$$I_{\text{much more}} = I_{\mu^{1.75}} = I_{\mu}^{1.75} \cdot I_H^{-0.75} \quad (37)$$

$$I_{\text{more}} = I_{\mu^{1.5}} = I_{\mu}^{1.5} \cdot I_H^{-0.5} \quad (38)$$

$$I_{\text{plus}} = I_{\mu^{1.25}} = I_{\mu}^{1.25} \cdot I_H^{-0.25} \quad (39)$$

It can be seen the rational power α for concentration hedge operations in (7) and (35)-(39) is bigger than one ($\alpha > 1$), so the value of $1-\alpha$ is negative. Therefore, using the fact that $x^y = 1/x^{-y}$, (18) for concentration operations can be expressed as follows:

$$I_{\mu^\alpha}(x) = \frac{I_{\mu}^\alpha}{I_H^{\alpha-1}} \quad (40)$$

or equivalently, (40) can be expressed as follows:

$$I_{\mu}^\alpha = I_{\mu^\alpha}(x) \cdot I_H^{\alpha-1} \quad (41)$$

In order to employ FG-MOS transistor for implementation of (41), the powers of this equation will be converted to the values of equal or smaller than one. Performing rational power $1/\alpha$ for both sides of (41) and then using $(xy)^m = x^m \cdot y^m$,

this equation can be rewritten as:

$$I_{\mu} = I_{\mu^\alpha}^{\frac{1}{\alpha}}(x) \cdot I_H^{\frac{1-\alpha}{\alpha}} \quad \frac{1}{\alpha} < 1 \quad (42)$$

Now, using the proposed synthesis in preceding subsection and comparing (42) and (18), the concentration operations can be implemented by a few modifications of Fig. 3. To this end, the first input capacitance ratio of FG-MOS in Fig. 2 is considered equal to the inverse of rational power ($w_1 = 1/\alpha$), and also, the current signals I_{μ} and I_{μ^α} of that Figure are exchanged.

Fig. 4 shows the complete circuit design for all concentration operations based on (42). Fig. 4 can be used for implementation of any current-mode linguistic-hedge operation that its rational power is more than one. Particularly, by assumption the value of the first input capacitance ratio equal to 4, 2, 1.75, 1.5 and 1.25 in Fig. 4, the concentration hedge operations *absolutely*, *very*, *much more*, *more*, and *plus* can be implemented, respectively.

From Fig. 4, the proposed circuit for concentration operations has the same advantages that are described in the preceding section for dilation operations circuit of Fig. 3.

V. SIMULATION RESULTS

The proposed circuits of Fig. 3 and Fig. 4 were simulated using Hspice with 0.18um TSMC CMOS process parameters. The supply voltage of 0.7V was employed and the value of normalized current I_H was set to 100nA. The aspect ratios of transistors were chosen 20um/2um. For FG-MOS transistors the model of reference [23] is used. The input signal I_{μ} for simulation is applied the triangle membership functions, which are frequently used in fuzzy control system, and its amplitude was chosen 100nA. Fig. 5 shows the input signal and output responses for the first input capacitance ratio values of 3/4, 1/2 and 1/4 corresponding to the dilation hedge operations *minus*, *more or less*, and *slightly*, respectively (plots down to up accordingly). From Fig. 5, we can observe that the powers smaller than one result in convex functions.

In a similar way, Fig. 6 shows the input signal and output responses for the first input capacitance ratio values 4, 2,

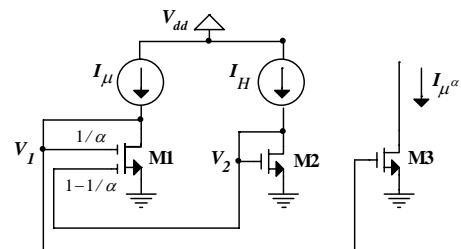


Fig. 4 Proposed circuit diagram of the concentration hedge operations

1.75, 1.5 and 1.25 corresponding to the hedge operations *absolutely*, *very*, *much more*, *more*, and *plus*, respectively (plots down to up accordingly). It can be seen that from Fig. 6, the powers bigger than one result in concave functions.

Simulation results showed the power consumption of each circuit operation is less than 200nW, the maximum absolute error is within 0.7% and dynamic range is more than 60dB. Also, the results show that the output of the proposed circuit is almost consistent with the ideal case.

A comparison was made with formerly reported hedge operation circuits. Table I summarizes this comparison by showing some important parameters of the circuits.

TABLE I
A COMPARISON BETWEEN DIFFERENT LINGUISTIC-HEDGE OPERATIONS
CIRCUITS

Parameter	Ref. [12]	Ref. [13]	Ref. [15]	This Work
Technology	035u	0.8u	0.35u	0.18u
Supply Voltage	3.3V	3.3V	3.3V	0.7V
Power Consump. for each operator	Expected >400uW	Expected >400uW	Expected >500uW	<200nW
Transistor Count for each operator	>42	>42	>44	3
Input Range	24dB	34dB	20dB	>60dB
Body Effect	Yes	Yes	Yes	No

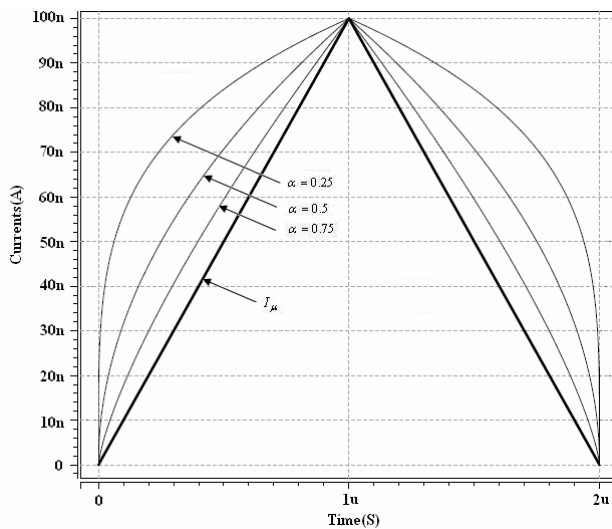


Fig. 5 Input current (bolded) and output current $I_{\mu^{\alpha}}$ for different dilation hedge operations

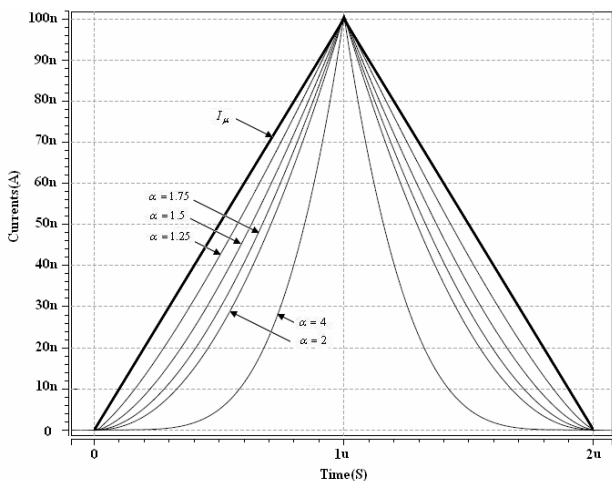


Fig. 6 Input current (bolded) and output current $I_{\mu^{\alpha}}$ for different concentration hedge operations

VI. CONCLUSION

A set of new linguistic-hedge circuit design that employs FGMOS transistors operating in weak inversion region is presented. The circuits that operate in current-mode are with low circuit complexity, are immune from body effect, work at low-voltage/low-power and do not need extra biasing to inject current into the transistors. Simulation results of the circuits show that the technique is promising and can be used in the fuzzy logic controller integrated circuits.

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Ebrahim Farshidi was born in Shoushtar, Iran, in 1973. He received the B.Sc. degree in 1995 from Amir Kabir University, Iran, the M.Sc. degree in 1997 from Sharif University, Iran and the Ph. D. degree in 2008 from electrical engineering at IUT, Iran, all in electronic engineering. He worked for Karun Pulp and Paper Company during 1997-2002. From 2002 he has been with shahid chamran university, Ahvaz, where he is currently assistant professor and head of electrical engineering department. He is author of more than 23 technical

papers in electronics. His areas of interest include current-mode circuits design, low power VLSI circuits, and data converters.