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Low Power Digital System for Reconfigurable Neural Recording System

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***Abstract*—**A digital system is proposed for low power 100-channel neural recording system in this paper, which consists of 100 amplifiers, 100 analog-to-digital converters (ADC), digital controller and baseband, transceiver for data link and RF command link. The proposed system is designed in a 0.18 μm CMOS process and 65 nm CMOS process.

***Keywords*—**multiplex, neural recording, synchronization, transceiver

I. Introduction

RECENTLY, the multi-channel neural recording system which has a wide range of applications such as upper and lower limb prostheses, bladder and bowel movement control for spinal cord injury patients has been studied popularly [1]. According to the challenging requirements for a neural recording system, the neural recording system should be recording a large number of channels, wireless transmission, on-the-fly processing, programmable specifications and power consumption and chip area [1], [2]. To meet these challenging requirements, we propose a low power 100-channel neural recording system.

The digital system consists of digital controller and digital baseband processing part. This paper covers majorly the digital system and it is organized as follows. Section II introduces the system architecture of our proposed low power 100-channel neural recording system. Section III and IV focuses on the digital controller and the digital processor, respectively. Section V discusses the simulation results and the conclusion is summarized in section VI.

II. System Architecture

The proposed system consists of three chips: neural interface IC (IC1), communication IC for data transmission and command receiving (IC2), communication IC for data receiving (IC3) and discrete module which contains command transmission and central processing unit. The block diagram of whole system is shown in Fig. 1. IC1 contains the neural probe array which is planted in brain to monitor neuron's signals and convert the amplified analog signal to the digital signal. Then the digitalized signal is processed by digital system in IC2 which is placed between skull and skin.

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IC2 is connected to IC1 by flexible cables. This wire communication is reliable and allows the IC2 to process the neural data in a real-time. The wireless communication is between IC2 and IC3 in order to avoid the significant restrictions which are imposed by wires. There are two links for data and commands, respectively. The data link has high rate for data throughput and the command link has low rate for command communication where the low power RF can be applied [3].

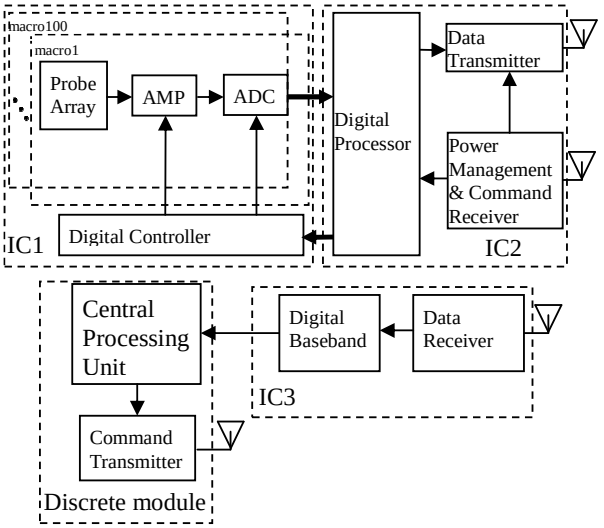

Fig. 1 Block diagram of low power 100-channel neural recording system

III. Digital Controller

Digital controller is to control 100 channels amplifiers and ADCs. It contains SPI block and multiplex block. The block diagram of IC1 is shown in Fig. 2.

To accommodate the requirements of various different applications, the specifications, such as the selected channels, the gains and bandwidths of amplifiers and the mode of ADC should be programmed by digital controller through SPI. The signals of SPI are from IC2. Compared with our previous system [4], we can choose any No. of channels. The channels which are not used will be disabled to reduce the power consumption. There are two ADC modes: fast mode and slow mode. The default setting is enabled 20 slow ADC and 18 fast ADC. The multiplex ADC out is sampled by clk. The output sequence is 18 fast parallel ADC channels followed by 2 slow parallel ADC channels in one 25 kHz time cycle. To decrease the power consumption, we set the clock gating style in the synthesis. The schematic diagram of the multiplex is shown in Fig. 3.

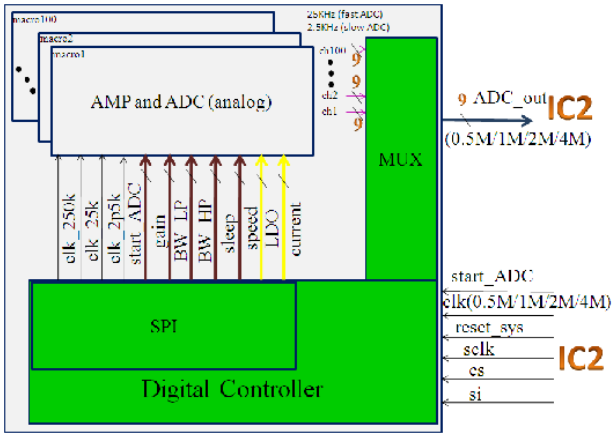

Fig. 2 Block diagram of IC1

In Fig. 3, we only take 10 channels for example. Here, sleep[9:0] is configured as 0111000101 and speed[9:0] is configured as 0100111110. In other words, channel 1, 3, 7, 8 and 9 are enabled and the other 5 channels are disenabled. The channel 1, 7 and 8 are fast ADC channels among the 5 enabled channels and the other 2 enabled channels are slow ADC channels.

N_{fast} is the No. of fast ADC channels and N_{slow} is the No. of slow ADC channels.

The data rate of ADC output in multiplex is fixed. In our design, there are four data rate – 0.5M, 1M, 2M and 4M. The data rate can be configured by SPI. If the real data rate is smaller than the data rate we set by SPI, some zeros are inserted. In the digital synthesis, we set clock gating style. Thus, this method can save much power consumption when the real data rate is smaller than the configured data rate.

IV. Digital Processor

Digital processor contains four main blocks: data coder, command decoder, SPI block and ack block. Data coder block is to code the ADC and power information. Command decoder block is to decode the command information from command RX (RF) block. SPI block is to configure programmable parameters. The ack block is to generate the coded acknowledgement. The block diagram of digital processor is shown in Fig. 4. There are two modes for this part. If enable is 1, all parameters can be programmed by command link. Otherwise, they will be programmed by external SPI signals.

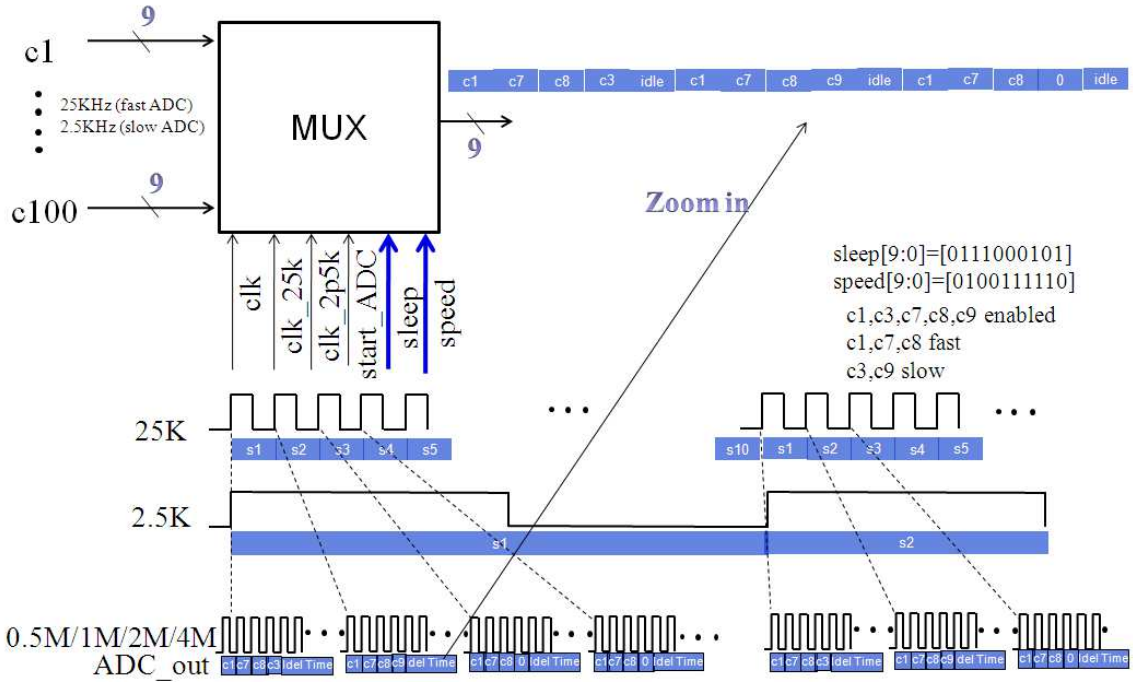

Fig. 3 The schematic diagram of the multiplex

The ADC output clocks 25kHz and 2.5kHz are divided from 0.5M/1M/2M/4M. The real data rate is calculated by the formula

$$rate_{real} = 25000 \times N_{fast} + 2500 \times N_{slow} \quad (1)$$

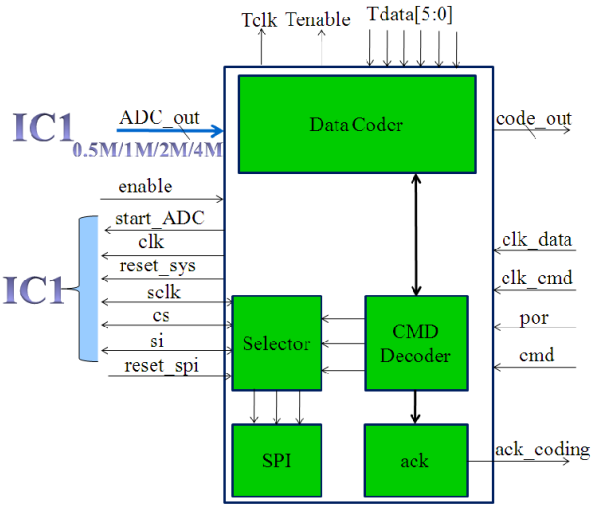

Fig. 4 Block diagram of digital processor

A. Data coder

For command mode, there are four data rate of ADC's outputs. The parallel ADC data combined with power information will be transformed as serial data. The data rate of the serial data is ten times than original ADC data. After serial-to-parallel conversion, the data rate is down to 5M/10M. Thus, Data coder has 1, 2 or 4 input bits if the serial data rate is 5M/10M, 20M or 40M, respectively. The code rate of data coder is 16, so the data rate after data coder is 80M/160M. The block diagram of data coder is illustrated in Fig. 5. After header generation, data coding is done according to our coding Table. In the period of header generation, the ADC start signal – start_ADC will be high from low to synchronize IC1 and IC2. In SPI testing mode, the inputs of data coder are from external signals-Tdata[5:0] and the p/s and s/p will be bypassed. For synchronization with internal 5M/10M in SPI testing mode, digital processor will generate this 5M/10M clock to sample Tdata[5:0] when the Tenable is high.

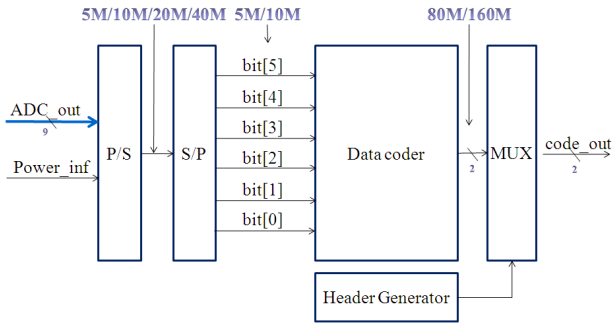

Fig. 5 Block diagram of data coder

B. Ack block

The ack block will spread the power information according to the coding Table, which is shown in TABLE I. We use 001100111010 as our preamble because this sequence has good correlation property. Fig. 6 shows the auto-correlation property of this preamble. This coding style is similar with baseband of command transmitter.

TABLE I
THE CODING TABLE OF ACK BLOCK

bit	Coding sequence
0	01100010111
1	00011101011

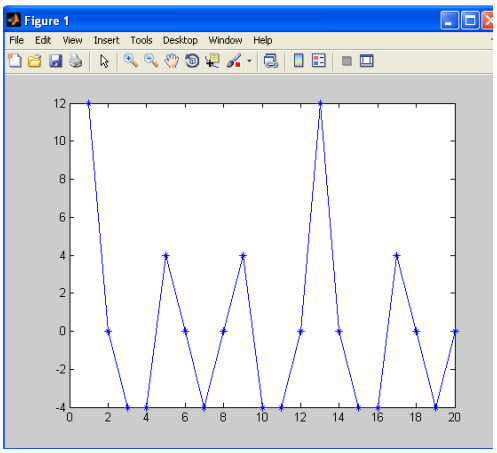

Fig. 6 The auto-correlation property

C. CMD decoder

As mentioned in ack block, the preamble is also 001100111010. In CMD decoder, we employ the property of correlation to detect the preamble. The discrete cross-correlation [4] is defined as

$$p(m) = \sum_{k=0}^{n-1} r(m+k) \cdot w(k). \qquad (2)$$

Where $r(\cdot)$ is received bitstream, $w(\cdot)$ is preamble and n is the length of window. Here n is 12. As well known, auto-correlation will always generate a peak correlation value. The cross-correlation should be computed using formula (1) for every clock. If the value of computed the cross-correlation between received bitstream and preamble sequence is above the threshold T, the preamble is determined.

When the preamble is detected, the dispreading will be done. It is the inverted procedure of spreading mentioned in Table I.

V. Simulation Results

We use Matlab for system level performance and optimization. Then we convert the Matlab design into Verilog-HDL. The standard digital design flow is then applied, which includes RTL coding, synthesis, place and route and verification.

Assume that ADC's output data is the No.th of channel. Under the default settings, the simulation result of IC1 is shown in Fig. 7. Then, we change the data rate as 4M and change the No. of enabled ADC by using SPI, the simulation result of IC1 is shown in Fig. 8.

Fig. 7 The simulation result of IC1 (0.5M)

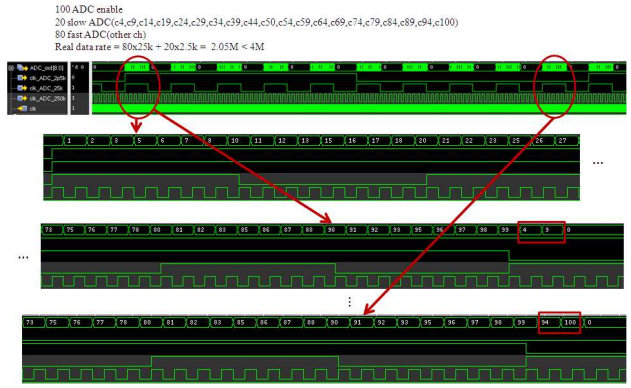

Fig. 8 The simulation result of IC1 (4M)

Fig. 9 shows a simulation result of ack block. When a command is received completely, the encoded acknowledgement will be generated. Here, the power information is 10. Thus, the coded acknowledgement is 00110011101000011101011011000010111.

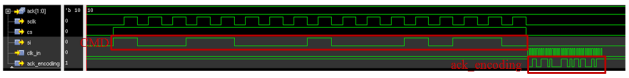

Fig. 9 A simulation result of ack block

VI. Conclusion

In this paper, we have presented a digital system for our low power 100-channel neural recording system with human body communication. It is implemented in 0.18-µm CMOS technology and 65-nm CMOS technology. The core area of digital IC1 (DIC1) which is implemented by using 0.18-µm CMOS technology is about 1500-µm by 200-µm and the core area of digital IC2 (DIC2) which is implemented by using 65-nm CMOS technology is about 200-µm by 200-µm.

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