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Jitter Transfer in High Speed Data Links

Tsunwai Gary Yip

***Abstract*—**Phase locked loops for data links operating at 10 Gb/s or faster are low phase noise devices designed to operate with a low jitter reference clock. Characterization of their jitter transfer function is difficult because the intrinsic noise of the device is comparable to the random noise level in the reference clock signal. A linear model is proposed to account for the intrinsic noise of a PLL. The intrinsic noise data of a PLL for 10 Gb/s links is presented. The jitter transfer function of a PLL in a test chip for 12.8 Gb/s data links was determined in experiments using the 400 MHz reference clock as the source of simultaneous excitations over a wide range of frequency. The result shows that the PLL jitter transfer function can be approximated by a second order linear model.

***Keywords*—**Intrinsic phase noise, jitter in data link, PLL jitter transfer function, high speed clocking in electronic circuit

I. Introduction

HIGH speed, data links running at 16 Gb/s in parallel can provide terabyte memory bandwidth for high performance computing [1]. The random jitters of the link components are as small as one picosecond or less in order for the link to achieve sufficiently large data opening.

Fig. 1 is a generic model of jitter propagation typical of the architecture of data links. The phase locked loops (PLLs) in the transmitting (Tx) and receiving (Rx) devices and the reference clock source are primary sources of the random jitters in the received data stream. Since these PLLs are designed to operate with a low jitter input reference signal, output signal can be dominated by the intrinsic noise of the PLLs, N_{TX} and N_{RX}. Reported in this paper is a novel technique for characterizing high speed, low jitter PLLs. The focus of this study is on the intrinsic phase noise and jitter transfer functions of the PLLs. The approach is based on a linear model which accounts for the intrinsic noise.

II. Clock Jitter Reduction

The jitter transfer functions of the Tx PLL and Rx PLL in a data link determine the degree of jitter reduction in the reference clock signal. In Fig. 1 jitters from the clock source propagate along the data and reference clock (RefClk) paths. The Tx PLL and Rx PLL are low pass filters thus reducing the high frequency jitter components in the clock signal. The remaining low frequency jitters are partially cancelled in the receiving device after the Rx PLL. The received data also carry the intrinsic noise of both PLLs. References [2] and [4] report the characterization of the band pass filtering effect in 5 Gb/s data links.

Tsunwai Gary Yip, Ph.D., is with Rambus Inc., 4440 El Camino Real, Los Altos California 94022 (e-mail:gyip@rambus.com). He is an Associate Fellow of the American Institute of Aeronautics and Astronautics.

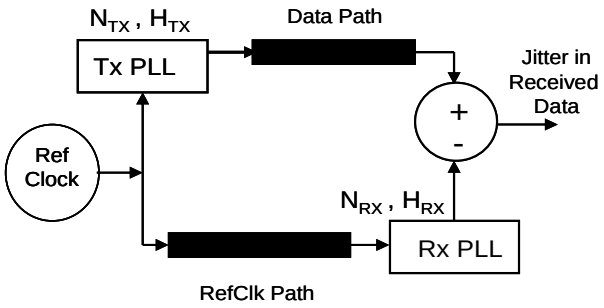

Fig. 1 Generic model of jitter propagation commonly found in high speed data link architecture

III. Intrinsic Phase Noise

The intrinsic phase noise of a PLL must be accounted for in order to characterize its phase jitter transfer function accurately. The data in Fig. 2 are the phase noise profiles output by a PLL for three different RefClk noise levels. When a nominal RefClk is used, the PLL output exhibits its characteristic peaking behavior. As the jitter of RefClk decreases, the output becomes dominated by the intrinsic phase noise of the PLL. When the jitter of RefClk is below a certain level, the effect of peaking is masked out completely. Therefore, the intrinsic phase noise can be measured when the RefClk has very low phase noise. Fig. 3 shows the intrinsic phase noise associated with the random jitter of a 5 GHz PLL. The data exhibits a 10 dB/decade slope on the left and -20 on the right. The deterministic jitter components are separated and not shown.

IV. A Linear Model with Intrinsic Noise

In this study a linear model including a term to account for the intrinsic noise of a PLL is used to analyze the phase jitter transfer function of the PLL.

The phase noise of PLL output Y at the offset frequency *f* is represented by

$$Y(f) = X(f)\,H(f) + N(f) \quad (1)$$

where X is the phase noise of the input clock (RefClk), and N is the intrinsic phase noise of the PLL [3]. Equation (1) is in the spectral power density domain and its unit is dBc/Hz.

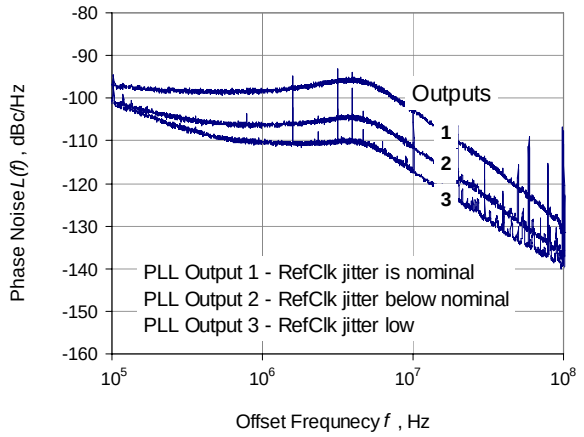

Fig. 2 Peaking becomes dominated by the intrinsic phase noise of the PLL as RefClk jitter decreases

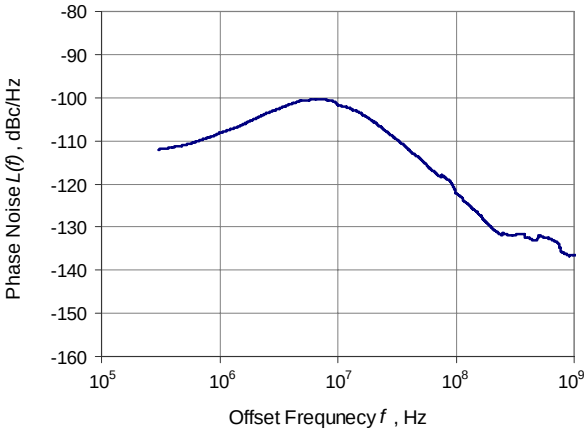

Fig. 3 Intrinsic random phase noise of a 5 GHz PLL (deterministic jitter components are removed)

Fig. 4 shows two phase noise profiles of the 6.4 GHz outputs of a PLL in a test chip for a 12.8 Gb/s data link. The frequency of the RefClk is 400 MHz. When the jitter of RefClk is low, the intrinsic noise of the PLL is significantly larger than the amplified input phase noise, i.e. Y ~ N. For a RefClk with nominal jitter, the frequency multiplication also amplifies the input phase noise by the same ratio, 24 dB. The resulting phase noise is high enough to mask out the intrinsic noise of the PLL, i.e. Y ~ XH. These measurements show that Equation (1) is an adequate approximation of the jitter transfer for PLLs that requires low phase noise reference clock in high speed data links.

V. Jitter Transfer Function

Given two inputs of the same frequency but different in jitter levels, namely X_1 and X_2, the corresponding outputs can be written as:

$$Y_1(f) = X_1(f)\,H(f) + N(f) \quad (2)$$

$$Y_2(f) = X_2(f)\,H(f) + N(f) \quad (3)$$

The jitter transfer function can be determined by

$$H(f) = \frac{Y_2(f) - Y_1(f)}{X_2(f) - X_1(f)} \quad (4)$$

where X_1 and X_2 cannot be too small for Y ~ N to be true.

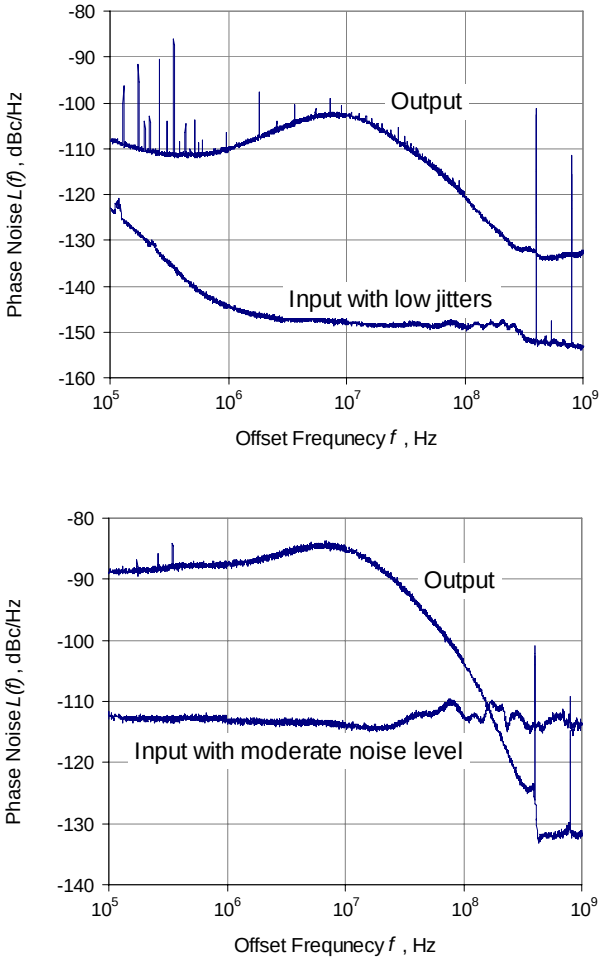

Fig. 4 Variations in output phase noise with low and moderate levels of input jitters

VI. Transfer Function Characterization

Figs. 5 and 6 show the phase noise profiles of two 400 MHz inputs and the corresponding PLL outputs at 6.4 GHz. The data points were collected using an instrument for measuring phase noise. Each profile has a few thousands data points over the indicated range of offset frequency. Based on the definition of phase noise, the data are valid up to the offset

frequency equal to one half of the carrier frequency. Since the input carrier, RefClk, is 400 MHz, the jitter transfer function determined from the data is valid up to 200 MHz.

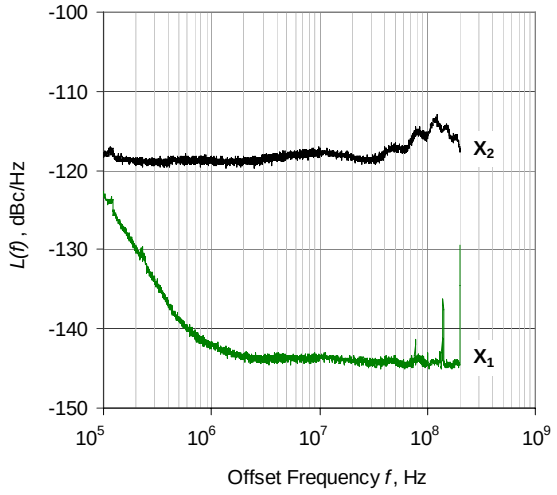

Fig. 5 Two phase noise profiles for different levels of input clock jitter

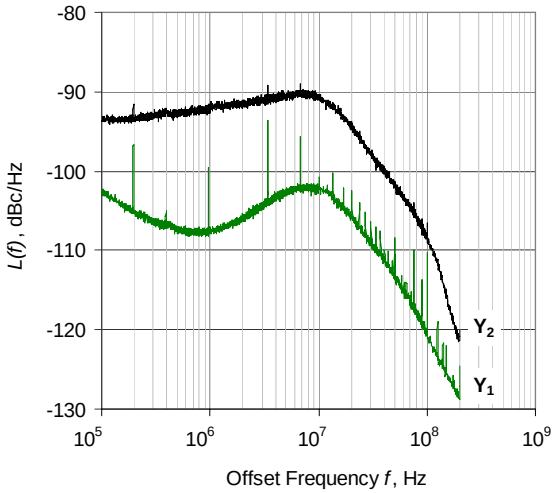

Fig. 6 PLL outputs at 6.4 GHz for the two levels of jitters carried by the input clock

The jitter transfer function determined using Equation (4) is shown in Fig. 7. The -3dB point of the PLL is at 40 MHz. The decay of the transfer function matches the rate of a second order linear model, i.e. -20 dB per decade.

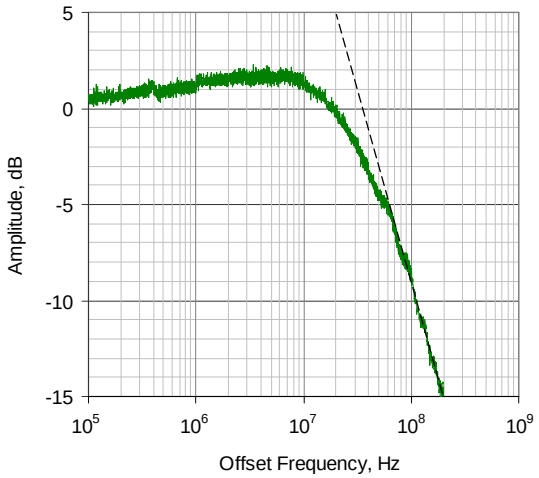

Fig. 7 Jitter transfer function of a 6.4 GHz PLL. Dotted line indicates the 20 dB/decade decay rate typical of a second order linear model

VII. Comparison with Sinusoidal Excitation

Equation (4) can also be used to determine the transfer function when the RefClk is modulated by a sinusoidal signal. This commonly used technique can characterize the PLL at one discrete frequency at a time.

Contrarily the present approach requires only four measurements to determine the jitter transfer function over a range of frequency by introducing excitations simultaneously at different frequencies. Each phase noise measurement captures a profile of the jitter components. Two RefClks of different phase noise levels are used. The profile of the excitations includes the difference in the phase noise at each frequency. Accordingly the response of the PLL is the difference in the two corresponding output noise profiles. Based on Equation (4), four phase noise measurements can collect sufficient data to determine the jitter transfer function over a selected offset frequency range.

A reference clock, instead of a sinusoidal, signal is normally the input of a PLL and its jitter is wideband. The output of the PLL contains the responses to the simultaneous modulation by all the jitter components in the RefClk signal. The jitter transfer characteristic determined by a sinusoidal modulation cannot capture the simultaneous phase modulations at the adjacent frequencies. Therefore clock sources with nominal jitter levels can introduce the more realistic wideband excitation encountered by a PLL.

VIII. Conclusion

This study has shown that a linear model with an intrinsic noise term is adequate for describing the jitter transfer characteristic of low noise PLLs for high speed data links. Measurement of the intrinsic noise of a PLL requires a very low noise RefClk source. The paper has also introduced a novel approach for determining the jitter transfer function of a PLL. It uses a clock with jitter near the nominal operating

conditions as a source for wideband excitation. The results show that the PLLs in this study have the characteristics of a second order linear system.

REFERENCES

[1] *Terabyte Bandwidth Initiative*, Rambus Developer Forum, Tokyo, Japan, November 28-29, 2007.
[2] Ken Chen et al, "Clock and Circuit Design for a Parallel IO on a First Generation Cell Processor", Session 28, Paper 28.9, IEEE International Solid-State Circuit Conference, San Francisco, California, Feb. 6, 2005.
[3] T.G. Yip, *Phase Noise Initiative: Characterizing Intrinsic Phase Noise and Phase Noise for Diagnostic*. Rambus Technical Forum, Nov. 16, 2007.
[4] T.G. Yip et al, "Clock Jitter Reduction in High Speed Interfaces", Accepted for presentation at DesignCon 2009, Santa Clara, California USA, February 2009.