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Investigation of Multiple Material Gate Impact on Short Channel Effects and Reliability of Nanoscale SOI MOSFETs

Paniz Tafakori and Ali A. Orouji

Abstract**—**In this paper the features of multiple material gate silicon-on-insulator MOSFETs are presented and compared with single material gate silicon-on-insulator MOSFET structures. The results indicate that the multiple material gate structures reduce short channel effects such as drain induce barrier lowering, hot electron effect and better current characteristics in comparison with single material structures.

Keywords**—**Short-channel effects (SCEs), Dual material gate (DMG), Triple material gate (TMG), Pentamerous material gate (PMG).

I. Introduction

AS improvement of technology, the feature size of CMOS circuits is reduced [1]. Also the smaller dimension of (CMOS) devices created problems such as short-channel effects (SCEs); including problems that arise due to shrinking device dimensions have been created. Some of these effects contain drain induced barrier lowering (DIBL), subthreshold swing, threshold voltage roll-off, hot carrier effect, and increased leakage current. Multiple structures have been presented to reduce SCEs in SOI transistors [2]. Silicon on insulator (SOI) transistors have many advantages in compared with bulk transistors such as reduced parasitic capacitance and less short channel effects [3].

Long et al, [4] in 1999 introduced a new structure that they called dual material gate (DMG) FET, which improves short channel effects, electric field of the source side and carrier transport efficiency using gate engineering instead of doping engineering. In a DMG FET two variant material with different work functions are situated which for an n-channel MOSFET the work function of metal gate1 must be greater than metal gate2 and inverse for a p-channel MOSFET [3]. Also, the variation of minimum channel potential in DMG structure due to the greater work function of gate near the source is negligible Therefore, the DMG structure in SOI MOSFETs is preventing completely affecting from DIBL effects [5]. So DMG structures are good candidates for sub-100nm structures to improving short channel effects [2]. Also using of triple material structures due to more controllability upon the channel leads to better short channel effects [6]. In this paper we have investigated the dual material gate(DMG), triple material gate (TMG), and pentamerous material gate (PMG) SOI MOSFET structures using the device simulator ATHLAS [7]. Our results indicate that the DMG, TMG, and PMG structures improve short channel effects such as DIBL, subthreshold swing and hot electron effect in comparison with the SMG structure.

Paniz Tafakori, Electrical Engineering Department, Semnan University, Semnan, Iran, (corresponding author to provide phone: 00989123969445; e-mail: paniz.tafakori@yahoo.com).

Ali. A. Orouji, Electrical Engineering Department, Semnan University, Semnan, Iran, (e-mail: aliaorouji@ieee.org).

II. Device Structure

A schematic cross-sectional view of DMG, TMG, and PMG SOI MOSFETs are shown in Fig. 1-a, 1-b, and 1-c, respectively [8]. The channel length of SMG structure is equal to *100nm* [9]. The gate materials of *DMG* structure are M_1, M_2 with gate lengths $L_{G1}=L_{G2}=50nm$. For TMG structure the gate materials are M_1, M_2, M_3 with gate lengths $L_{G1}=L_{G2}=L_{G3}=33nm$ and the gate materials of PMG structures are M_1, M_2, M_3, M_4, M_5 with gate lengths $L_{G1}=L_{G2}=L_{G3}=L_{G4}=L_{G5}=20nm$ [10]. Table I indicates the work function of gate materials for the structures. The doping concentration in the p type region is $10^{15}cm^{-3}$ and n^+ source/drain regions is kept at $2\times10^{19}cm^{-3}$[3]. The value of gate-oxide thickness is equal to 2nm. The thickness of thin-film, and buried oxide are *60 nm*, and *340nm*, respectively. All parameters of SMG MOSFET are equivalent to those of DMG, TMG, and PMG MOSFETs [8].

TABLE I
Work Function of the DMG, TMG, and PMG Structures

Structure	Φ_1	Φ_2	Φ_3	Φ_4	Φ_5
DMG	5.65	4.6	-	-	-
TMG	5.65	5	4.6	-	-
PMG	5.65	5.2	5	4.8	4.6

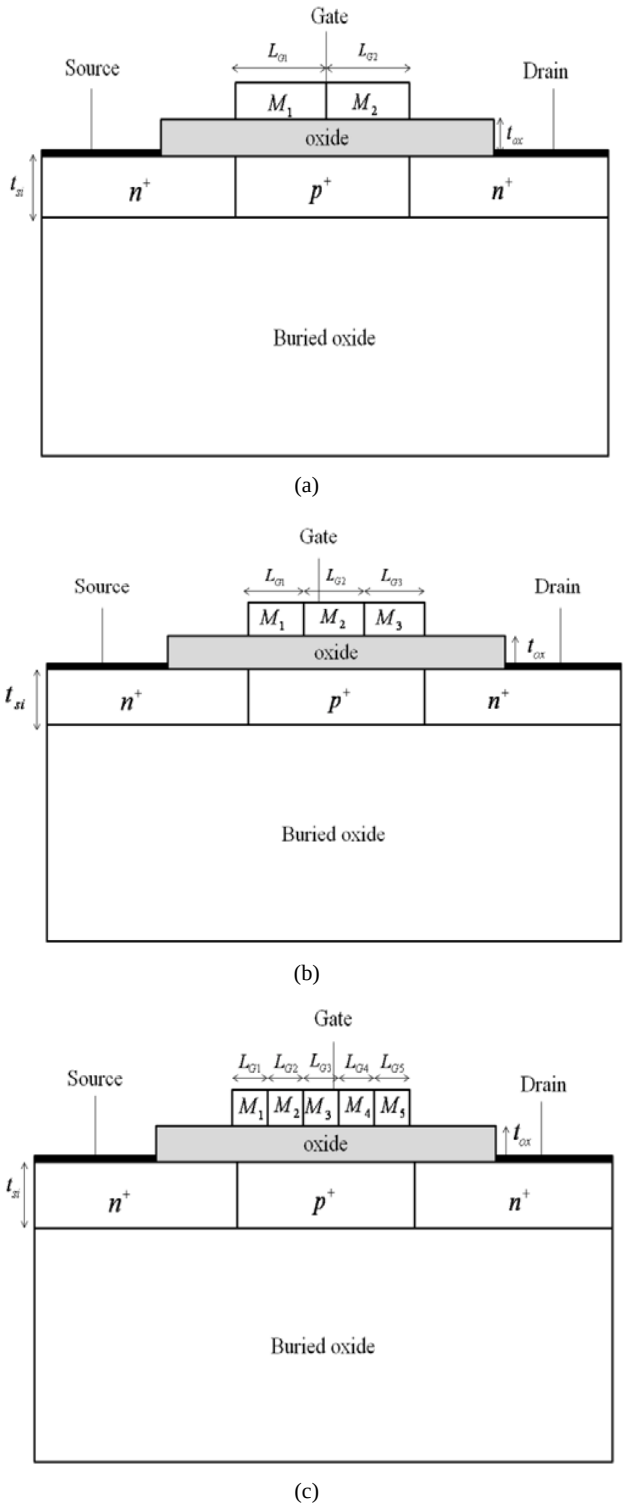

Fig. 1 Schematic cross-sectional view of (a) DMG, (b) TMG, and (c) PMG SOI MOSFETs

III. Results And Discussion

In Fig. 2 output characteristics of DMG, TMG, and PMG structures are compared with the SMG device for the same channel length *L=100nm*. It can be seen from Fig. 2 that the drain current of DMG, TMG, and PMG structures is lower than the SMG structure because of the difference in threshold voltages. The DIBL is determined as the division of difference between threshold voltages to difference of drain voltages when the drain voltage is increased from 0.01 to 1 volt. The off-state leakage current(I_{off}) is the drain current at $V_D=0.1$ *V* and $V_G=-0.2$ *V* when the gate voltage changes from -0.5 to -0.2 volt and also the saturation current is the drain current at $V_D=1$ *V* and $V_G=1$ *V* when gate voltage changes from 0 to 1volt [11].

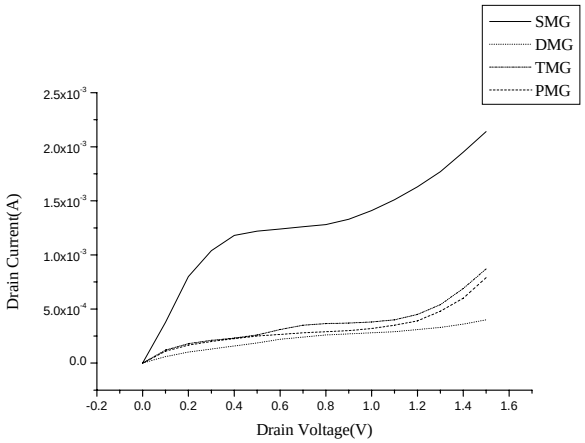

Fig. 2 I_D-V_D characteristics of SMG, DMG, TMG, and PMG structures for channel length L=100nm

Table II shows the DIBL structures. It can be observed from the table that using of DMG, TMG, and PMG structures leads to better DIBL because of better channel control by gates [6]. Fig. 3 indicates the off-state leakage current in channel. We can be observed from the figure that the off-state leakage current in DMG, TMG, and PMG structures is reduced in comparison with SMG structure. Also the on-off current ratio of PMG structure is more than other structures which is shown in Fig. 4.

TABLE II
DIBL Values for DMG, TMG, and PMG Structures

Structure	DIBL
SMG	3.33
DMG	2.22
TMG	1.11
PMG	1.1

Fig. 5 shows the surface potential profile in channel. It can be observed that the barrier height of SMG structure is more than other structures. Fig. 6 indicates the electric field in lateral position of the channel. It can be observed from the figure that the DMG structure has lower electric field at drain side which it means the hot electron effect is reduced in comparison with other structures [2]. Also shows the peak of

the electric field near the source in the DMG, TMG, and PMG structures is reduced due to accelerating rapidity of the carriers in the channel [12].

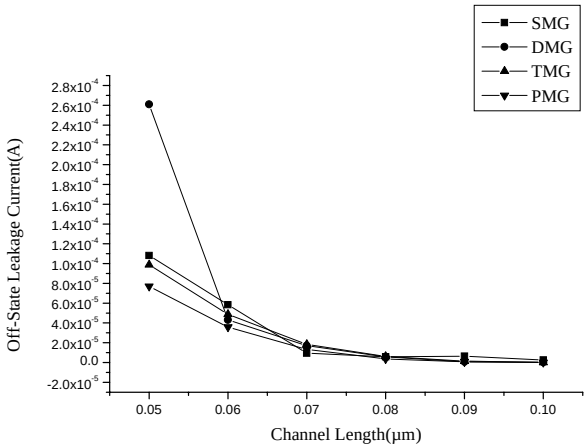

Fig. 3 Variation of off-state leakage current characteristics of SMG, DMG, TMG, and PMG structures for different channel lengths

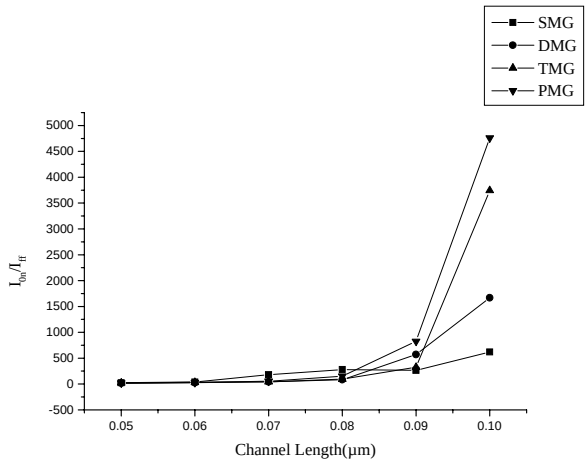

Fig. 4 The on-off current ratio of SMG, DMG, TMG, and PMG structures for the different channel length

Fig. 7 shows the threshold voltage in the channel. As we can be observed from the figure PMG structure in compare with SMG structure has better threshold voltage roll-off. Fig. 8 shows the transconductance of SMG, DMG, TMG, and PMG structures at $V_D=0.5\ V$ when the gate voltage changes from 0 to 2 volt. As we can be observed from the Fig. 8 until $V_G=0.83\ V$ transconductance of DMG, TMG, and PMG are more than SMG and vice versa for voltages greater than 0.83 volt. Fig. 9 shows the drain conductance of SMG, DMG, TMG, and PMG structures at $V_D=0.5\ V$ and the gate voltage changes from 0 to 2 volt for the channel length $L=100nm$. As we can be seen from the Fig. 9 the drain conductance of SMG structure are much lower than the DMG, TMG, and PMG structures.

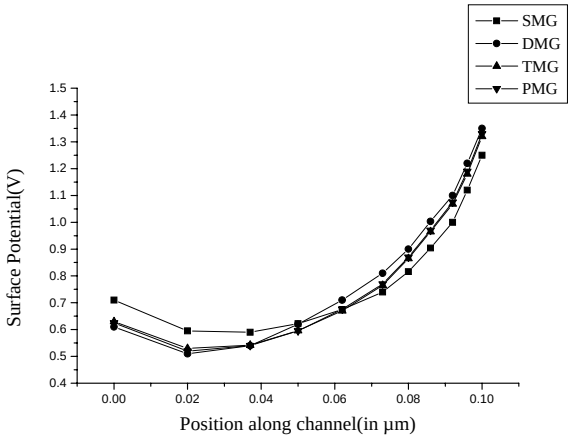

Fig. 5 Surface potential profile in the channel of SMG, DMG, TMG, and PMG structures for the channel length L=100nm

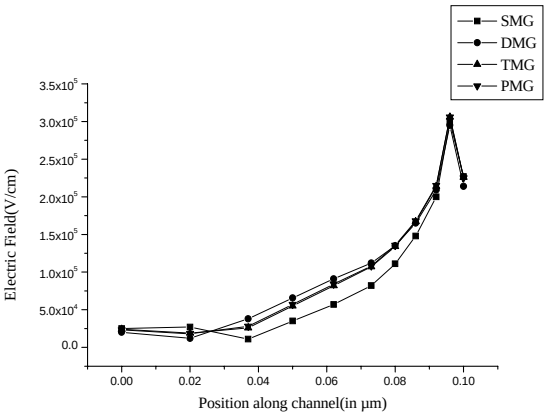

Fig. 6 Electric field in the channel of SMG, DMG, TMG, and PMG structures for channel length L=100nm

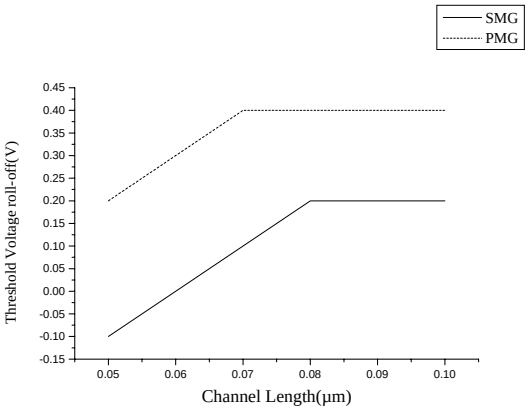

Fig. 7 Threshold voltage of SMG and PMG structures for different channel lengths

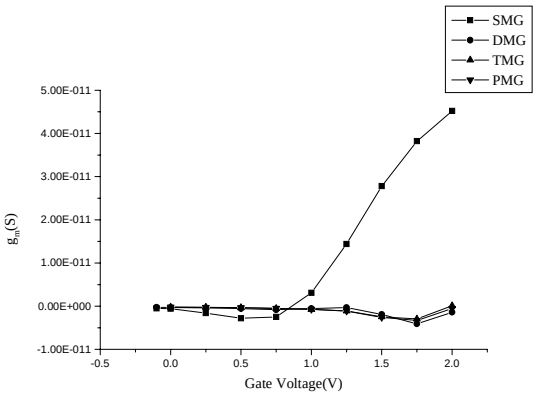

Fig. 8 Transconductance of SMG, DMG, TMG, and PMG structures for the channel length L=100nm

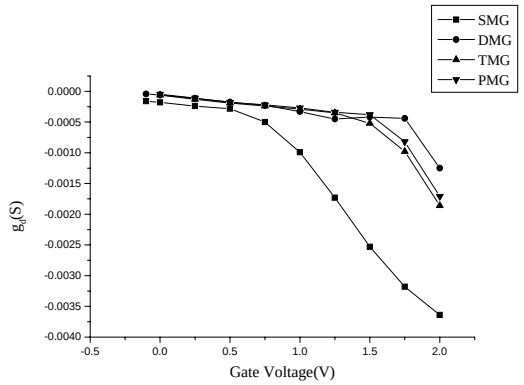

Fig. 9 Drain conductance of SMG, DMG, TMG, and FMG structures at V_D=*0.5 V* for the channel length *L=100nm*

IV. Conclusion

To decrease the short channel effects of sub-100nm single material gate SOI MOSFETs and improvement performance of the device dual material, triple material and pentamerous material gate structures are proposed and compared with together. Based on the simulation consequence, it is indicated that due to the presence of the different materials with various work functions in the gates leads to better control of the channel by gates and consequently reduces short channel effects such as DIBL and hot electron effect. Also it can be observed that the DMG, TMG and PMG structures leads to reduction of transconductance and improvement of drain conductance.

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P. Tafakori Delbari received the B.E. degree in electronic engineering from Azad University of Saveh, Markazi, Iran, in 2008, and is already studying the M.S. degree at Electrical Engineering Department of Semnan University, Semnan, Iran. Her research interests include analysis and simulation of Silicon-on-Insulator transistors (SOI MOSFETs).

A. A. Orouji (M'05) was born in Neyshabour, Iran, in 1966. He received the B.S. and M.S. degrees in electronic engineering from the Iran University of Science and Technology (IUST), Tehran, Iran, in 1989 and 1992, respectively. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, Indian Institute of Technology, Delhi, Hauz Khas, New Delhi, India. Since 1992, he has been working at the Semnan University, Semnan, Iran, as a faculty member. His research interests are in modeling of silicon- on- insulator metal-oxide-semiconductor field-effect transistor (SOI MOSFET), novel device structures, and analog integrated circuits design.