Investigation of Constant Transconductance Circuit for Low Power Low-Noise Amplifier

Wei Yi Lim, M. Annamalai Arasu, M. Kumarasamy Raja, and Minkyu Je

Abstract**—**In this paper, the design of wide-swing constant transconductance (g_m) bias circuit that generates bias voltage for low-noise amplifier (LNA) circuit design by using an off-chip resistor is demonstrated. The overall transconductance (G_m) generated by the constant g_m bias circuit is important to maintain the overall gain and noise figure of the LNA circuit. Therefore, investigation is performed to study the variation in G_m with process, temperature and supply voltage (PVT). Temperature and supply voltage are swept from -10 °C to 85°C and 1.425 V to 1.575 V respectively, while the process conditions are also varied to the extreme and the g_m variation is eventually concluded at between -3% to 7%. With the slight variation in the g_m value, through simulation, at worst condition of state *SS*, we are able to attain a conversion gain (S_{21}) variation of -3.10% and a noise figure (*NF*) variation of 18.71 %. The whole constant g_m circuit draws approximately 100μA from a 1.5V supply and is designed based on 0.13μm CMOS process.

Keywords**—**Transconductance, LNA, temperature, process.

I. INTRODUCTION

CONSTANT g_m circuits are often used to bias analog circuit blocks, to ensure that the key performance metrics are not compromised under PVT (Process, Voltage and Temperature) variations. An example of such key analog block is a LNA. By using an external off chip resistor, the g_m of the bias circuit and LNA is fixed. Since the overall gain of a simple source degenerated LNA is G_mR_{Load}, by maintaining the G_m of circuit, even when process, temperature and supply voltage are changed, performance of the LNA will not be compromised. Therefore, for our study purpose, we have decided to make use of a wide-swing constant g_m bias circuit [1] to bias a differential LNA. However, since our focus is on demonstrating the const- $g_{m,}$ we will use a single-ended LNA (Fig. 2) for illustration and explanation purposes. A study of the behavior of the G_m of the LNA circuit with process, temperature and voltage variation will be discussed in this paper.

Investigation is performed with process variation, temperature varying from -10°C to 85°C and supply voltage changing from 1.425 V to 1.575 V.

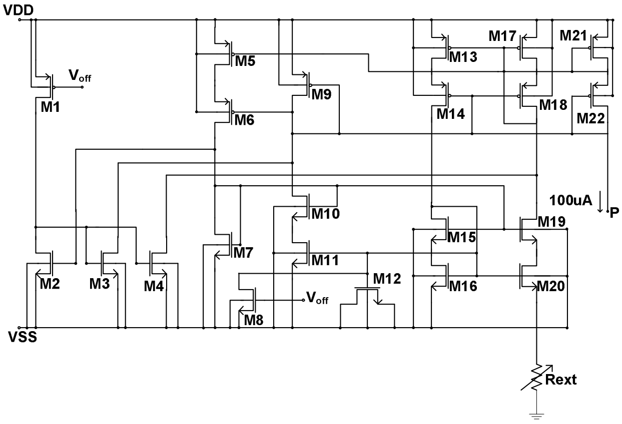

Fig. 1 Wide-swing constant g_m bias circuit

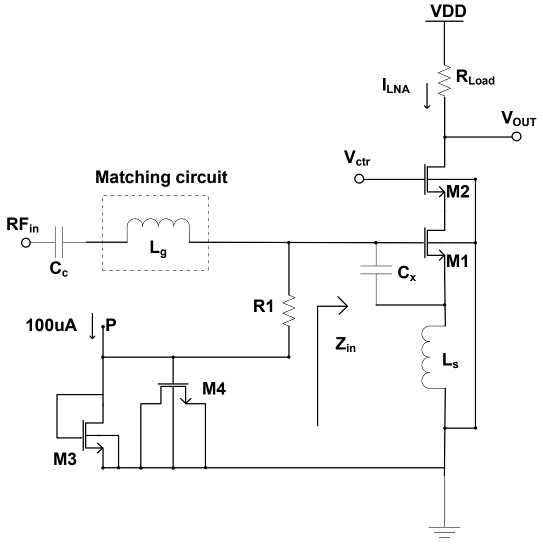

Fig. 2 Schematic of the LNA design

II. CONSTANT G_M BIAS CIRCUIT

The constant g_m circuit designed is shown in Fig. 1. This circuit is a typical wide-swing constant g_m bias circuit [1]. We have decided to make use of a wide-swing constant g_m bias circuit as it reduces second-order effects caused by finite output impedance of transistors. Voltage V_{off} of Fig. 1 is kept low to ensure that transistor *M1* is always on, the gate of transistors *M3* and *M4* will be pulled high and these transistors will then start up the whole circuit. Once the circuit is in operation, transistor *M2* will be turned on, drawing all the current from *M1* to ground. The startup circuit will then be

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turned off. Since there are parasitic capacitance contribution by the pad, transistor *M1* is designed to act as capacitor to maintain the stability of the circuit. The offchip resistor, *Rext*, is kept at 4.32 kΩ in simulation. This will send a current of 100 µA across transistor *M21* and *M22*. As shown in Fig. 1, the generated current will flow through the node P in Figs. 1 and 2. A bias voltage of about 0.62 V will be generated at the input gate of the LNA circuit. The g_m value of transistor *M1* of Fig. 2 will determine the overall gain of the LNA circuit. Thus, maintaining a constant g_m value is relatively important to ensure good performance of the circuit. We can investigate the PVT variation on the overall G_m of the LNA. In this paper, we will define *SS*, *SF*, *TT*, *FS* and *FF* as the different states for the circuit and their definitions are summarized in Table I. The g_m value of transistor *M1* of Fig. 2 at state *TT* is taken as the reference value and the g_m percentage variation for different states are plotted in Fig. 3. Due to the usage of the constant g_m bias circuit, we are able to keep the variation of g_m value at a relatively low percentage of between -3 % and 7% with different PVT setting. If we should replace the constant g_m circuit with an ideal current source at point *p* and to supply a current of 100 µA to transistor *M3* (Fig. 2), we will notice a bigger variation in the G_m of the LNA circuit, of about ±20 % (illustrated in Fig. 3). Therefore, we can conclude that constant g_m bias circuit is able to maintain a more stable g_m value than an ideal current source structure.

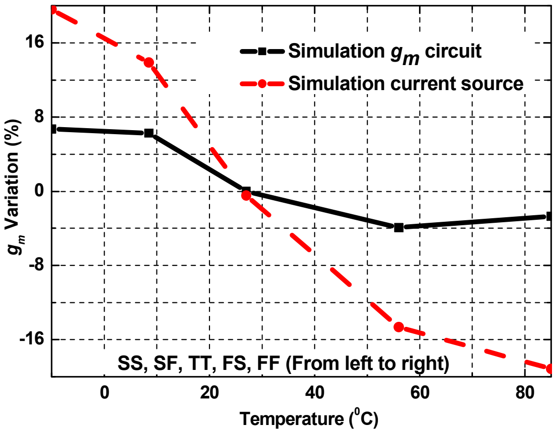

Fig. 3 g_m % variation for different states at different temperature

The phenomena which we observe in Fig. 3 can actually be explained with the g_m of a *NMOS* transistor operating in saturation region. The drain current flowing through a transistor, for instance, *M1*, can be expressed as below:

$$I_{D,M1} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \tag{1}$$

where $I_{D,M1}$ is the drain current that is flowing through transistor *M1*, μ_n is the mobility of electrons, C_{ox} is the gate oxide capacitance per unit area, *W/L* is the aspect ratio of transistor *M1*, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage of transistor *M1*, V_{DS} the drain source voltage and λ is the channel-length modulation coefficient. Expressing (1) in terms of g_m, we can get (2) as below:

TABLE I
DEFINITION OF DIFFERENT STATES

State	*Process*	*Supply Voltage (V)*	*Temperature (°C)*
SS	Slow-Slow	1.425	85
SF	Slow-Fast	1.463	56
TT	Typical	1.5	27
FS	Fast-Slow	1.538	8.5
FF	Fast-Fast	1.575	-10

TABLE II
S_{21} AND *NF* OF CIRCUIT WITH DIFFERENT SETUP

Different Setup	*State*	S_{21}	*NF*
Current source	*TT*	36.16	1.55
Constant g_m	**TT**	**36.16**	**1.55**
Current source	*SF*	35.06	1.72
Constant g_m	**SF**	**35.64**	**1.70**
Current source	*SS*	34.44	1.87
Constant g_m	**SS**	**35.04**	**1.84**

$$g_{m,M1} \approx \sqrt{\frac{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} I_{D1}}{(1+\lambda V_{DS})}} \tag{2}$$

Looking at (2), we know that μ_n decreases exponentially when temperature increases. Apart from temperature, process change will also affect the g_m of a *NMOS* transistor as different process will have different V_{TH} value with slow process having a larger V_{TH} value as compared to typical or fast process. Looking at (1), we know that a larger V_{TH} will result in a lower drain current and thus a lower g_m value. This explains why despite a constant current source of 100µA, we can still see a sharp fall in the g_m when temperature increases. Therefore, to prevent this negative coefficient effect from setting in, a constant g_m bias circuit is essential to maintain the performance of the LNA. In fact, we have taken down the S_{21} and *NF* when the LNA is performing in *TT*, *SF* and *SS* mode. The results are recorded in Table II. It can be observed that as temperature increases and process becomes slower, the performances of LNA degrade faster for a current source configuration than a constant bias $\mathrm{g_m}$ circuit configuration. In fact, if we choose a current source configuration for the same LNA design, for *SS* analysis, our S_{21} would have worsened by 0.6 dB and *NF* would have increased by 0.03 dB. In the next section, we shall investigate the performance of the LNA circuit under different state condition. Basically the parameters which we will be using as a gauge of performance will be the S_{21} and *NF* of the LNA.

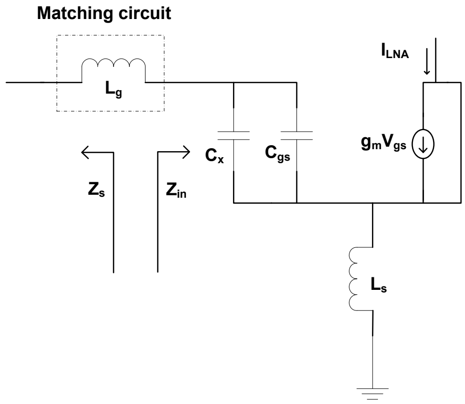

Fig. 4 Small-signal equivalent circuit of the LNA shown in Fig. 2

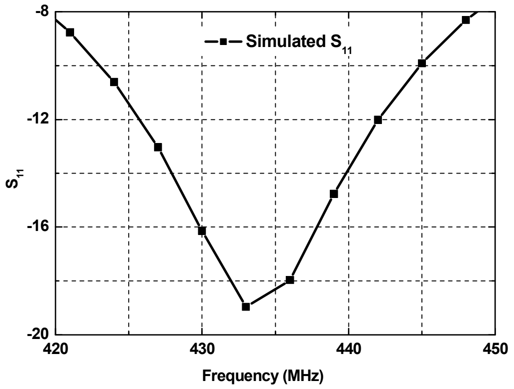

Fig. 5 Simulated input return loss (S_{11})

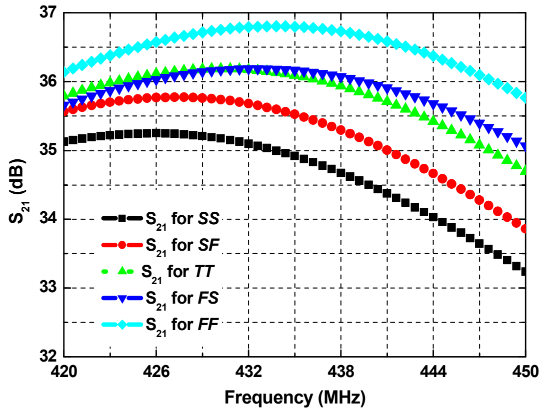

Fig. 6 Simulated S_{21} of the LNA for temperature sweep

TABLE III
GAIN AND NOISE FIGURE VARIATION FOR DIFFERENT STATES

State	*S_{21} % change*	*NF % change*
SS	*-3.10*	18.71
SF	*-1.44*	9.68
TT	*0*	0
FS	*0.08*	-5.81
FF	*1.77*	-11.61

III. LNA CIRCUIT SIMULATIONS

The LNA is designed to match at a RF frequency of 433 MHz, with a low noise and low power consumption. To achieve a good input match of < -10 dB for the LNA, the input impedance of the LNA is matched closely to 50 Ω. Since an inductive degeneration cascade LNA topology is often used to provide high gain, low noise and high isolation [2]-[3], such structure is being used for our investigation. Inductor L_s of Fig. 2 will determine the input impedance, Z_{in}, of the LNA. Z_{in} can be expressed by (3),

$$Z_{in} = sL_S + \frac{1}{sC_T} + \frac{g_m L_S}{C_T} \tag{3}$$

where C_T is the sum of C_x and C_{gs} of Fig. 4 and L_g is an off-chip inductor for matching purposes. Equation (3) can be derived based on the small-signal equivalent circuit of the LNA. According to [2], to optimize the performance of the LNA, we need to fix one of the design parameters of C_{gs}, V_{gs}, L_s and C_x, since the constant g_m bias circuit is able to generate a constant supply voltage of 0.62 V to the input of the LNA, we will keep the value of V_{gs} of transistor M1 of Fig. 2 at 0.62 V. By fixing it, we will be able to evaluate the value of the other design parameters.

V_{ctr} of the LNA design is used to control the gain of the LNA. For our investigation, V_{ctr} is kept high to keep *M1* and *M2* in deep saturation region. Fig. 5 shows the simulated S_{11} of the LNA with LNA operating in the high gain mode. The LNA is matched at a frequency of 433 MHz.

Simulations are then carried out for the LNA design where PVT are varied according to conditions in Table I. The S_{21} and *NF* are then plotted in Figs. 6 and 7 respectively. As we can see from the graphs, even with the wide swing constant g_m bias circuit, there is a fall in S_{21} and degradation in the *NF* of the LNA. The percentage variations of the S_{21} and *NF* of different states from *TT* for different PVT are then complied. The S_{21} is eventually concluded at a percentage variation of between -3.1 % to 1.77 % and the *NF* is concluded with a percentage variation of between -11.61 % to 18.71 %.

The existence of the percentage variation for $S_{21}$and *NF* can actually be understood from the gain of the LNA, G_mR_{Load}. Looking at this equation, the gain of the LNA is actually not purely affected by the g_m of transistor *M1*; in fact the value of R_{Load} of the LNA (Fig. 2) will also affect the gain. R_{Load} is temperature dependant and we can understand this through (4)

$$R_{Load} = R_0\left[1 + \alpha\left(T - T_0\right)\right] \tag{4}$$

where R_{Load} is the resistance value of the load resistor of the LNA, R_0 is the resistor value at room temperature, α is the temperature coefficient of resistance, T is the temperature and T_0 is the room temperature. Since the temperature coefficient is positive in this case, we will expect the value of R_{Load} to decrease with temperature and performance of LNA circuit to worsen.

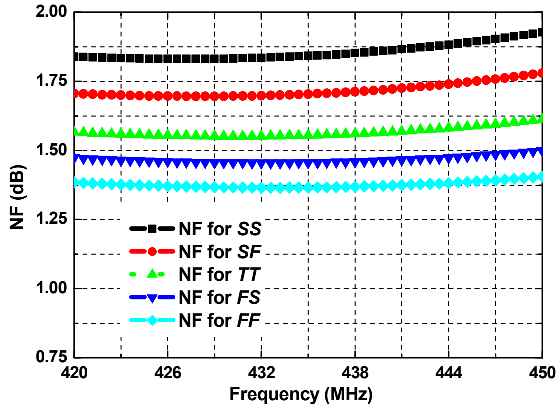

Fig. 7 Simulated *NF* of the LNA for temperature sweep

IV. CONCLUSION

This paper has investigated a wide-swing constant g_m bias circuit and verification has been made to show the feasibility of the circuit in maintaining a relatively good constant g_m value when PVT is varied. Though the constant g_m circuit is able to achieve a reasonable good gain and low noise figure when PVT is varied, a better gain and noise figure performance may be achieved for the LNA circuit if a PTAT current generator or on-chip resistor is used.

By using a PTAT current generator to generate the bias voltage [4] for the circuit, we can increase the G_m of the LNA by the same percentage as the decrease in R_{Load} due to temperature increment; this will ensure us to sustain the gain for the LNA. Furthermore, for this study, an external on-chip variable resistor is used for adjustment of g_m value for the constant g_m bias circuit, according to [5], an on-chip resistor is actually less susceptible to power supply variation. Therefore, an on-chip structure may be another alternative to maintain a more stable g_m. By doing so, we may be able to improve on maintaining the performance of the circuit.

ACKNOWLEDGMENT

The authors would like to thank Ms. Josephine Jesalva Fernandez for layout support. The authors would also like to acknowledge Mr. Yoshihiko Tezuka from Nagano Japan Radio Co., Ltd., Japan and Mr. Atsushi Tamura from Cubic Micro KK, Japan for the technical discussions.

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