

Interconnect Analysis of a Novel Multiplexer Based Full-Adder Cell for Power and Propagation Delay Optimizations

G.Ramana Murthy, C.Senthilpari, P.Velraj Kumar, Lim Tien Sze

Abstract—The proposed multiplexer-based novel 1-bit full adder cell is schematized by using DSCH2 and its layout is generated by using microwind VLSI CAD tool. The adder cell layout interconnect analysis is performed by using BSIM4 layout analyzer. The adder circuit is compared with other six existing adder circuits for parametric analysis. The proposed adder cell gives better performance than the other existing six adder circuits in terms of power, propagation delay and PDP. The proposed adder circuit is further analyzed for interconnect analysis, which gives better performance than other adder circuits in terms of layout thickness, width and height.

Keywords—Full Adder, Interconnect Analysis, Low-Power, Multiplexer, Propagation Delay, Parametric Analysis.

I. INTRODUCTION

INTERCONNECT design and analyses of VLSI circuits are challenging tasks in terms of Ultra Deep Sub Micron (UDSM) feature size. This capability is primarily due to the inherent heterogeneity of these systems, where different fabrication processes. In these diverse systems, global interconnect, such as clock and power distribution, grow in importance. The signal switching on the topmost metal layer of a digital plane can produce a noise spike. Interconnect design has become a dominant issue in high-speed integrated circuits (ICs), with the decreased feature size of CMOS circuits. As on-chip inductance becomes important, some wire optimization algorithms have been enhanced to consider RLC impedances [1]. In this paper, the trade-off between signal propagation delay and transient power dissipation in sizing of long interconnect driven by the proposed adder cell is discussed. In the circuit layout both line inductance and short-circuit power are considered. The minimum power delay product is used as a criterion to size long interconnects. A new criterion, the Power-Delay-Area-Product (PDAP), is introduced as efficient criterions to size interconnect within the adder cell.

G. Ramana Murthy is with the Multimedia University (Melaka) Faculty of Engineering & Technology, 75450 Melaka, Malaysia (phone: +606 252 3303; fax: +606 231 6552; e-mail: ramana.murthy@mmu.edu.my).

C. Senthilpari is with the Multimedia University (Melaka) Faculty of Engineering & Technology, 75450 Melaka, Malaysia (phone: +606 252 3926; fax: +606 231 6552; e-mail: c.senthilpari@mmu.edu.my).

P.Velraj Kumar is with the Multimedia University (Melaka) Faculty of Engineering & Technology, 75450 Melaka, Malaysia (phone: +606 252 3303; fax: +606 231 6552; e-mail: p.velraj@mmu.edu.my).

T.S. Lim is with the Multimedia University (Melaka) Faculty of Engineering & Technology, 75450 Melaka, Malaysia (phone: +606 252 3052; fax: +606 231 6552; e-mail: tslim@mmu.edu.my).

This paper discusses interconnection propagation delay, coupling details and shows why it is becoming more important to examine interconnection performance in VLSI circuits [2]. As circuit performance moves from transistor dominance to interconnection dominance, direct method simulators need to devote less time to costly non-linear transistor model evaluation. This direct method simulators (BSIM4) gives distributed elements of interconnections (Resistance, Inductance and Capacitance) must be broken into a series of discrete elements and an adding excessively to the limiting number of circuit nodes. Our proposed adder circuit gives 12 nodes due to Pass Transistor Logic (PTL) approach, which give lower interconnect effect with other existing adder circuit.

The proposed adder and other adder circuits are designed and simulated by PTL logic, for parametric, and interconnect analysis that can operate at ultra low-power supply voltage. Reducing the supply voltage and increasing the transistor count are the major obstacles for the design of adder cells which is eliminated in our proposed design. The proposed adder has very low short - circuit current and reduced transition activity compared with previously proposed low-power adders. A new multiplexer based adder cell is presented along with the existing circuits are simulated and the results of power dissipation, propagation delay, power-delay product, area efficiency are analyzed and compared. Proposed adder cell is compared for capacitance versus power dissipation and supply voltage versus power dissipation in parametric analysis with the existing designs. The new adder cell is also analyzed to identify the capacitance, inductance and resistance parameters of the layout for lower propagation delay and less power.

II. DESIGN METHOD OF THE PROPOSED FULL ADDER CELL

The proposed full adder circuit is designed by using multiplexing method and Boolean identities. After the simplification of Boolean identities the equations of sum and carry are as shown in (1) and (2). The simplest way of approach to the $A \oplus B$ is designed according to the multiplexer method. The exclusive of C input node which is directly fed to $A \oplus B$ generates the sum and its schematic form is shown in Fig.1 (a). According to carry (2), the $A \oplus B$ circuit and C input node are combined in the form of logical AND. The exclusive of this output node along with AB circuit generates the carry output according to (2) and its schematic form is shown in Fig. 1 (b). This circuit uses multiplexing method

efficiently to reduce the number of nodes to 12. The proposed full adder circuit eliminates power guard problem due to regular arrangement of transistor input nodes. Due to this, the proposed circuit gives low power dissipation, low propagation delay, and low PDP when compared to the widely used existing full adder circuits.

$$S = A \oplus B \oplus C \quad (1)$$

$$C_{out} = AB + (A \oplus B)C \quad (2)$$

A. Figures

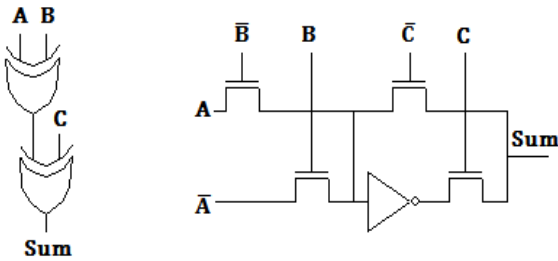


Fig. 1(a) Proposed multiplexer based full adder sum circuit

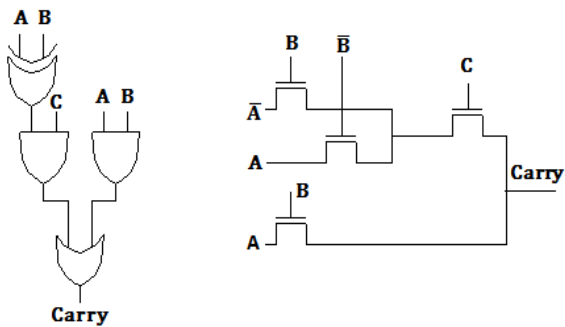


Fig. 1 (b) Proposed multiplexer based full adder carry circuit

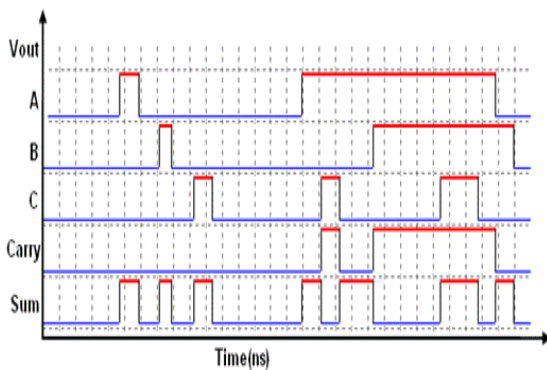


Fig. 2 Proposed multiplexer based adder timing diagram

A. Interconnect Analysis of the proposed full-adder cell

The proposed adder layout interconnect analysis is also analyzed for optimized power, propagation delay and area. The propagation delay can be measured by using the metal layer of resistance, inductance and capacitance. The

interconnect resistance of the proposed full adder cell decreases with increasing line width, increasing L_{int}/R_{int} the ratio between the line inductance and resistance. Due to wire sizing outperforms the VLSI circuit layout in RLC lines, the optimum heterogeneous wire interconnect expression for $h_{opt-RLC}(W_{int})$ [3] is as shown in (3)

$$h_{opt-RLC}(W_{int}) = \sqrt{\frac{R_o C_{int}(W_{int})}{R_{int}(W_{int}) C_o}} \frac{1}{[1 + 0.16(T_{L_{int}}/R_{int}(W_{int}))^3]^{0.3}} \quad (3)$$

Where

$$T_{L_{int}}/R_{int}(W_{int}) = \sqrt{\frac{L_{int}(W_{int})/R_{int}(W_{int})}{R_i C_i}} \quad (4)$$

C_i and R_i are the input capacitance and output resistance of a minimum size adder, respectively. $R_{int}(W_{int})$, $C_{int}(W_{int})$, and $L_{int}(W_{int})$ are the interconnect line resistance, capacitance, and inductance as functions of the interconnect width. An increase in the layout length and width increases the capacitance driven by the full adder cell. To drive a high capacitive load, a larger logic circuit is required to decrease the overall delay. The optimum proposed adder layout size depends upon interconnect values of R, L, and C is increasing function of line width. The transition of electric charge (input) depends upon interconnect signal [4]. The minimum signal propagation delay of an optimum adder system decreases with increasing line width as the total gate delay decreases. For an inductive interconnect layout the total signal propagation delay can be measured as shown in (5).

$$t_{pd-total}(W_{int}) = k_{opt-RLC}(W_{int}) t_{pd}(W_{int}) \quad (5)$$

where $t_{pd}(W_{int})$ is the signal delay of each RLC section as a function of the interconnect width.

To estimate the switching performance of the proposed full adder cell is to identify the most important lumped-element contributions to C_{out} . This quantity is estimated by the proposed full adder layout. The proposed full adder circuit load capacitance is its internal FET contributions, and represents the total external load capacitance. To estimate the low-to-high time t_{LH} [5] the (6) can be used with the exponential approximation

$$V_{out}(t) = V_{DD} [1 - e^{-t/\tau_p}] \quad (6)$$

which gives

$$t_{LH} \approx \ln(9) \tau_p \approx 2.2 \tau_p \quad (7)$$

According to (6) and (7) the proposed full adder circuit gives low propagation delay.

In the proposed full adder circuit when V_{IN} is at a stable logic 0 or logic 1 voltage level, either the nFET or the pFET is in cutoff mode. There is no direct current flow path through the transistors either nFET or pFET between the power supply

and ground [6]. In a realistic circuit, however, a small amount of quiescent leakage current I_{DDQ} flows across the reverse biased the drain-bulk regions due to push pull configuration of PTL logic. According to Roubik Gregorian [6] the maximum power supply current I_{max} occurs when $V_{IN} = V_T$ which is verified by noting that both the nFET and the pFET are saturated at this point.

The DC inputs neglect the fact that the output capacitor C_{out} can store electric energy. If we apply a pulsed voltage to the input, then the complete cycle will lead to an additional component of power dissipation that increases with increasing signal frequency f . The amount of transient power dissipated obviously depends upon the rate at which we switch the input, i.e., the signal frequency f .

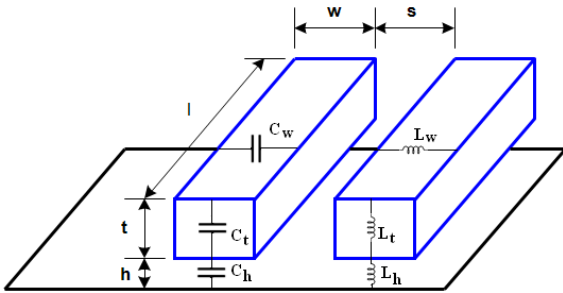


Fig. 5 Interconnect modelling of the substrate

III. RESULTS AND DISCUSSION

The proposed full adder and other six existing full adder circuits are schematized by using DSCH2 and their layouts are analysed by using Ultra Deep Sub Micron Process. The proposed full adder circuit is balanced for sum and carry due to the proper arrangement of transistors. The proposed full adder is further verified by Boolean identities and the results are shown in Fig.2. The worst delay for sum and carry are calculated by using the different combinations of inputs.

The full adder circuit performance depends on the transistor count as well as design concept. The CPL circuit is designed by using differential node concept uses 22-T [7], the power consumption and propagation delay is increased due to restoration concept. The XOR-10T [8] adder circuit suffers a problem of differential node in sum and carry circuits, due to this the power consumption and propagation delay is high. The mixed Shannon [9] and Shannon [10] circuits are designed by using MCIT and Shannon theorem technique. Due to this hybrid concept the sum and carry circuits produce NMOSFET drivability problem. The Shannon theorem based adder gives voltage swing restoration. Due to these problems the Shannon and mixed Shannon adder circuits consume high power and operate at low speed. The MUX-12T [11] adder circuit is designed by using multiplexer concept which has a complex node in its design. The drivability of input consumes high power to transmit the voltage level. The MCIT-7T [12] adder circuit is designed by multiplexing control input technique. The transient of input nodes consume more power which leads to high power consumption in the circuit.

IV. PARAMETRIC ANALYSIS

As technology scale leakage currents become increasingly large and must be taken into account to minimize total power consumption [13]. Once the magnitude and general shape of the curve has been examined, the measurements can be done using a linear scale for current. The proposed full adder is compared with the other six existing adders in parametric analysis at 90nm feature size such as capacitance versus power dissipation and voltage versus power dissipation by using BSIM 4, as shown in Fig. 3 and Fig. 4. The proposed adder gives lower power dissipation than CPL, XOR-10T, Mixed Shannon, Shannon, MUX-12T, and MCIT-7T circuits. The output node voltage makes a power transition, when load capacitance values are increased irrespective of supply voltage level. Generally, in digital CMOS circuits dynamic power is dissipated when energy is drawn from the power supply voltage to charge up which is clearly identified in Fig. 4. According to diode equation [14], the power in the circuits increases exponentially after the threshold voltage which is obeying ohm's law. The proposed circuit gives lower power dissipation when compared to other six existing circuits irrespective of the supply voltage. Thus, the proposed adder circuit can be used in lower power operating VLSI circuits.

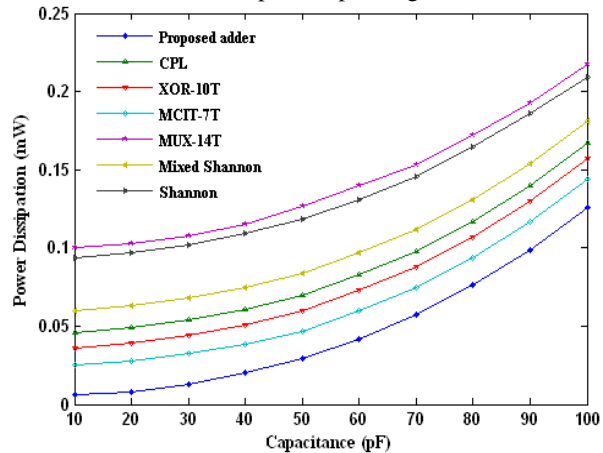


Fig. 3 Capacitance Vs Power dissipation for the proposed adder (90nm)

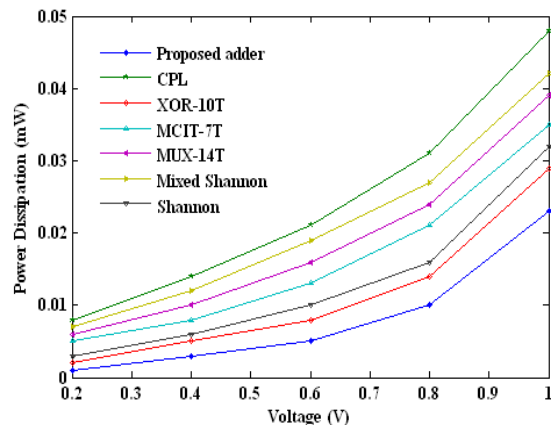


Fig. 4 Supply voltage Vs Power dissipation for proposed adder (90nm)

V. INTERCONNECT RLC PARAMETERS OF THE PROPOSED FULL ADDER LAYOUT

An integrated circuit is a set of patterned material layers that combine to form a 3-dimensional physical structure that are the electronic devices and interconnects [15]. In modern layout processing, 3 to 7 or more separate metal interconnect layers have become more common. In earlier days of MOS processing, aluminium (Al) was used exclusively for FET gates and interconnects examine the contributions to illustrate the optimal process. The output capacitance and its lumped parameters of the proposed adder layout are shown in Fig. 5 that are directly driven by the output node and also experience a change in voltage during a switching event.

A. Layout Capacitance of The Proposed Full Adder Cell

The proposed adder layout output capacitance can be obtained by examining the load presented to the output node during a switching event. Consider, the adder input is initially high, and then falls to a low value at time $t=0$. The side-wall, junction, bottom and fringe capacitances are charged up and its value is as shown in (9). All these capacitors mentioned charges from logic '0' volt to logic '1' volt

$$C_{out} = [(C_{GDn} + C_{GDp}) + (C_{DBn} + C_{DBp})] + [C_{line} + C_{FO}] \quad (9)$$

The proposed adder circuit is simulated to estimate the interconnect parameters of the layout by using BSIM analyser. The substrate thickness is varied from $0.04\mu\text{m}$ to $0.4\mu\text{m}$ while keeping its length, and height as standard fixed parameters. This paper mainly focuses on estimating the width capacitance (C_w), height capacitance (C_h) and thickness capacitance (C_t) while varying the thickness of the substrate to maintain the aspect ratio concepts [16]. The thickness capacitance decreases from 257.144 fF/mm to 88.214 fF/mm . The height capacitance increases from 75.46 fF/mm to 105.102 fF/mm . The width capacitance increases from 78.948 fF/mm to 109.074 fF/mm for the proposed adder circuit as shown in Fig. 6.

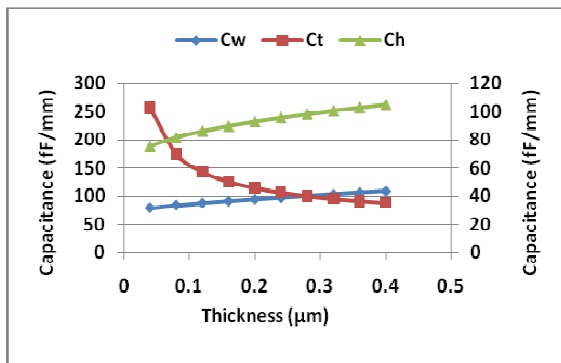


Fig. 6 Simulation results of interconnect capacitance for the proposed adder

B. Layout Resistance of the Proposed Full Adder Cell

The proposed adder parasitic resistance value of the layer is proportional to its length L and inversely proportional to its cross-section area A . The resistance of a rectangular conductor

can be expressed as shown in (10)

$$R = \frac{\rho L}{A} = \frac{\rho L}{HW} \quad (10)$$

where ρ is the resistivity of the material (in $\Omega\text{-m}$), L , W and H are length, width and height of the layout respectively.

This paper mainly focuses on estimating the width resistance (R_w), height resistance (R_h) and thickness resistance (R_t) while varying the thickness of the substrate to maintain the aspect ratio concepts. The thickness resistance decreases from $0.43\text{ }\Omega/\text{square}$ to $0.043\text{ }\Omega/\text{square}$ when the thickness is varied from $0.04\mu\text{m}$ to $0.4\mu\text{m}$ due to sheet resistance concept [17]. The variation in thickness of the substrate has no impact on height and width resistances as shown in Fig. 7.

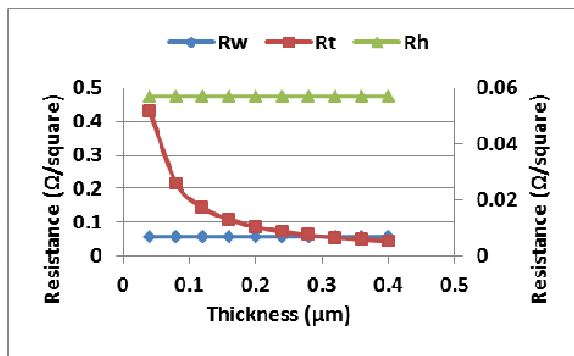


Fig. 7 Simulation results of interconnect resistance for the proposed adder

C. Layout Inductance of the Proposed Full Adder Cell

Consequences of on-chip inductance include ringing and overshoot effects, reflections of signals due to impedance mismatch, inductive coupling between lines, and switching noise due to Ldi/dt voltage drop [17]. The proposed adder circuit layout inductance of a section in a circuit can always be evaluated as shown in (11).

$$\Delta V = L \frac{di}{dt} \quad (11)$$

The inductance of the proposed full adder circuit is focused by varying the thickness of the substrate while keeping width and height as constant parameters. According to spacing and thickness concept, when the substrate current (I_{sub}) becomes large, inductance values are much desired while varying the thickness of the layout. The layout thickness is varied from $0.04\mu\text{m}$ to $0.4\mu\text{m}$ according to CMOS design rules. The simulation to estimate the interconnect inductance of the proposed adder is applied for 6 metal-layer, when the supply voltage is varied from (1V-2.5V) for 90-nm CMOS technology [16]. The thickness inductance (L_t) gradually decreases from 0.671 nH/mm to 0.416 nH/mm . The height inductance (L_h) increases from 0.067 nH/mm to 0.528 nH/mm due to thickness absorption ratio increase in the layout. The width inductance (L_w) decreases from 0.508 nH/mm to 0.437 nH/mm as shown in Fig. 8.

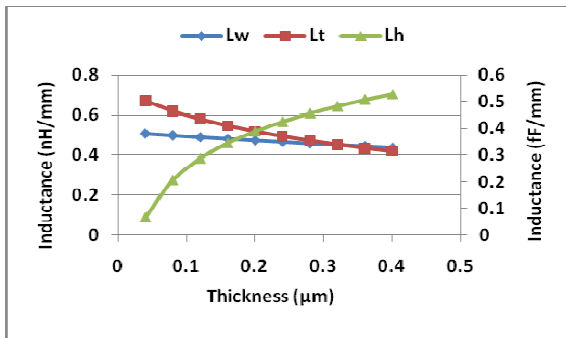


Fig. 8 Simulation results of interconnect Inductance for the proposed adder

Due to the increase in substrate layout current the interconnect inductance values also increases. If substrate currents are high in the layout the rate of change of current also increases at a constant bias-voltage. The inductive coupling between the parasitic layers increases according to mutual inductance concept.

VI. CONCLUSION

In this paper, a novel Multiplexer based full adder circuit has been proposed. The proposed circuit is designed by using DSCH 2 CAD tool and layouts are generated by using Microwind 2 CAD tool. The parametric and interconnect analyses are done by using BSIM 4 analyzer. The comparison for the proposed circuit has been carried out in terms the power consumption, propagation delay and power-delay product for circuit optimization. The proposed adder circuit is analyzed for the parametric analysis, the results shows better performance than other six existing adder circuits. Further, the proposed adder circuit is also simulated to estimate interconnect layout parameters which give a better performance at low voltage applications in terms of lower propagation delay and less power. The proposed adder circuit may be suitable to use at low voltage, high speed VLSI interconnect circuits.

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