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Implemented 5-bit 125-MS/s Successive Approximation Register ADC on FPGA

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***Abstract*—**Implemented 5-bit 125-MS/s successive approximation register (SAR) analog to digital converter (ADC) on FPGA is presented in this paper.The design and modeling of a high performance SAR analog to digital converter are based on monotonic capacitor switching procedure algorithm .Spartan 3 FPGA is chosen for implementing SAR analog to digital converter algorithm. SAR VHDL program writes in Xilinx and modelsim uses for showing results.

***Keywords*—**Analog to digital converter, Successive approximation, Capacitor switching algorithm, FPGA

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to digital converters (ADCs) require several comparison cycles to complete one conversion, and therefore have limited operational speed. SAR architectures are extensively used in low-power and low-speed (below several MS/s) applications. In recent years, with the feature sizes of CMOS devices scaled down, SAR ADCs have achieved several tens of MS/s to low GS/s sampling rates with 5-bit to 10-bit resolutions [1],[2]. Successive approximation register (SAR) converters offer the combination of resolution and speed unmatched by delta-sigma,pipeline or flash type ADCs. SAR's have no latency, and can be multiplexed. Furthermore, the power consumption is relatively low. These features make SAR converters suitable for data acquisition and fiber-optic applications [3]. The main reason ,which limited SAR resolution and speed,is comparison cycles to complete one conversion. Monotonic capacitor switching procedure algorithm as compared to conventional algorithm uses less comparsion cycles.This paper proposes implementing a capacitor switching procedure algorithm on FPGA to show industrial applications of this method.

II. Conventional SAR Architecture

A successive approximation ADC works by using a digital to analog converter (DAC) and comparator to perform a binary search to find the input voltage.A sample and hold circuit (S&H) is used to sample the analog input voltage and hold the sampled value whilst the binary search is performed. The binary search starts with the most significant bit (MSB) and works towards the least significant bit (LSB).For a 8-bit output resolution, 8 comparsion cycles are needed in binary search ,taking a least 8 clock cycles.

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The sample and hold circuit samples the analog input on a rising edge of sample signal.The comparator output is a logic 1 if the sampled analog voltage is greater than the output of DAC, 0 otherwise. Figure 1 shows SAR algorithm based on binary search over DAC output.

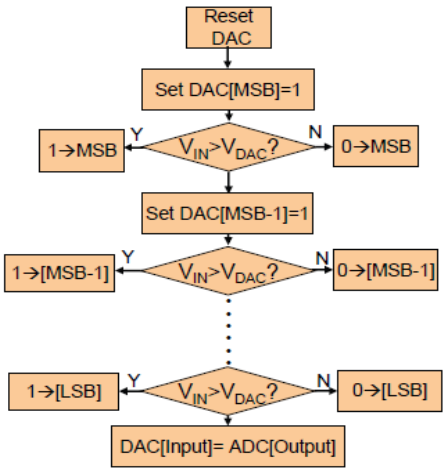

Fig. 1 SAR ADC algorithm block diagram [4]

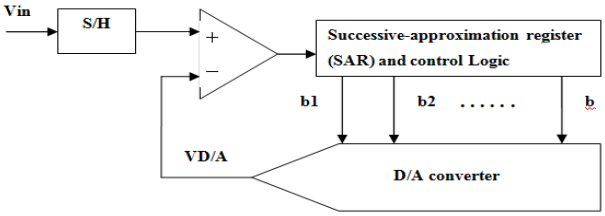

Fig. 2 SAR architecture

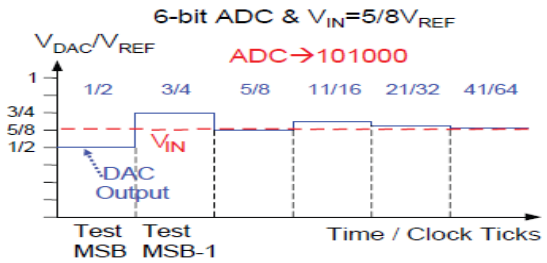

Fig. 3 Examlpe of 6-bit SAR ADC [4]

III. Proposed SAR Architecture

Figure 4 shows the proposed SAR ADC, where the proposed Switching procedure can be either upward or downward.

For fast reference settling, discharging through n-type transistors, downward switching was selected in this ADC. The proposed ADC samples the input signal on the top plates via bootstrapped switches, which increases the settling speed and input bandwidth. At the same time, the bottom plates of the capacitors are reset to $Vref$. Next, after the ADC turns off the bootstrapped switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor $C1$ on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer,resulting in samaller power dissipation.This proposed SAR ADC uses less compaton cycles as compared to conventional SAR [5].

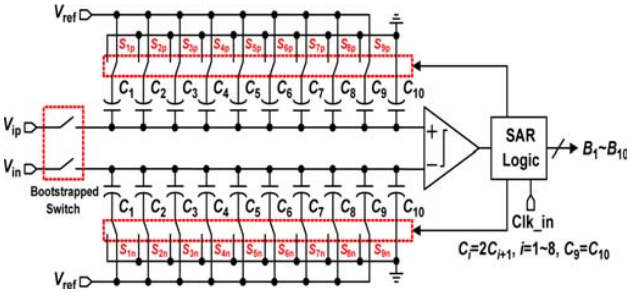

Fig. 4 Proposed SAR architecture [5]

IV. Implemented Specifications

FPGA specification:
Family : Spartan 3
Device : XC3S50
Package: PQ208

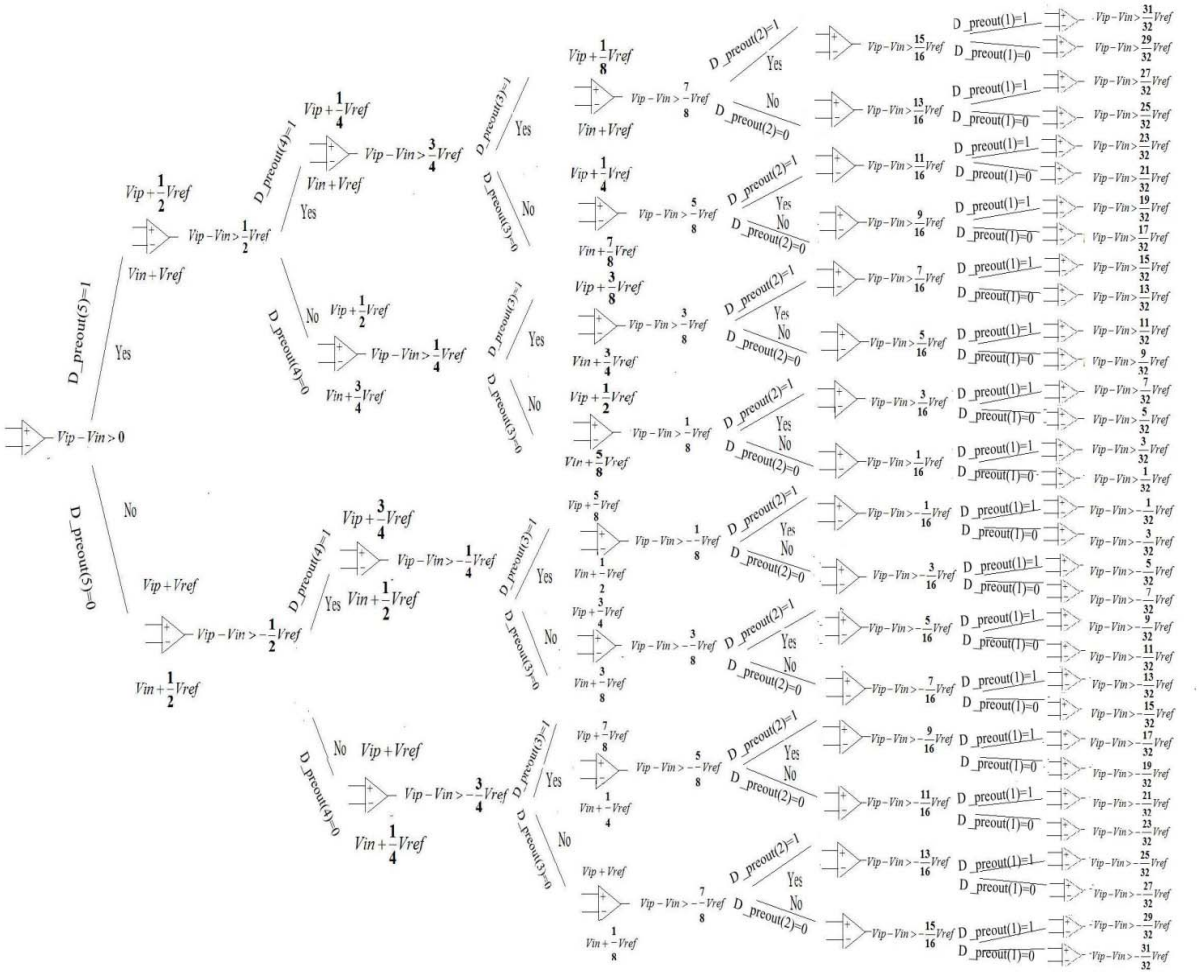

Fig. 5 SAR algorithm implemented on FPGA

Figure 5 displays the SAR algorithm (based on proposed SAR acrchitecture as showen in Fig.4) witch implemented on FPGA.

Digital sinusodial voltage has been created with lookuptable for input voltage in testbench.Figure 6 shows SAR ADC block diagram witch implemented on FPGA.

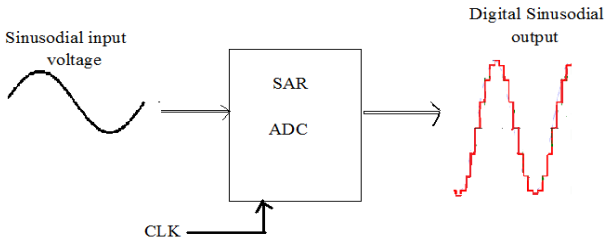

Fig. 6 Implemented SAR ADC Block diagram

For Simplicity in simulation, sinusodial input voltage shifts to achieve positive input amplitude as figure 7 shows. Therefore top side of SAR algorithm (Top side in Fig 5) is needed to implement.

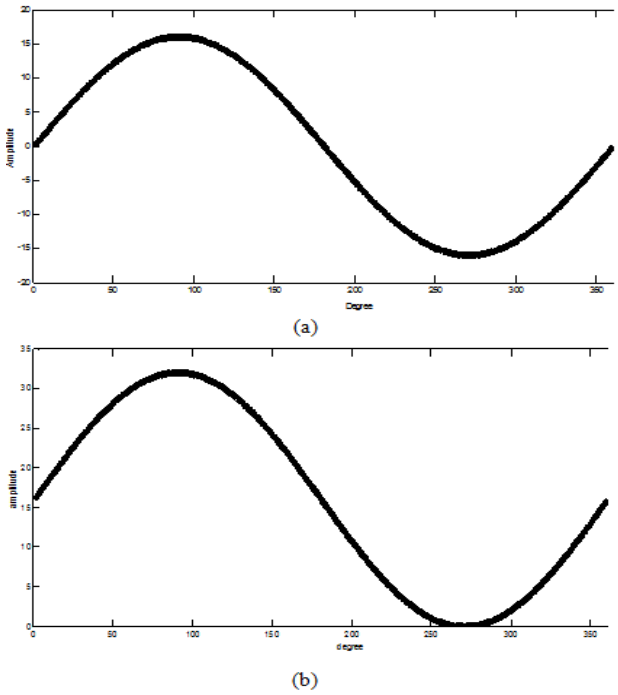

Fig. 7 a)Sinusodial input voltage without shift b)Sinusodial input voltage with shift

V. Simulation Results

SAR ADC VHDL program synthesis in Xilinx and Simulation results represent in figure 8 to 10. Modelsim and Xilinx Isim used to show final results.

VI. Conclusion

The proposed SAR analog to digital converter (5-bit and 125MS/s) has been successfully simulated. Monotonic capacitor switching procedure algorithm implemented on spartan3 FPGA.Simulation results in Xilinx Isim and modelsim express that , this algorithm Can be used in industry.The reviewer can develop proposed algorithm (Fig 5) to achieve high resolution and , with decreasing clock cycles high speed is obtainable.

Acknowledgment

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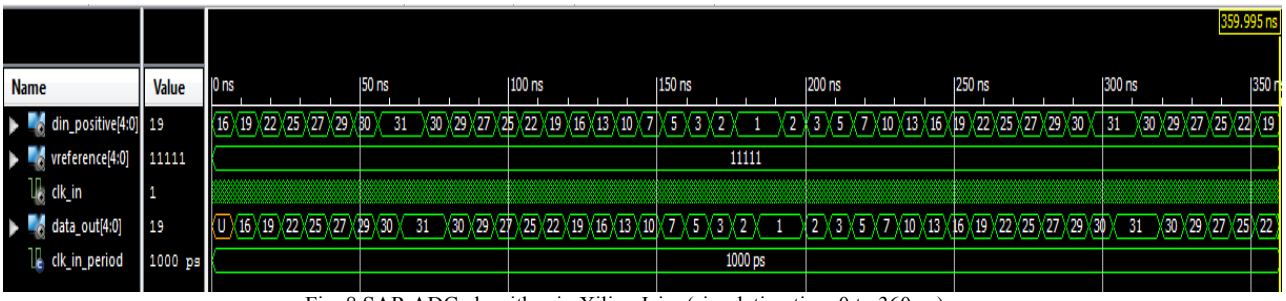

Fig. 8 SAR ADC algorithm in Xilinx Isim (simulation time 0 to 360 ns)

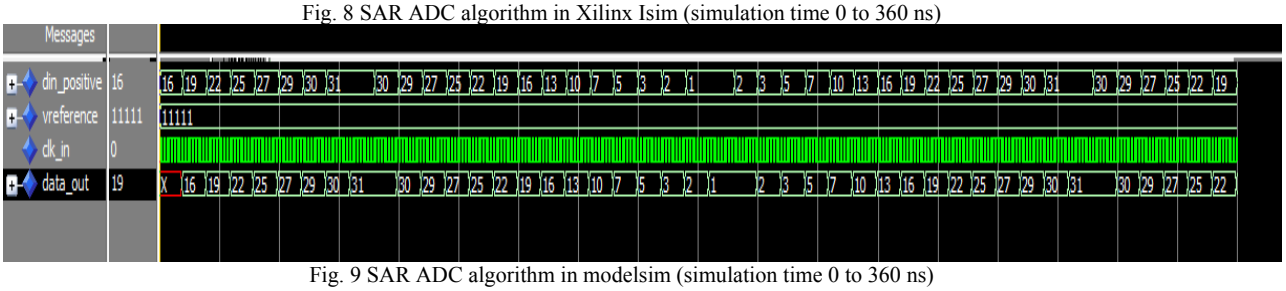

Fig. 9 SAR ADC algorithm in modelsim (simulation time 0 to 360 ns)

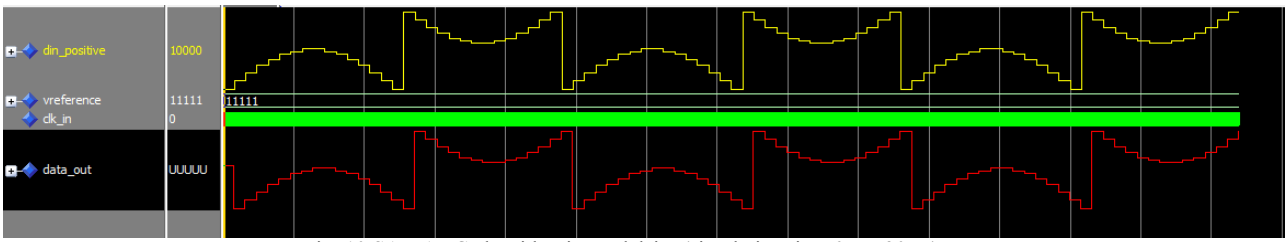

Fig. 10 SAR ADC algorithm in modelsim (simulation time 0 to 720 ns)

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