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High-Speed High-Gain CMOS OTA for SC Applications

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Abstract**—**A fast settling multipath CMOS OTA for high speed switched capacitor applications is presented here. With the basic topology similar to folded-cascode, bandwidth and DC gain of the OTA are enhanced by adding extra paths for signal from input to output. Designed circuit is simulated with HSPICE using *level 49* parameters (BSIM 3v3) in 0.35µm standard CMOS technology. DC gain achieved is 56.7dB and Unity Gain Bandwidth (UGB) obtained is 1.15GHz. These results confirm that adding extra paths for signal can improve DC gain and UGB of folded-cascode significantly.

Keywords**—**OTA (Operational Transconductance Amplifier), DC gain, Unity Gain Bandwidth (UGBW)

I. Introduction

IN design of most closed loop systems, design of the OTA is most challenging unit from design perspective. It has to achieve high DC gain and low thermal and flicker noise, also high band width required for systems with high frequency clock, especially in switched capacitor applications. Additionally, power consumption of the OTA is one of critical issues for applications with low power consumption target. Slew-rate and input common mode range are other important aspects of the OTA [1]. Telescopic and folded-cascode structures are two common structures for single stage op-amps. Two main drawback of first one are low input common mode range and large voltage headroom in output and main drawbacks of folded one is higher power consumption and lower UGBW. In this work to benefit high input common mode range of folded-cascode and also having higher DC gain and UGBW, total transconductance of the amplifier is increased adding extra paths for signal from input to output [2]. Other techniques for increasing DC gain of the op-amp such as using positive feedback or gain boosting are based on increasing output resistance of the op-amp and so only DC gain of the op-amp increases with these techniques and UGBW remains constant [3]-[4]. This paper is divided into flowing parts. A brief review for conventional folded-cascode OTA is given in section 2, in section 3 proposed multipaths OTA is analyzed. Simulation results are indicated in section 4 and section 5 concludes paper.

II. Foled –cascode OTA

Fig. 1 shows schematic of a folded-cascode amplifier in the differential mode. Because of wide applications of this topology its analysis is performed in many references [5]-[6].

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The DC voltage gain of the op-amp is obtained as equation (1) where, G_m is total transconductance of the amplifier.

$$A_v = G_m . R_{out} \tag{1}$$

$$G_m = g_{m1} \cdot \left(\frac{r_{o2}}{g_{m3}^{-1} + r_{o2}} \right) \tag{2}$$

$$R_{out} = (g_{m3} r_{o3} (r_{o2} \parallel r_{o1})) \parallel (g_{m4} r_{o4} (r_{o5} \parallel r_{o6})) \tag{3}$$

Unity gain bandwidth of the op-amp is in the equation below.

$$w_u = \frac{G_m}{C_{out}} \cong \frac{g1}{C_{out}} \left(\frac{r_{o2}}{g_{m3}^{-1} + r_{o2}} \right) \tag{4}$$

Where C_{out} is output capacitance and is equal to equation (5)

$$C_{out} = C_{d3} + C_{d4} + C_L \tag{5}$$

Phase margin of the op-amp mostly corresponds to the first and second poles of the op-amp which are calculated for discussed folded-cascode as equations (6) and (7). First pole located at the output node and second pole located at the CS node.

$$w_{p1} \cong \frac{1}{R_{out} C_{out}} \tag{6}$$

$$w_{p2} \cong \frac{g_{m3}}{C_{d1} + C_{d2} + C_{s3}} \tag{7}$$

III. Design of a Fast Settling OP-AMP

A. Basic topology

Main idea is to increase DC gain and UGBW of the OTA by increasing its total transconductance, in order to do this extra paths for signal from input to output is provided. Basic fully differential topology of the designed OTA is shown in Fig. 2. Two extra paths are provided in addition to the conventional folded-cascode. The first path is constructed by m3:m5 current mirrors (1: M) and the second one is constructed by m3:m4 current mirrors (1: N). Common mode feedback is applied to p-type transistors of m9 which are not located on signal path. Having extra paths for signal makes extra poles in transfer function of the amplifier. Capacitance of C_c are devised for neutralizing effect of critical pole which is closer to origin and so preparing feed forward compensation [6].

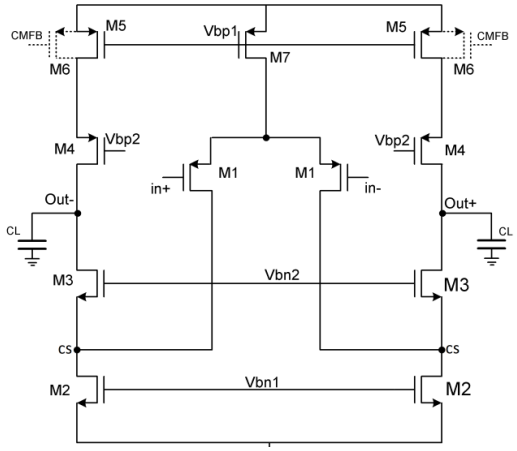

Fig. 1 Conventional folded-cascode OTA

B. Small signal Analysis

The voltage gain transfer function of the op-amp is obtained as

$$A_v(w) = G_m(w).Z_{out}(w) \tag{8}$$

Where the total transconductance of the op-amp denoted by $G_m(w)$ and achieved by adding transconductance of all the existing signal paths.

$$G_m(s) = \frac{Mg_{m1}}{(1+ {}^{s}\!/_{w_{py}})(1+ {}^{s}\!/_{w_{px}})} + \frac{g_{m2}}{(1+ {}^{s}\!/_{w_{py}})} + \frac{Ng_{m1}}{(1+ {}^{s}\!/_{w_{pz}})(1+ {}^{s}\!/_{w_{px}})} \tag{9}$$

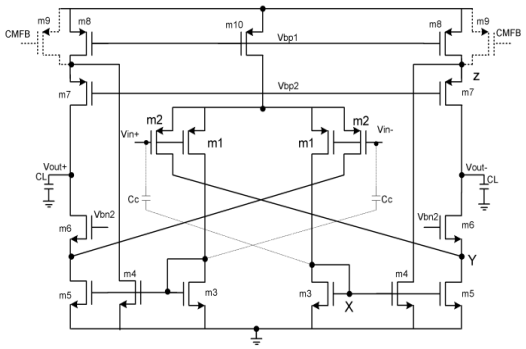

Fig. 2 Topology of designed OTA

Where

$$w_{px} \cong \frac{1}{R_x C_x} = \frac{g_{m3}}{(C_{d1} + C_{d3} + C_{g3} + C_{g4} + C_{g5})} \tag{10}$$

$$w_{py} \cong \frac{1}{R_y C_y} = \frac{g_{m6}}{(C_{s6} + C_{d5} + C_{d2})} \tag{11}$$

$$w_{pz} \cong \frac{1}{R_z C_z} = \frac{g_{m7}}{(c_{d8} + C_{d4} + C_{s7})} \tag{12}$$

are the poles associated with the nodes X, Y, and Z. In the equation (9) zeros due to gate-drain capacitance of m1-m5 is neglected since they are located on higher frequencies. Using the feed forward capacitance of C_c a left-hand zero is appeared on current mirror signal paths of m3:m4 and m3:m5 which equals to

$$w_{zc} = -\frac{g_{m1}}{C_c} \tag{13}$$

Proper selection of C_c according to (14), w_{zc} can cancel the effect of the w_{px} out and C_c obtained as equation (14).

$$C_c = \left(\frac{g_{m1}}{g_{m3}}\right).(C_{d1} + C_{d3} + C_{g3} + C_{g4} + C_{g5}) \tag{14}$$

Omitting w_{px} from equation (9) and doing some algebraic efforts equation (9) could be simplified as equation (15).

$$G_m(s) = \frac{(g_{m2} + (M+N)g_{m1})(1+ {}^{s}\!/_{w_{zph}})}{(1+ {}^{s}\!/_{w_{py}})(1+ {}^{s}\!/_{w_{pz}})} \tag{15}$$

$$w_{zph} = \frac{(g_{m2} + (M+N)g_{m1})(w_{py}w_{pz})}{(g_{m2} + Mg_{m1})(w_{py}) + Ng_{m1}w_{pz}} \tag{16}$$

Finally Z_{out} as an output impedance of the OTA can be obtained with

$$Z_{out} = \frac{R_{out}}{1 + R_{out}C_{out}s} \tag{17}$$

Where

$$C_{out} = C_{d7} + C_{d6} + C_L \tag{18}$$

$$R_{out} = \left(g_{m6}r_{o6}\left(r_{o5} \parallel r_{o2}\right)\right) \parallel \left(g_{m7}r_{o7}\left(r_{o8} \parallel r_{o4}\right)\right) \tag{19}$$

From above calculations DC gain and UGBW of the OTA achieves as equations (20) and (21), respectively.

$$A_v = (g_{m2} + (M+N)g_{m1}).(R_{out}) \tag{20}$$

$$w_u = \frac{g_{m2} + (M+N)g_{m1}}{C_{out}} \tag{21}$$

IV. Simulation Results

Three-path OTA and folded-cascode OTA have been designed in 0.35μm standard CMOS technology and simulated with HSPICE software. To have a fair comparison between folded-cascode and three-path OTA aspects load capacitances, size of input transistors and power consumption have been selected the same for both OTA. Fig. 3 shows layout of three-path OTA which occurs aria about 3060 μm^2.

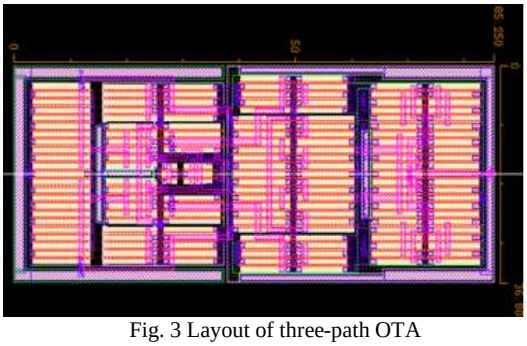

Fig. 3 Layout of three-path OTA

Table I lists specifications of folded-cascode and Three-path OTAs. In this table for both OTAs load capacitance is 1pF, input transistors size is equal to W/L=140µm/350nm and power consumption is 12.1 mw.

Variations of designed three-path OTA with process variations is shown in Fig. 7 which shows reduction about %22 in DC gain in FF corner and %15 in UGBW in SS corner also OTA shows slight variations in SF and FS corners. Output voltage swing of three-path OTA is 3 V_{p-p} for proposed OTA.

A routine setup is used as shown in Fig. 4 to evaluate the settling time of the OTAs. A step voltage with 0.3v amplitude is applied to the input in differential mode. Step responses of OTAs and closed look at step responses are shown in Fig. 5 and this figure is a clear evidence for faster settling time of designed OTA compared with folded-cascode. To test distortion of three-path OTA FFT analysis is done to output voltage in f=1 kHz and V_{op-p}=3v, output voltage spectrum is indicated in Fig. 6.

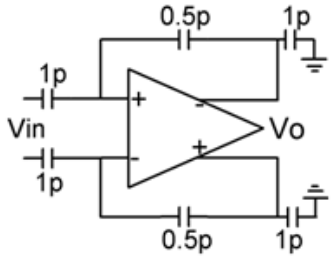

Fig. 4 Close-loop configuration for settling time testing

V. Conclusion

In this paper providing extra paths for input signal to output with the aim of increasing total transconductance of the OTA in fully differential mode has been done by adding two current mirror paths additional to cascode path. Consequently, with the same input transistors and same power consumption and load capacitance, DC gain and UGBW of the amplifier improved by three and two times, respectively.

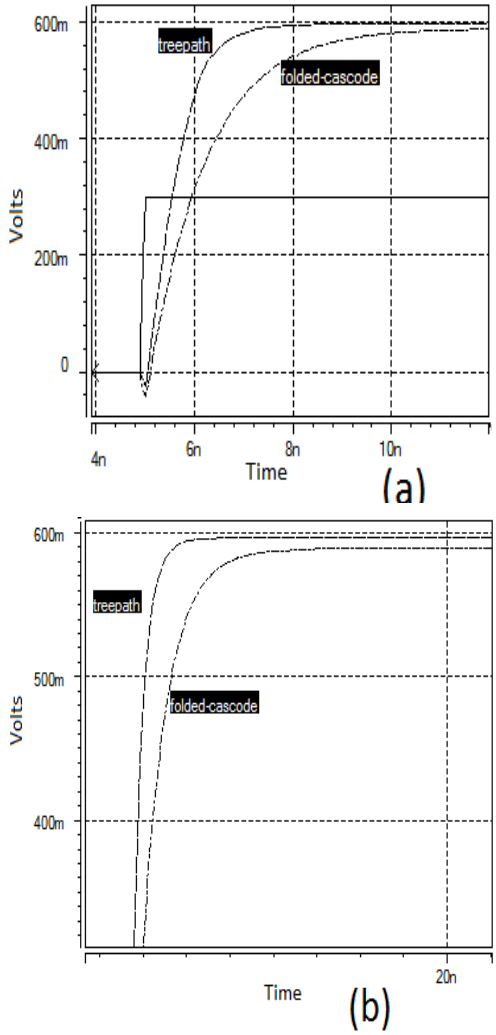

Fig. 5 (a) Step response of the three-path and folded-caascode (b) Closed look at step response

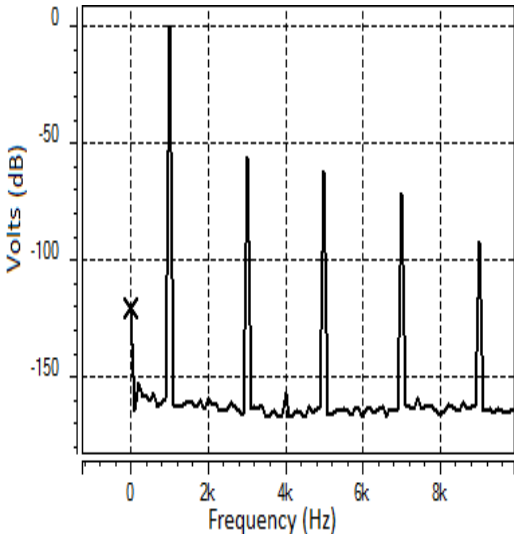

Fig. 6 THD in f=1 kHz and V_{op-p}=3v

TABLE I
SPECIFICATIONS OF FOLDED-CASCODE AND THREE-PATH OTAS

Parameter	Folded-cascode	Three-path
DC gain (dB)	47.4	56.7
UGBW (GHz)	574	1.15
Phase margin (°)	75	63
THD (f=1k,$V_{op\text{-}p=3v}$) (dB)	-63	-65

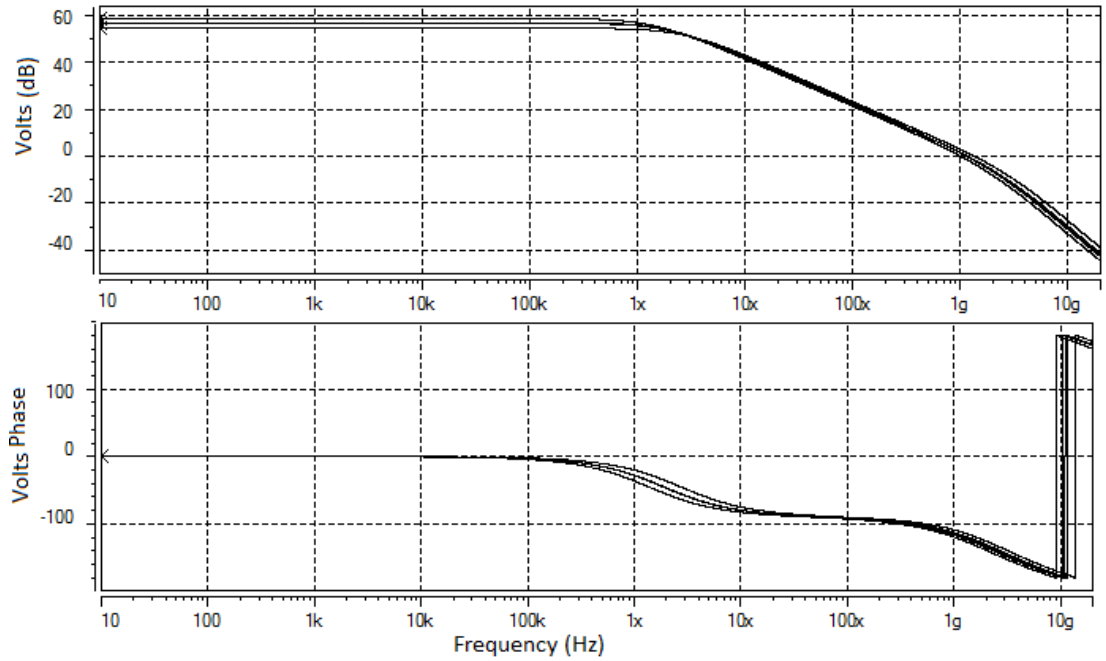

Fig. 7 Open loop Bode plot showing variations of three-path OTA with process corners (TT, FF, and SS)

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