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High Speed and Ultra Low-voltage CMOS NAND and NOR domino gates

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Abstract—In this paper we ultra low-voltage and high speed CMOS domino logic. For supply voltages below $500mV$ the delay for a ultra low-voltage NAND2 gate is aproximately 10% of a complementary CMOS inverter. Furthermore, the delay variations due to mismatch is much less than for conventional CMOS. Differential domino gates for AND/NAND and OR/NOR operation are presented.

Keywords—Low-Voltage, High-Speed, NAND, NOR, CMOS.

I. Introduction

In recent years, the power problem has emerged as one of the fundamental limits facing the future of CMOS integrated circuit design. The aggressive scaling of device dimensions to achieve greater transistor density and circuit speed results in substantial subthreshold and gate oxide tunneling leakage currents. Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits.

Depending upon the application, there are numerous methods that can be used to reduce the power consumption of VLSI circuits, these can range from low-level measures based upon fundamental physics, such as using a lower power supply voltage or using high threshold voltage transistors; to high-level measures such as clock-gating or power-down modes[1][2]. The power consumption in digital circuits, which mostly use complementary metal-oxide semiconductor (CMOS) devices, is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and thereby improve the circuit performance, the transistor threshold voltage must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage Vt results in significant increase in the subthreshold leakage current.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) and Low-Power (LP) logic [3]. However, in modern CMOS technologies there are significant gate leakages which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances, either poly-poly, MOS or metal-metal, to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [3]. There are several approaches to FG CMOS logic [4], [5]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [6].

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II. Ultra-low-voltage semi-floating-gate logic

The ULV logic styles presented in this paper are related to the ULV domino logic style presented in [7]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra loads represented by the floating capacitors are less than extra load given by increased transistor widths. The capacitive inputs lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay. The ULV logic styles may be used in critical sub circuits where high speed and low supply voltage is required. The ULV logic styles may be used together with more conventional CMOS logic. A ULV high speed serial carry chain [8] has been presented using a simple dynamic ULV logic [9]. In this paper we exploit an NP domino ULV static differential logic style.

The simple dynamic edge and level ULV inverters[7] are shown in Figure 1. Apply a clock signal to power the inverter, i.e. either ϕ to E_n to and V_{DD} to E_p, or $\overline{\phi}$ to E_p and GND to E_n and precharge to 1 or 0 respectively. The gate resembles NP domino logic. In order to hold the precharged value until an input transition arrives the E transistor connected to a supply voltage is made stronger than the other E transistor. The function of the inverter can be described as $\overline{O} = \overline{A}D$

The ON and OFF currents of a complementary CMOS inverter is given by the effective gate source voltages V_{DD} and $0V$ respectively. Assuming $\frac{Cin}{CT} = 0.5$ where C_T is the total capacitance seen by a floating gate, we may estimate the delay, dynamic and static power and noise margins of the different ULV logic styles relative to a complementary CMOS inverter.

A. Static Differential Ultra Low-Voltage Logic

The static differential NP domino ULV logic is shown in Fig. 2. If we apply ϕ to the E_n transistors and V_{DD} to the E_p transistors we precharge both outputs to logic 1 in the recharge mode, hence $B = \overline{B}$. The pMOS keepers will be turned off and the nMOS keepers will be turned on holding the initial recharge value of the nMOS transistor. The only way

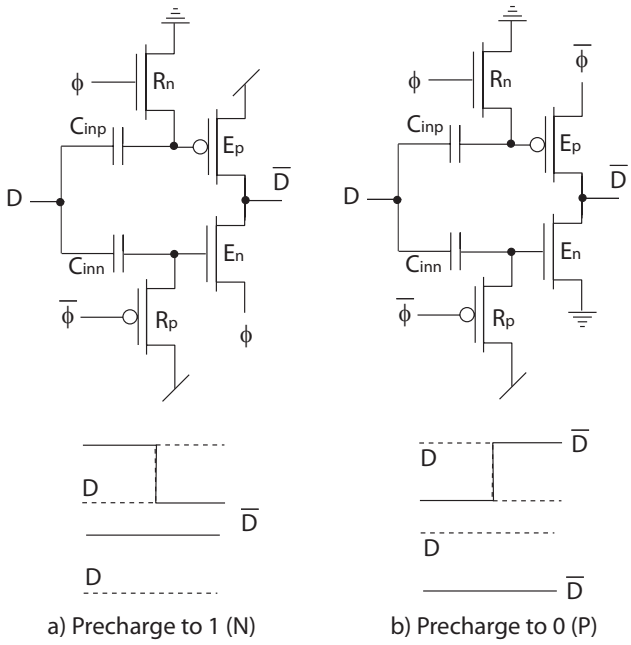

Fig. 1. *ULV domino inverters.*

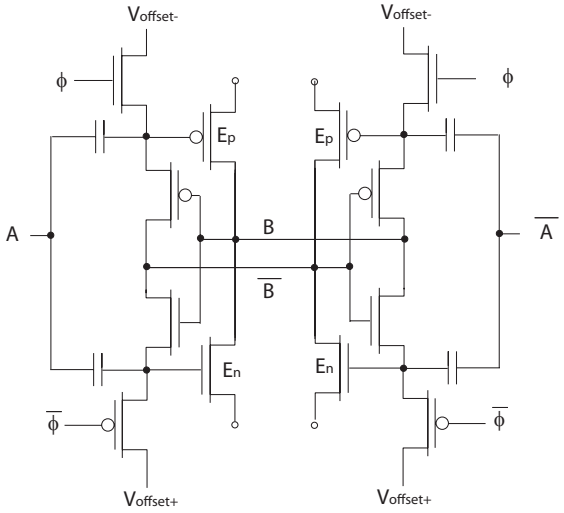

Fig. 2. Static differential ULV NP domino (SDNPU) inverter.

to turn the keepers ON is to pull one of the outputs towards 0. Furthermore, the SDNPU inverter is suitable for large logic depths. The good noise margin secures stable signal values with insignificant static power consumption.

The different configurations of static differential ULV logic inverters are shown in Fig. 3. By inverting the clock signals we obtain a latch configuration. The latched signal is available through a gate leaving the evaluation mode and entering the recharge mode. The edge created in the precharge process forces the next gate to respond to the edge and the output will be equal to the latched state. However, the delay of the first gate responding to a latched value will be large compared to the delay further down the chain. The reason for this increased

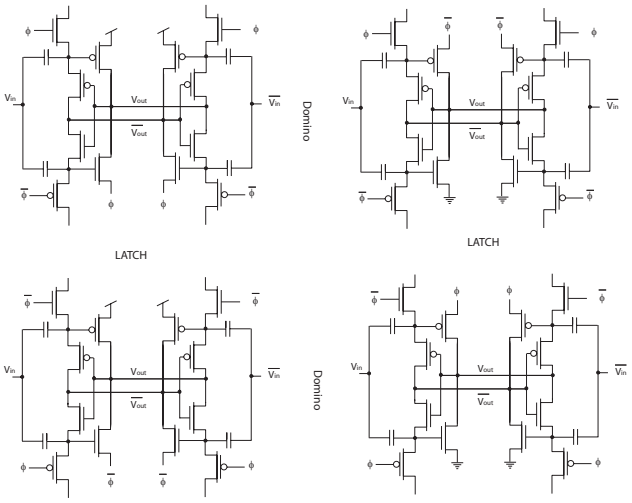

Fig. 3. Different configurations of static differential ULV logic inverters.

delay is the time required to precharge.

III. ULV AND AND NAND GATES

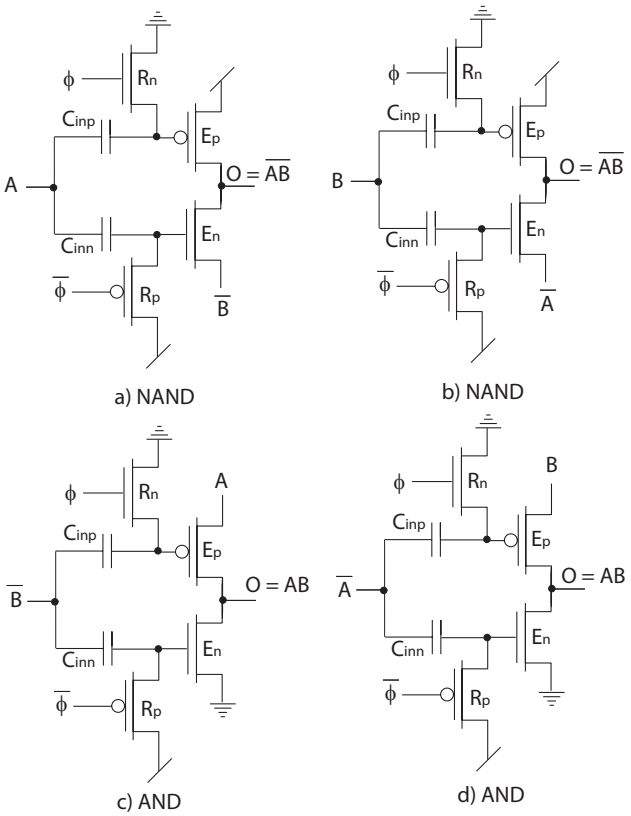

Fig. 4. *ULV domino AND and NAND gates.*

Different applications of the ULV domino inverter is shown Figure 4. The inverters can be used to implement AND2 and NAND2 functions by using one of the inputs to set the

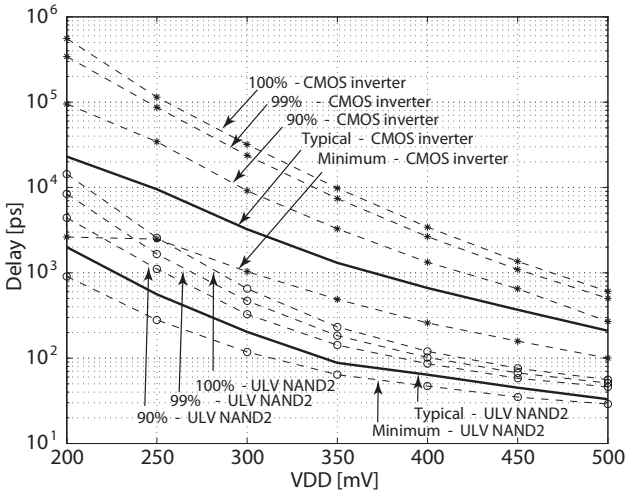

Fig. 5. *Delay variation due to mismatch for CMOS inverter and ULV NAND2 gate.*

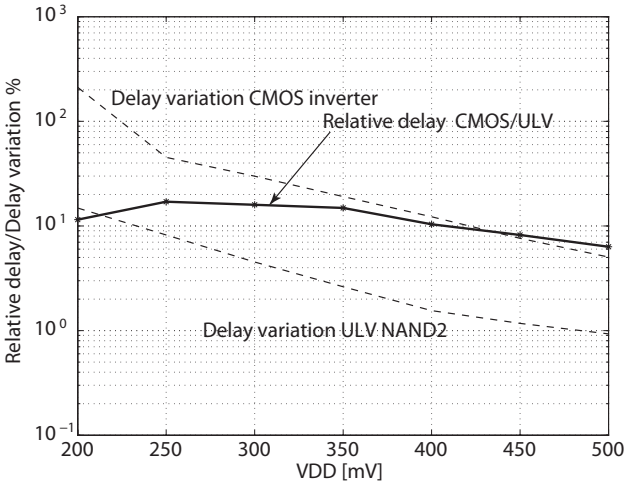

Fig. 6. *Relative delay CMOS inverter compared to ULV NAND2.* $\max(Delay) / \min(Delay)$ *are shown for CMOS inverter and ULV NAND2.*

precharge level. The gates in Figure 4 can be described as a pass transistor with an increased current level. The delay of the gates are dependent on the input delay. If we consider the gate in a) we observe that the evaluate transistor E_n acts as a pass transistor for the input $\overline{B}$ when $\overline{B}$ switches from 1 to 0 and the other input A switches from 0 to 1. The delay of the AND2 and NAND2 gates are less than 10% of a standard complementary inverter for supply voltages $400mV$ as shown in Figure 5. The typical delay for supply voltages ranging from $200mV$ to $500mV$ is shown. Monte Carlo simulations using 100 runs is performed and the maximum delay for 100%, 99% and 90%, and minimum delay for the ULV NAND2 gate and an CMOS inverter are shown. The delay variations is dependent on the current level, hence supply voltage. Due to the increased current level for the ULV logic the delay variations for the ultra low supply voltages is far less for the ULV logic compared to complementary CMOS logic.

Delay variation due to mismatch for CMOS inverter and ULV NAND2 gate is shown in Figure 6. The typical delay for a NAND2 ULV gate is less than 10% of a CMOS inverter and the delay variation is also significantly less than for complementary CMOS. For $V_{DD} = 300mV$ the delay variation for the ULV NAND2 and a complementary CMOS inverter can be expressed as $\max(Delay_{ULV-NAND2}) = 7 \min(Delay_{ULV-NAND2})$ and $\max(Delay_{CMOS}) = 32 \min(Delay_{CMOS})$ respectively. The relative delay CMOS inverter compared to ULV NAND2 and $\max(Delay) / \min(Delay)$ are shown in Figure 6.

The delay variation is proportional to the delay, i.e. current level, as shown in Figure 7.

ULV domino NOR/NAND gates can be implementet in different ways as shown in Figures 8 and 9.

IV. Conclusion

Different ultra low-voltage domino NAND and NOR gates have been presented. The ULV domino gates are high speed,

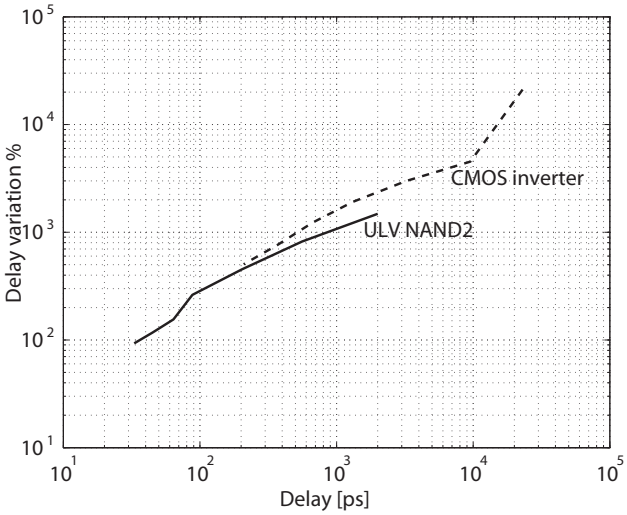

Fig. 7. *Delay variation as functions of delay.*

i.e. the delay compared to a CMOS inverter is less than 10%. The delay variation of the ULV gates due to process mismatches is much less than for a CMOS inverter operationg at the same supply voltage.

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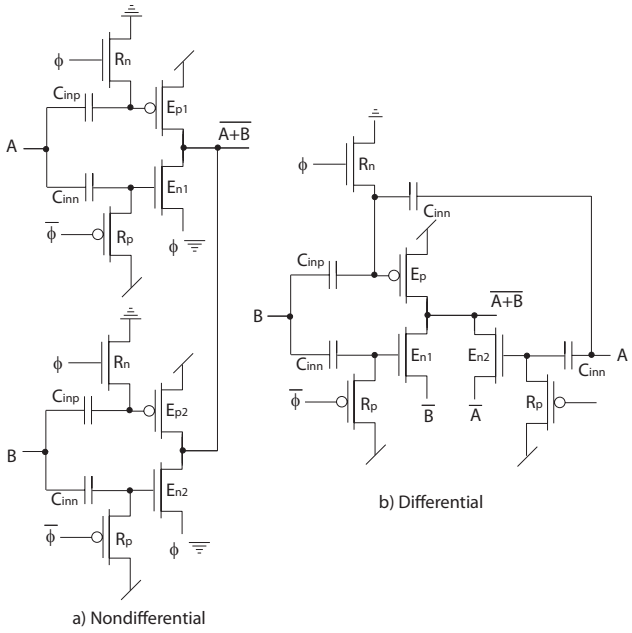

Fig. 8. *ULV domino NOR gates.*

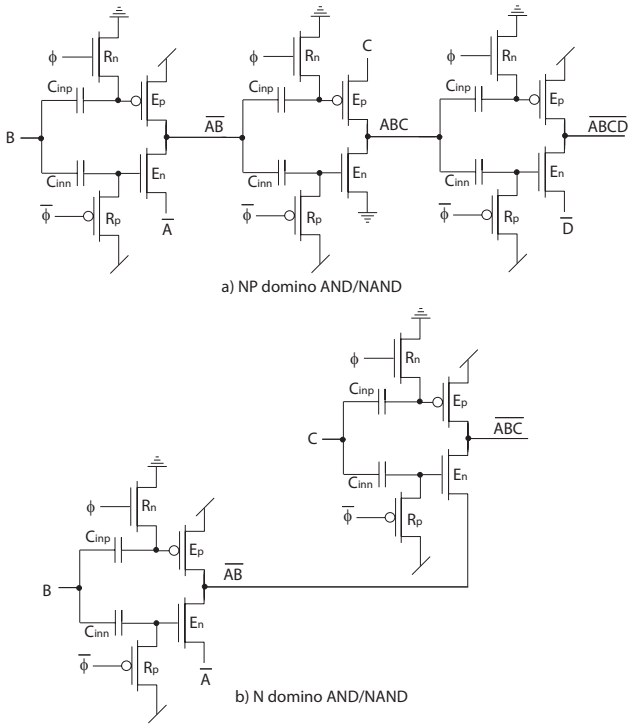

Fig. 9. *Different ULV domino AND/NAND gates.*

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