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Fabrication of Cylindrical Silicon Nanowire-Embedded Field Effect Transistor Using Al_2O_3 Transfer Layer

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***Abstract*—**In order to manufacture short gap single Si nanowire (NW) field effect transistor (FET) by imprinting and transferring method, we introduce the method using Al_2O_3 sacrificial layer. The diameters of cylindrical Si NW addressed between Au electrodes by dielectrophoretic (DEP) alignment method are controlled to 106, 128, and 148 nm. After imprinting and transfer process, cylindrical Si NW is embedded in PVP adhesive and dielectric layer. By curing transferred cylindrical Si NW and Au electrodes on PVP-coated p^{++} Si substrate with 200nm-thick SiO_2, 3μm gap Si NW FET fabrication was completed. As the diameter of embedded Si NW increases, the mobility of FET increases from 80.51 to 121.24 $cm^2/V{\cdot}s$ and the threshold voltage moves from –7.17 to –2.44 V because the ratio of surface to volume gets reduced.

***Keywords*—**Al_2O_3 Sacrificial transfer layer, cylindrical silicon nanowires, Dielectrophorestic alignment, Field effect transistor.

I. Introduction

ONE dimensional Si nanostructures including nanowire (NW), nanotube and nanobelt have been studied widely as a building block for semiconductor device in nanocale such as field effect transistors (FETs) [1], photosensors [2], solar cell [3], biosensors [4], light-emitting diodes [5], and so on due to their own physics or chemistry. In order to manufacture various nano-devices, researchers are supposed to solve fundamental and economic limitation of conventional fabrication process. Imprinting and transferring method have been researched and receiving much interest as one of the most popular technologies over the past decade because it has the advantages in high throughput, low cost and convenient fabrication. As one of the candidates for transfer media, Polydimethylsiloxane (PDMS) is widely used and researched in printing electronic field because it is soft and elastic so that devices on PDMS can be transferred onto aimed position by conformal contact. However, PDMS has a flaw that it absorbs organic solvent and swells up when it is exposed by organic solution. Photolithography, one of the representative methods to define electrodes, includes development and stripping process, which are using organic solvent such as acetone and methanol. It is hard to define electrodes on PDMS by photolithography because photo resist (PR) pattern or defined electrodes would be damaged or peeled off while PDMS are absorbing developer and stripper and swelling up.

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Here, we applied Al_2O_3 film for sacrificial transfer layer replacing PDMS block. Al_2O_3 with high dielectric constant is not damaged by alcohol used in dielectrophoretic (DEP) alignment process, one of methods to link NWs on electrodes, and is useful to form electric field between electrodes. Furthermore, the electrical properties such as mobility and threshold voltage change of fabricated FET by controlling the degree of embedded cylindrical Si NW into PVP of adhesive layer at the imprinting and transferring step were measured.

II. Experimental

In general, the method for the direct imprinting and fabrication of cylindrical Si NW FET by using Al_2O_3 as a sacrificial transfer layer consists of four processes. The first is preparation of Si NWs and transfer block, which is synthesis of p-type cylindrical Si NWs using diameter-controllable metal catalyst-assisted etching (MCE) method and dispersion these Si NWs in 99.9% ethanol. After then Al_2O_3 was deposited on flexible Polyimide (PI) substrate and short gap of Au electrodes were defined on Al_2O_3 layer by photolithography method. The second is alignment of single Si NW by DEP which allows Si NW to be addressed between defined Au electrodes on Al_2O_3 layer. The third and the last steps are preparation of PVP adhesive layer and imprinting for manufacturing transistor. PVP was spin-coated on commercial Si substrate with a 300 nm-thick SiO_2 and softly baked at 110°C for 10min. The fabrication of cylindrical Si NW FET was completed as Si NW and Au electrodes on Al_2O_3 were imprinted and transferred onto softly baked PVP layer. The flow sequence of entire process is depicted in Fig. 1. Si NWs were formed through diameter controllable MCE method using a p-type Si (100). This synthesis process of the Si NWs has been reported in our previous work [6]. The different process from previous method is that Au was additionally deposited on Ag layer/Si wafer by e-beam evaporator to enhance the adhesion between alloy nanoparticle which acts as catalyst and Si substrate instead using Ag layer alone. In order to modulate the diameters of cylindrical Si NWs, the thickness of evaporated Ag layer is controlled to 6 nm, 7 nm and 8 nm and 5 nm in the thickness of Au layer was individually deposited on Ag layer. The following processes from annealing process were conducted through same sequence to previous work. And the synthesized cylindrical Si NWs were dispersed in the solution of dilute hydrazine and 99.9% ethanol solution.

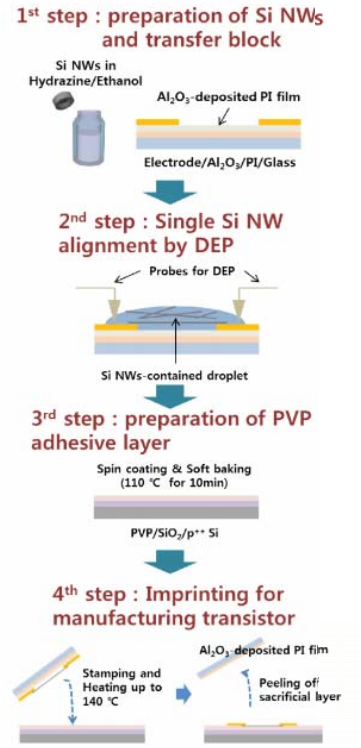

Fig. 1 The process flow sequence to imprinting and fabrication of circular Si NWs FET using Al_2O_3 layer as a sacrificial transfer layer

15 μm-thick PI film which wrapped the slide glass was prepared to be used as sacrificial layer. It was cleaned following standard cleaning step (99.9% acetone, 99.9% methanol and deionized (DI) water by sonication). And by using e-beam evaporator, 20 nm-thick Al_2O_3 was deposited on PI substrate. After then, PR solution (AZ5214E) was spin-coated on Al_2O_3-deposited PI substrate with 500 rpm for 5 s and 2500 rpm for 45 s and baked at 110 °C for 50. The exposure time was confirmed to 6 s and PR was developed in developer solution (AZ MIF 300) for 27 s. 40 nm-thick Au layer was deposited on PR pattern. By stripping process Au electrodes with gap of 3 μm were defined. After all, the surface of Au electrodes were cleaned by O_2 plasma treatment with power of 300 W, flow rate of 50 sccm, working pressure of 20 pa, and operation time of 5 min.

Prepared Si NWs (dispersed in hydrazine and ethanol solution) was linked between Au electrodes by DEP alignment method. After suspending a dispersion solution with Si NWs on Au electrodes, direct current (DC) bias with frequency of 1 kHz, amplitude of 10 Vpp, and pulse width of 500 μs was applied [7].

To prepare adhesive layer at third step in Fig. 2, 10 wt% Poly(vinlypyrrolidone)(PVP) was used as both a polymeric adhesive agent and dielectric layer for field effect transistor. It was coated with the condition of 500 rpm for 5 s and 5000 rpm for 120 s onto 300 nm-thick SiO_2/p^{++} Si substrate and softly baked at 110 °C for 10 min. To complete the fabrication of field effect transistor, prepared Si NWs and Au electrode on Al_2O_3 layer were attached on PVP layer and they were heated up to 140°C. After detaching Al_2O_3 layer from PVP layer, softly baked PVP was completely cured at 175°C for 1h.

III. Result and Discussion

When Ag single layer is deposited on Si substrate and annealed by RTA process, nanoparticles formed on substrate shows weak adhesion property and they easily move in the lateral direction when specimen was put into etching solution so that nanoholes cannot be formed vertically. To overcome this problem, RTA was performed in H_2 ambience and etching solution was cooled down to –20°C. However, the fundamental problem of poor adhesion property between Ag nanoparticles and Si substrate is not improved. In order to enhance the adhesion, in this paper, Au film was additionally deposited on Ag film and annealing process was conducted to form Au and Ag alloy nanoparticles. According to phase diagram of Ag-Au materials, Eutectic reaction occurs from 835°C [8]. This Eutectic temperature is beyond on RTA process temperature of 700°C so that Ag nanoparticles cannot form strong bonding with Si substrate. On the other hands, Au and Si show the property to form Eutectic phase at 363°C [9], which is lower than process temperature. If Au is used alone without Ag, Eutectic reaction occurs before forming regular hemi-spherical nanoparticles and random shapes of nanostructures are generated. That's why we designed Au on Ag double layer structure to form hemi-spherical particles with strong adhesion with Si substrate. Cylindrical Si NWs synthesized with 5 nm/6 nm in the thickness of Au/Ag film had the mean diameter of 108 nm as well as 5 nm/7 nm and 5 nm/8 nm in the thickness of Au on Ag films showed the mean diameters of 128 and 147.9.

Fig. 2 (a) shows the scanning electron microscopy (SEM) (JEOL, JSM 7001F) image of Au and Ag alloy nanoparticles on Si substrates after annealing process with 5 nm/7 nm in the thickness of Au and Ag film and Fig. 2 (b) indicates A statistical diameter distribution of Ag-Au alloy nanoparticles in Fig. 2 (a).

Furthermore, vertically aligned 40 μm-long Si NWs with a high aspect ratio (~800) were produced via a 3 h of the second MCE process and Fig. 2 (c) shows Si NWs synthesized with 5 nm/7 nm in the thickness of Au and Ag film.

After cutting these Si NWs, they were dispersed in the solution of dilute hydrazine and ethanol in order to prevent surface oxidation of Si NWs. The synthesized Si NW was characterized by using high-resolution transmission electron microscopy (HRTEM) (JEOL, JEM 2100F). Fig. 3 (a) indicates that Si NWs were produced along <100> direction. Also, Si NWs formed through MCE method has rough surface as shown in Fig. 3 (b) and it was confirmed that they were of single crystalline by the electron diffraction pattern as shown its inset.

Material used for transfer layer is supposed to have the characteristics of flexibility and Au electrodes can be easily peeled off from the material in order to form conformal contact and transfer electrodes and Si NWs in high yield when electrodes are contacted to adhesive layer. In this paper, Al_2O_3 film was used for sacrificial transfer layer which is rigid in bulk and is fragile rather than bendable when external strain is applied. In general, however, even though a material shows

rigid property, it turns to be flexible if the thickness of the material scale-downs to nano-unit. So 20 nm-thick Al_2O_3 film was deposited on PI substrate. And the thicknesses of PI substrate and Au-deposited on PR pattern/Al_2O_3 after photolithography process were optimized to 15 μm and 40 nm, respectively.

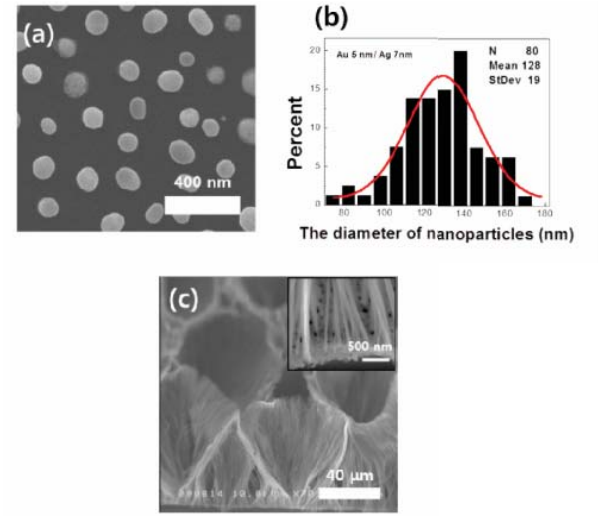

Fig. 2 (a) A top view SEM image of Au and Ag alloy nanoparticles after rapid thermal annealing with 5 nm/7 nm in the thickness of Au/Ag layer. (b) A statistical diameter distribution of Ag-Au alloy nanoparticles in (a). (c) 45°-tilted SEM images of typical Si NWs formed with 5 nm/7 nm-thick Au/Ag layer and the inset shows high magnified SEM image

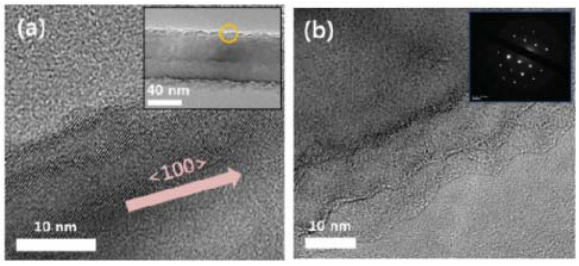

Fig. 3 (a) A TEM image of a single-crystalline with <100> direction (b) Rough surface of circular Si NW synthesized by MCE process

DEP process depends on the dielectric medium, the density of NWs in medium, the bias on-time and the strength of bias field. As mentioned above, Al_2O_3 was applied for sacrificial transfer layer and Au electrodes were defined on it. The electric field used for DEP process is supposed to be strongly formed between Au electrodes without leakage in other direction. Also, Al_2O_3 has a high dielectric constant of 9.0~10.1 in order not to permit leakage [10].

The solution affiliated with alcohol is widely used for dielectric medium. Al_2O_3 is not damaged by organic solvent so that the precise DEP can be conducted. As the density of Si NWs in medium solution, the number of Si NWs linked between Au electrodes per unit time gets increased, on the other hands, the bias on-time would increase to address the certain number of Si NWs on Au electrodes with dilute medium solution. The conditions for DEP were optimized in order for one or two of Si NWs to be aligned for 3 s. Fig. 4 (a) shows optical microscopy (OM) image the linked cylindrical NWs between Au electrodes with the 3μm.

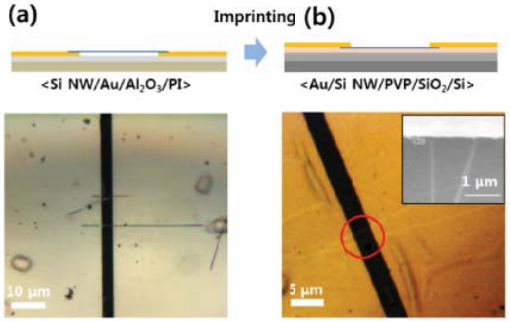

Fig. 4 (a) An OM image of Si NWs addressed on Au electrodes by DEP process. (b) An OM image of the transferred Si NWs and Au electrodes on to PVP adhesive layer and inset is the SEM image of Si NWs embedded in PVP layer and Au electrodes on it

The p^{++} Si substrate and the thermally oxidized 300 nm-thick SiO_2 were used for bottom gate and gate insulator, respectively, and PVP was applied as adhesive polymer to transfer Si NWs and Au electrodes defined on Al_2O_3 film. The ratio of PVP, PMCF, and PGMEA were optimized to 1 : 2 : 8 (v : v : v). In order to reduce the amount of generated solvent gas during baking process after transfer step, PVP layer coated on SiO_2 was softly baked. And then, Au electrodes and Si NW on Al_2O_3 film were flipped over and attached into PVP adhesive layer as shown in the fourth step of Fig. 1. With pressure of 0.8 kgf/cm^2, the specimen was heated up to 140°C in order for PVP layer to hold Au electrodes and Si NWs while the PVP was partially baked and the Al_2O_3-deposited PI substrate was detached. The adhesion force between Al_2O_3 and Au layer is weak and gets increases as temperature increases but the degree of adhesive strength is insignificantly changed as well as the bonding of PVP and Au electrodes is stronger as PVP is cured so that Si NWs and Au electrodes can transferred to PVP. Beyond 140 °C, PVP formed strong bonding not only electrode but also Al_2O_3 layer and PVP was partially peeled off during detachment of sacrificial transfer layer. After transfer process, the specimen was baked in vacuum at 175 °C for 1 h. Without keeping it in vacuum state, as mentioned above, the solvent gas generated from PVP solution is trapped between Au electrodes and adhesive polymer, which causes decline of contact property of Si NWs and electrodes. Fig. 4 (b) is the top view OM image of transferred Si NWs and electrodes on PVP layer and its inset is a SEM image of device which indicates that the cylindrical Si NWs were embedded in PVP Adhesive polymer layer.

To verify the feasibility of our process to a fabricate a short gap Si NW transistor with imprinting method using Al_2O_3 as sacrificial layer, single Si NW transistors with various diameters of 108, 128, and 148 nm were fabricated and their electrical properties were measured. From the top view SEM image and OM image in Fig. 4 (b) and its inset, the active

channel width and length of all the devices were confirmed. Channel lengths were fixed at 3 μm and channel widths of device were equal to diameters of Si NWs. Current-voltage (I-V) characteristics were measured by using an Agilent semiconductor parameter analyzer (model 4145B), with contacts to the devices made by using a probe station (Desert Cryogenics, model TTP4). The values of capacitances for gate dielectric were simulated by *Silvaco* along to the diameter of cylindrical Si NW embedded into PVP layer. The electrical property of p-channel transistor with 128 nm in the diameter of single Si NW was confirmed by transfer (I_{ds}-V_g) curve and the output (I_{ds}-V_{ds}) curve as shown in Figs. 5 (a), (b).

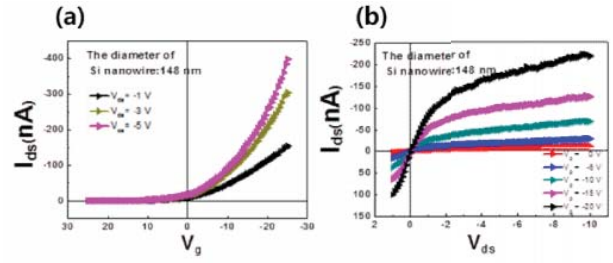

Fig. 5 (a) Transfer and (b) output characteristics Si NW transistor with a diameter of 128 nm

For field effect transistor with 128 nm in the thickness of Si NW, An on/off ratio of 2.01 x 10^4 was measured with the transconductance was measured to be 0.0067 μS at V_{ds} of –1 V and a threshold voltage (V_{th}) of –4.55 V. The p-type linear field-effect mobility (μ_h) was calculated by using $\mu_h = L/(W \times C_d \times V_{ds}) \times g_m$, where L is the gap distance between electrodes (this value is same as the length of Si NWs from source to drain), W is the channel width of the device equal to the diameter of Si NWs, C_d represents the capacitance per unit area of the gate dielectric whose value is 423.5 pF/cm^2, and g_m is transconductance. The mobility μ_h was 97.84 cm^2/Vs. The output characteristic was measured And I_{ds} increased as the applied V_g increased and was saturated as the V_{ds} increased, which means good Ohmic contact between Au electrode and Si NW and shows the performance of typical p-channel transistor. The mobility values were determined to be 80.51, 97.84, and 121.24 cm^2/V·s for diameters of 108, 128, and 148 nm, respectively. Si NWs synthesized through MCE method has rough surface as shown in Fig. 3 and the defects on surface disturb the flow of carriers in the device. In particular, as the diameter of Si NW is smaller, the ratio of surface to volume is larger and the effect of the surface roughness on the flow of carriers is more dominant, and it caused decrease in the mobility. Also, the surface roughness of cylindrical Si NW affected on the threshold voltage. Scattering effect caused by carrier trapping at the interface let the threshold voltage shifted in negative direction of enhancement mode. And the excess carrier concentration in conduction channel at interface of PVP and Si NW is reduced by OH^- ion when Si NW embedded in PVP [11]. Experimental results of device threshold voltage were well matched to this theory, and the values were estimated to be –7.17, –4.55, and –2.44 V for diameters of 108, 128, and 148 nm, respectively. Like mobility of device, as the Si NW gets thicker, the carriers are passed through the internal of cylindrical Si NW rather than on the surface in order to be hardly affected by scattering effect. That's why the threshold voltage tends to move from negative value to 0 V as the diameter of Si NW increases.

IV. Conclusion

By following and modifying the previous method, cylindrical Si NWs were synthesized. Also, Al_2O_3 layer was deposited on PI substrate as sacrificial transfer layer and Au electrodes with short gap of 3μm were defined on Al_2O_3 layer by photolithography process. And single cylindrical Si NW with various diameters of 108, 128, and 148 nm were addressed between Au electrodes by DEP process. PVP was coated on p^{++} Si substrate and softly baked in order to evaporate solvent gas from PVP layer. Au electrodes which individual Si NW were linked on were attached on PVP adhesive layer and heated up to 140°C. Fabrication of single cylindrical Si NW FET was completed by being cured after detaching and it was confirmed that Si NW was embedded into PVP by the SEM image. The transistors showed that the mobility of device increased as the Si NW got thicker due to the rough surface characteristic of Si NW because the ratio of surface to volume was reduced and the defect on rough surface was not influential as the diameter of Si NW is larger. In the same way, the influence of scattering effect caused at the interface of PVP and Si NW decreased and the threshold voltage was move to 0 V as the diameter of Si got larger.

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