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Fabrication and Characterization of Poly-Si Vertical Nanowire Thin Film Transistor

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***Abstract*—**In this paper, we present a vertical nanowire thin film transistor with gate-all-around architecture, fabricated using CMOS compatible processes. A novel method of fabricating polysilicon vertical nanowires of diameter as small as 30 nm using wet-etch is presented. Both n-type and p-type vertical poly-silicon nanowire transistors exhibit superior electrical characteristics as compared to planar devices. On a poly-crystalline nanowire of 30 nm diameter, high I_{on}/I_{off} ratio of 10^6, low drain-induced barrier lowering (DIBL) of 50 mV/V, and low sub-threshold slope SS~100mV/dec are demonstrated for a device with channel length of 100 nm.

Keywords — Nanowire (NW), Gate-all-around (GAA), polysilicon (poly-Si), thin-film transistor (TFT).

I. Introduction

POLYCRYSTALLINE silicon has been an extensively researched platform for the development of thin-film transistors [1-3] due to its wide applications such as in active-matrix liquid crystal displays (AMLCD) [4] and implementation into three-dimensional device circuits [5]. Furthermore, the ease of integrating poly-Si thin-film transistors onto low cost substrates subjects it to becoming an ideal candidate for three-dimensional transistor devices. Poly-Si nanowire transistors in the planar form has been explored with much interest owing to its gate-all-around (GAA) architecture, enabling the nanowire channel electric potential to be well-controlled by the gate-electrode [6].

As poly-Si can be easily deposited uniformly on flat surfaces, one of the potential applications is to implement it in three-dimensional stacking of high-density GAA transistors for memory or logic devices [7]. In this paper, we fabricate isolated vertical GAA nanowire *n*-type and *p*-type transistors on poly-Si thin-film. The poly-Si thin-film is deposited on oxide surface which is grown from a bulk silicon wafer similar to glass substrates for AMLCD. Furthermore, we demonstrate novel methods to reduce the diameter of vertical nanowires by wet etch. A three-dimensional schematic diagram of an *n*-type vertical GAA nanowire transistor is shown in Fig. 1. The transistor source of each nanowire transistor is isolated from other transistors by implementing active area separations etch.

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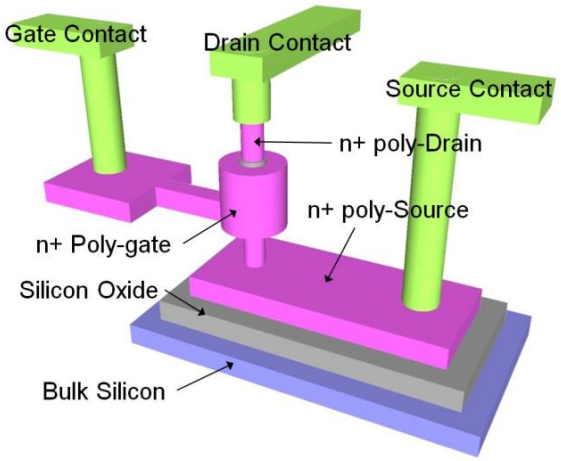

Fig. 1 Schematic diagram of poly-Si vertical nanowire GAA architecture, to be fabricated on top of oxide and bulk silicon

II. Device Fabrication

Poly-Si can be deposited on any surface, forming good quality thin-film required for electronic devices. In this paper, we deposit 500 nm of amorphous silicon by low-pressure chemical vapor deposition on a bulk silicon wafer, with 100nm of oxide in between to separate the two layers. This is required so as to create a distinct silicon layer by itself. Next, resist patterns in the form of circular dots are patterned by KrF lithography, which is subsequently used to define the vertical nanowire. The smallest diameter of the circular dots measures 200 nm after patterning. The underlying amorphous silicon is dry-etched using plasma dry-etching to create approximately 300 nm-tall vertical nano-pillars.

Nano-pillars can be converted into thin nanowires by conventional methods such as sacrificial oxidation [8], in which a layer of oxide is grown followed by diluted hydrofluoric acid removal of the grown oxide or simply by using isotropic etching of the original resist to reduce the diameter [9]. However oxide grown on poly-Si is found to be difficult to remove with non-uniform etch-rate and the uniform-control of resist trimming is challenging when reducing resist of 200 nm diameter to small diameters such as 30 nm. In this paper, we introduce the reduction of vertical nano-pillars by wet-etch using tetramethylammonium hydroxide (TMAH). TMAH in a well-controlled temperature bath of 50˚C etches a uniform 60 nm of amorphous silicon every minute. Due to its isotropic etch nature, we used TMAH to reduce the size of the nano-pillar, resulting in diameters as small as 30 nm nanowires without compromising the height. After formation of the thin nanowires, active regions are defined again by KrF lithography to isolate *n*-type and *p*-type

transistor regions. The cross-sectional schematic can be seen in Fig. 2(a).

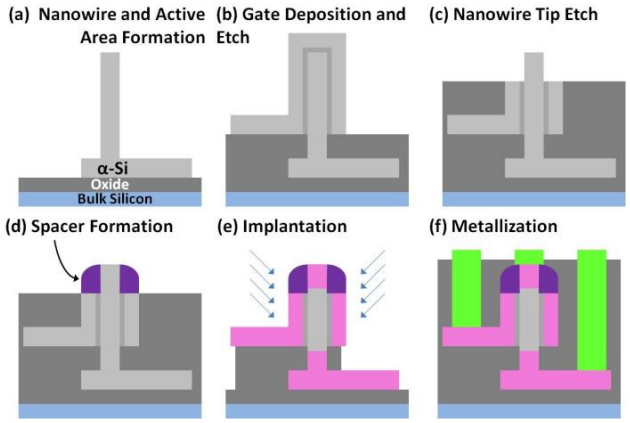

Fig. 2(a) Schematic diagram of poly-Si vertical nanowire with active region on oxide/silicon substrate similar to AMLCD applications, (b) gate-source isolation, gate-stack deposition and formation, (c) gate-tip removal, exposing poly-Si nanowire tip, (d) nitride spacer formation, (e) implantation and (f) final metallization processes

A layer of high-density plasma (HDP) oxide is deposited next, followed by resist coating. By trimming the resist using anisotropic O_2 plasma dry-etch, the vertical nanowire covered with HDP oxide on the sidewalls is exposed. Using controlled diluted hydrofluoric acid (DHF) wet etch, the HDP oxide is removed from the sidewalls, leaving the vertical nanowire protruding upwards with the active region embedded underneath the remaining layer of HDP oxide. A layer of gate oxide is grown by dry oxidation on the exposed amorphous silicon nanowire, at the same time recrystallizing it into a poly-Si state. The gate material is deposited with amorphous silicon, followed by gate definition, as shown by Fig. 2(b).

HDP oxide is deposited next, and using resist again, the tip is exposed and the oxide from the sidewalls is removed. TMAH is once again used to remove the amorphous silicon gate tip, with the vertical gate length defined consecutively at this stage, as shown by Fig. 2(d). A layer of nitride is deposited by plasma-enhanced chemical vapour deposition followed by plasma-dry etch to form a circular-ring spacer around the exposed poly-Si nanowire tip. The layers of HDP oxide is subsequently removed by DHF wet-etch to expose the bottom source, top drain and the gate. By selective lithography, *n*-type devices are opened by KrF lithography and implanted, followed by opening *p*-type devices for implantation, as shown in Fig. 2(e). Oxide is deposited next, followed by DHF wet-etch to expose the implanted drain. Contact holes on top of source and drain regions are patterned and etched, followed by standard metallization processes.

The following tilted SEM images captures the critical steps as described above. Fig. 3(a) shows the smallest nanowire with diameter of 30 nm after thinning by using TMAH wet-etch. Fig. 3(b) shows the removal of amorphous silicon gate tip, also by TMAH wet-etch, exposing the poly-Si nanowire tip protected by the grown gate-oxide. Fig. 3(c) shows the definition of the gate after plasma dry-etch and lastly, metallization in Fig. 3(d). There are a total of four outputs, one for source, drain, gate and another one connecting the bottom bulk silicon which has no effect in the characterization of our poly-Si transistor. Fig. 3(e) shows the cross-sectional TEM across a larger diameter nanowire transistor.

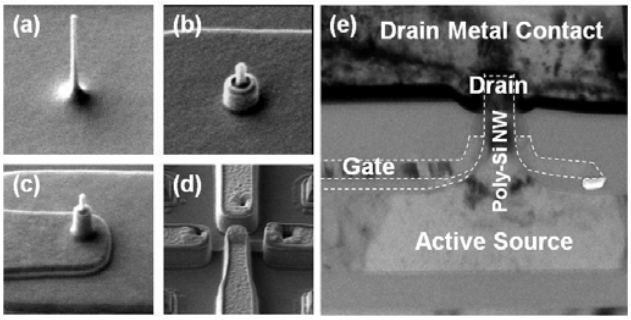

Fig. 3 Tilted SEM images of (a) nanowire formation after thinning by TMAH wet-etch, (b) gate-length definition, (c) gate definition with gate tip exposed, (d) metallization, (e) TEM image across a larger diameter nanowire, showing the source, drain and gate of the transistor

III. Results and Discussion

Individual *n*-type and *p*-type poly-Si nanowire transistors were characterized. Fig. 4 shows the drain-current versus gate-voltage characteristics. The devices measured were with 30 nm nanowire diameter and a gate length of 100 nm.

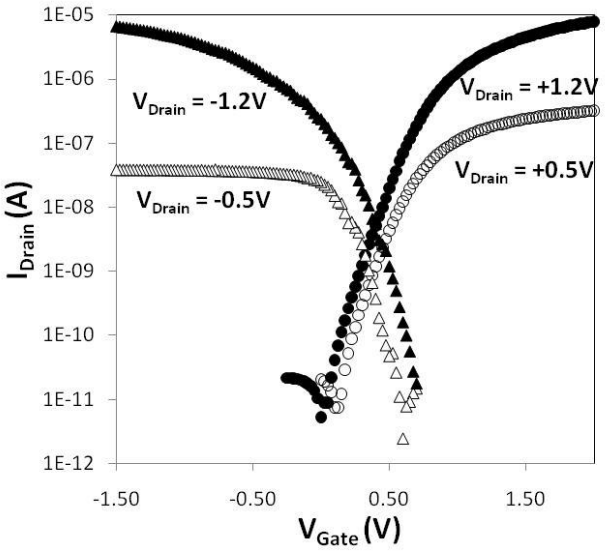

Fig. 4 Drain-current versus gate-voltage characteristic of n-type and p-type transistors with 30 nm nanowire diameter and 100 nm gate length.

The n-type poly-Si nanowire transistor exhibits faster turn-on performance with a subthreshold slope of ~80 mV/dec, I_{on}/I_{off} ratio of 10^6 and low DIBL of ~25 mV/V. The p-type

poly-Si nanowire transistor had a subthreshold slope of ~100 mV/dec, similar Ion/Ioff ratio of 10^6 and a larger DIBL of ~65 mV/V.

IV. Conclusion

We have demonstrated a fully-CMOS compatible fabrication method for vertical gate-all-around poly-Si nanowire transistors with both *n*-type and *p*-type. Poly-Si nanowires with diameters as small as 30 nm were fabricated by using wet-etching rather than by conventional lithographic dependent processes or dry-plasma etching. Both n-type and p-type transistors show comparable performance with high I_{on}/I_{off} ratios, low DIBL and good subthreshold slope. The results points to future stacking of vertical gate-all-around poly-Si nanowire transistors on thin-film platform.

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