

# Efficient Power-Delay Product Modulo $2^n + 1$ Adder Design

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**Abstract**—As embedded and portable systems were emerged power consumption of circuits had been major challenge. On the other hand latency as determines frequency of circuits is also vital task. Therefore, trade off between both of them will be desirable. Modulo  $2^n + 1$  adders are important part of the residue number system (RNS) based arithmetic units with the interesting moduli set  $\{2^n - 1, 2^n, 2^n + 1\}$ . In this manuscript we have introduced novel binary representation to the design of modulo  $2^n + 1$  adder. VLSI realization of proposed architecture under 180 nm full static CMOS technology reveals its superiority in terms of area, power consumption and power-delay product (PDP) against several peer existing structures.

**Keywords**—Computer arithmetic, modulo  $2^n + 1$  adders, Residue Number System (RNS), VLSI

## I. INTRODUCTION

THE Residue Number System (RNS) is a non weighted integer system that by decomposing the arithmetic operations into several independent sub operations implies carry free and thereby high speed operations [1]. RNS is useful in several applications including Digital Signal Processing [2], [3], Image Processing [4], and Fast Fourier Transform computation [5]. Moreover RNS is also inherently fault tolerant against faults and makes diagnosis and correction of errors easier [6], [7].

An RNS system is based on a set of  $n$  moduli  $\{m_1, m_2, \dots, m_n\}$ , that are pair-wise relative prime. The number of integers that can be uniquely coded in RNS called *dynamic range* is determined by the product of the moduli  $D = \prod_{i=1}^n m_i$ . Assume that  $|X|_m$  is the least nonnegative remainder of the division of  $X$  by  $m$  therefore each integer  $X$  is represented by  $n$ -tuple  $X = (x_1, x_2, \dots, x_n)$  residues, where  $x_i = |X|_{m_i}$  if  $X \geq 0$  and  $x_i = |D + X|_{m_i}$  otherwise. An RNS operation  $\diamond$  is defined as  $(z_1, z_2, \dots, z_n) = (x_1, x_2, \dots, x_n) \diamond (y_1, y_2, \dots, y_n)$ , where  $z_i = |x_i \diamond y_i|_{m_i}$  and  $\diamond$  indicates addition, subtraction or multiplication. Therefore an RNS operation is decomposed into several independent and parallel operations called *channel*.

Modulo  $2^n + 1$  is used in the interesting triple moduli set  $\{2^n - 1, 2^n, 2^n + 1\}$  which has several advantages [8]. The modulus of the  $2^n + 1$  form is also used in five moduli set

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proposed in [9]. This channel is also used as an adder in the last stage of RNS multipliers. Moreover modulo  $2^n + 1$  is widely applied in pseudo-random number generation, cryptography [10], and Data Encryption Algorithm [11]. Therefore effective design of modulo  $2^n + 1$  adder in terms of latency, power consumption, and power-delay product (PDP) is a vital task. The structure proposed in this manuscript is not competitive with regard to delay, but that it offers advantages in area, power, and PDP parameter.

Over the years, many papers have been addressed on the design of modulo  $2^n + 1$  adders (e.g., [12], [13], [14], and [15]) that the adder proposed in [15] is the most efficient one. We have compared our approach against the corrected version of previously published design in [15] which is described in [16] and the classic modulo adder which is proposed in [12] but uses ripple adders in its structure.

The rest of manuscript is organized as follows. First we introduce new binary representation in section II and then design its corresponding modulo adder in section III. We will show simulation results in section IV. Finally there are conclusions in section V.

## II. NOVEL REPRESENTATION

The bit positions in our novel number representation system have weights similar to conventional binary number system except that two least significant bits (LSBs) have the same weights. As a matter of fact, the weights of the bit positions are  $2^n, 2^{n-1}, \dots, 2^2, 2^1, 2^0, 2^0$ . There is an example in table I which illustrates representation of residues in the modulus of  $2^2 + 1$  in the novel binary system.

TABLE I  
REPRESENTATION OF RESIDUES IN BOTH CONVENTIONAL AND PROPOSED NUMBER REPRESENTATIONS IN THE MODULO  $2^2 + 1$

Number	Conventional	Propose Representation
0	000	000
1	001	001
2	010	011
3	011	101
4	100	111

Note that in cases that there are two ways for representation of numbers as number 2 which can be represented by either "0011" or "0100" the used convention in our approach is the using of least significant bits, therefore number 2 will be represented by "0011".

We will show that this new system will save area, power consumption, and PDP parameter with regard to earlier proposals.



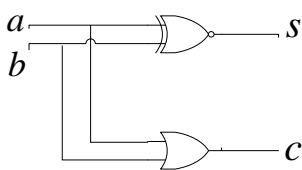


Fig. 4 The logic diagram of H.A\*

IV. COMPARISONS

We have compared our novel modulo adder against those reported in [15] and [12]. Note that as suggested in Fig. 5 we have applied ripple adders in the structure of modulo adder proposed in [12].

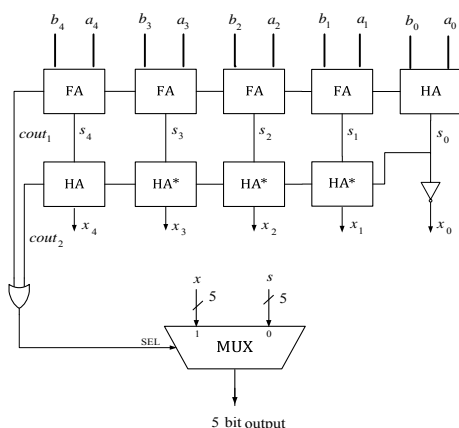


Fig. 5 The structure of modulo adder proposed in [12]

All structures are mapped into 180 nm full static CMOS technology with power supply of 1.8v and temperature of 25°C. In order to quantitative comparisons we ran simulations, for n= 4, 6, and 8 using HSPICE tool. The results for different values of n in modulo 2<sup>n</sup> + 1 adder appear in tables III, IV, and V. Considering cases that n is not power of 2, since there is no formal way to design of TPP therefore it is not applicable (N.A.) whereas our described modulo 2<sup>n</sup> + 1 adder can be applied for any number of n (not necessarily power of 2).

TABLE III

COMPARISON RESULTS FOR MODULO 2<sup>n</sup> + 1 ADDER USING 180 nm CMOS TECHNOLOGY WITH N=4

Adder	Area (Number of transistors)	Power (μW)	Delay (ns)	PDP (fJ)
Bayoumi [12]	194	24.483	0.5757	14.094
TPP [15]	408	52.829	0.5259	27.782
Proposed	184	25.327	0.3704	9.381

TABLE IV

COMPARISON RESULTS FOR MODULO 2<sup>n</sup> + 1 ADDER USING 180 nm CMOS TECHNOLOGY WITH N=6

Adder	Area (Number of transistors)	Power (μW)	Delay (ns)	PDP (fJ)
Bayoumi [12]	278	41.210	0.5919	24.392
TPP [15]	N.A.	N.A.	N.A.	N.A.
Proposed	268	35.999	0.6144	22.117

TABLE V

COMPARISON RESULTS FOR MODULO 2<sup>n</sup> + 1 ADDER USING 180 nm CMOS TECHNOLOGY WITH N=8

Adder	Area (Number of transistors)	Power (μW)	Delay (ns)	PDP (fJ)
Bayoumi [12]	362	52.663	0.8197	43.167
TPP [15]	852	109.55	0.6275	68.742
Proposed	352	47.716	0.8391	40.038

Our approach is slower than compared methods for N=6 and 8 but tables VI and VII indicate that area, power consumption, and PDP parameter of our approach are more efficient than previous proposals.

TABLE VI

SAVINGS OFFERED BY PROPOSED METHOD AGAINST [15] (%)

N	Proposed versus TPP [15]			
	Number of transistors	Power (μW)	Delay (ns)	PDP (fJ)
4	54.9	52.05	29.56	66.23
6	N.A.	N.A.	N.A.	N.A.
8	58.68	56.44	-33.72	41.75

TABLE VII

SAVINGS OFFERED BY PROPOSED METHOD AGAINST [12] (%)

N	Proposed versus Bayoumi [12]			
	Number of transistors	Power (μW)	Delay (ns)	PDP (fJ)
4	5.15	3.44	35.66	33.43
6	3.59	12.64	-3.8	9.32
8	2.76	9.39	-2.36	7.24

V. CONCLUSIONS

Modulo 2<sup>n</sup> + 1 adder is a fundamental module in the most arithmetic units based on RNS. In this paper a novel binary representation has been proposed and utilized to the design of modulo 2<sup>n</sup> + 1 adder. The proposed architecture has been simulated and evaluated in 180 nm CMOS process technology with HSPICE software. Simulation results indicate that proposed modulo adder is more efficient in respect of area, power consumption, and PDP parameter than compared architectures.

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