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Digital Filter for Cochlear Implant Implemented on a Field- Programmable Gate Array

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***Abstract*—**The advent of multi-million gate Field Programmable Gate Arrays (FPGAs) with hardware support for multiplication opens an opportunity to recreate a significant portion of the front end of a human cochlea using this technology. In this paper we describe the implementation of the cochlear filter and show that it is entirely suited to a single device XC3S500 FPGA implementation .The filter gave a good fit to real time data with efficiency of hardware usage.

***Keywords*—**Cochlea, FPGA, IIR (Infinite Impulse Response), Multiplier.

I. Introduction

THE motivation for designing an electronic model of the cochlea is the potential use in prosthetic implants, hearing aids and in systems that extract information from sound signals in a biomimetic fashion. The processing that takes place in the human cochlea is modeled as an array of bandpass filters, whose cutoff frequencies range over the human speech frequencies.

The digital cochlea is implemented on a single Xilinx Field Programmable Gate array (FPGA). The FPGA chip is on a board that contains both an analog to digital (A/D) converter and a digital to analog (D/A) converter. The A/D converter converts the speech signal into a digital representation and the D/A converter converts the digital signal into its original analog form [1]. An anti-aliasing filter is used to reduce the noise and limit the frequencies to speech frequency range.

Mishra A. and Hubbard A.E. have in their work [3] designed a cochlear filter for high frequency audio signal, using a 10-pole 20-zero IIR filter that is designed using LMSE algorithm. This work aims at designing the filer for speech frequency signals.

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II. Cochlear Map and Frequency placement

Sound undergoes a series of transformations as it progresses through the outer ear, middle ear, inner ear, auditory nerve and into the brain. The outer ear receives acoustic pressure waves, which are converted into mechanical vibrations in a series of small bones in the middle ear (malleus, incus and stirrup). In the inner ear, the cochlea a snail shaped cavity filled with fluid, transforms the mechanical vibrations to fluid vibrations. Pressure vibrations within the fluid of the cochlea displace a flexible membrane called the basilar membrane. These displacements depend on the frequency content of the acoustic signal. The inner hair cells, attached to the basilar membrane, are the sensory cells that transduce mechanical motion into neural stimuli. These hair cells respond according to the displacements of the basilar membrane and the associated fluid flow and cause neurons to fire and signal the presence of excitation in the inner ear. These auditory neurons carry information from the hair cells to the cochlear nucleus in the brainstem and thereby to higher nuclei in the brain.

The inner ear is responsible for analyzing the input signal into different frequencies. The location of inner hair cells along the basilar membrane determines the hair cells optimal response to various frequencies. Hair cells at the apex of the cochlea respond to low frequencies whereas hair cells at the apex respond best to high frequencies. The best frequency of a set of hair cells logarithmically varies with the spiral length of the cochlea (Fig. 1).If a signal consists of multiple frequencies, the resulting wave creates displacement along the basilar membrane. The cochlea acts as a spectrum analyzer, decomposing complex sound into its frequency components [2].

A function that relates the characteristic frequency (CF) of any location along the length of the cochlea to the distance(x) of that location from the apex i.e. the frequency-position function (also known as Greenwood function) given by the following equation:

$$CF = A\,(10^{\,ax/L} - K)$$

Where A is a constant that controls the high-frequency limit of the map (Hz); a is a constant that controls the slope of the map, L is the length of the cochlea in mm; K is a constant that controls the low-frequency behaviour of the map. For humans these constants are A=164.5, a=2.1, K=1.0 and L=35.

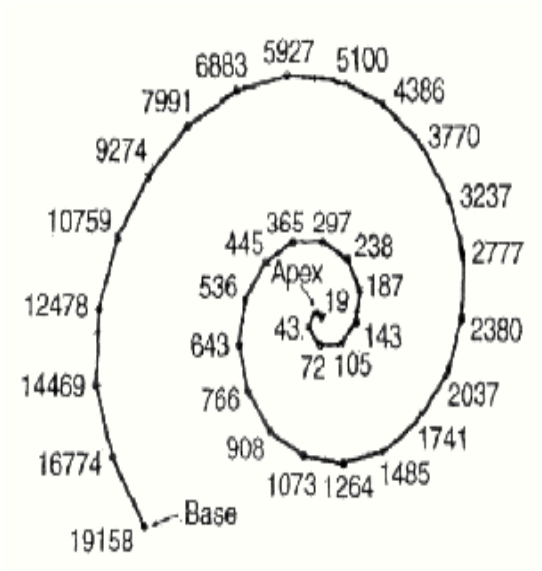

Fig. 1 Diagram of the basilar membrane showing the base

II. Filter Design

When the ear is stimulated by sound, different regions of the basilar membrane respond to different frequencies that occur in a sort of "tuning" of frequencies. These different regions can be translated as a bank of cochlear filters along the basilar membrane.

The human speech frequency ranges from approximately 100 to 3500 Hz. We have designed 16 bandpass filters whose centre frequencies as shown in Table 1 are chosen to cover the entire speech frequency range. The bandpass filters split the speech signal into different frequency components that can be used to recognize phonemes.

Bandpass filters were used because the cochlea acts as a spectrum analyzer, decomposing complex sound into its frequency components, and bandpass filters tell if a signal contains a frequency component with a specific frequency range. These 16 bandpass filters are all Infinite Impulse Response (IIR) filters. The FIR filter gives linear phase. But cochlear filters do not need a linear phase and therefore IIR filters are preferred to FIR filters [3] .IIR filters can achieve a given filtering characteristic using less memory and calculations than similar FIR filters. This work uses fixed-point arithmetic and the number of bits is optimized so that the disadvantage of lower computing time with fixed point implementation is overcome.

All of the filters used in this work are Butterworth. In Butterworth filters the magnitude response is maximally flat in the passband and monotonic overall.

The actual implementation of an IIR filter can be done in several ways. Some of the common ways are Direct Form I /II and their transpose forms, the Cascade form and Parallel forms. The direct form II transpose structure is preferred here because it cannot overflow "internally" in two's complement fixed-point arithmetic. The filter models are all designed in two's complement fixed-point arithmetic that implies the need for the direct form II transpose structure. Fixed-point numbers are not as precise as floating-point numbers, but fixed-point hardware is much more cost effective, allowing a significant saving in hardware.

TABLE I. BANDPASS FILTER FREQUENCY RANGE.

Center Frequency (Hertz) (3dB-points)	Frequency Range of Bandpass Filter (Hertz)
150	125 – 175
250	225 – 275
350	325 – 375
450	420 – 480
570	530 – 605
700	655 – 745
840	790 – 890
1000	940 – 1060
1170	1105 – 1235
1370	1285 – 1455
1600	1505 – 1695
1850	1745 – 1955
2150	2005 – 2295
2500	2345 – 2655
2900	2705 – 3095
3400	3145 – 3655

The number of coefficients for the filter indicates the sharpness of the filtering or the slope of the rolloff curve. The higher the order of the filter designed sharper is the filtering.Fiters of different order until eighth were implemented it was however observed that a second order filter satisfied the requirement, since it was observed that higher order filters used more memory because of the use of more coefficients .First order filters caused an overlap between neighboring filters and were therefore not used. Fig. 2 shows a second order bandpass filter with centre frequency of 1170 Hz sampled at 16 KHz designed using Simulink and the Xilinx Blockset. The implementation is a direct form II transpose structure.

In order to keep a certain frequency from resonating in more than one filter, filters were optimized. Since increase in order of the filter will increase the number of coefficients, the range of frequencies around the centre frequency of each filter was reduced. This reduced the magnitude of the intersection between adjacent filters which in turn reduced the overlap between neighboring filters.

The filter design also requires the use of correct number of bits [4] to arrive at a level of precision to accurately filter the desired range of frequencies while maintaining the memory capacity of the FPGA. The coefficients of the filter in the lower frequency range appear to be the same and therefore these need more number of bits. For Example if two filters with coefficients 0.00234587634523421 and

0.00234587634524327 both use insufficient number of bits to retain precision, both could get represented as 0.00234587634520000 and there would be no difference seen. So instead of full precision provided by Xilinx while representing coefficients user defined precision was used .Each of the numerator and denominator coefficients were represented using different precisions. It was observed that Numerator coefficient 1 and numerator coefficient 3 were equal except for the sign. It was seen that numerator 3 needed more bits than numerator 1 it was also observed that among the numerator and denominator coefficients numerator coefficients required more bits for greater precision.

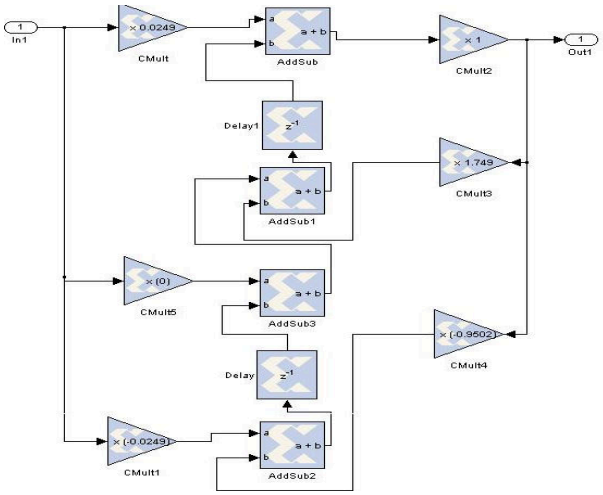

Fig. 2 II order bandpass filter in Direct Form II transpose structure

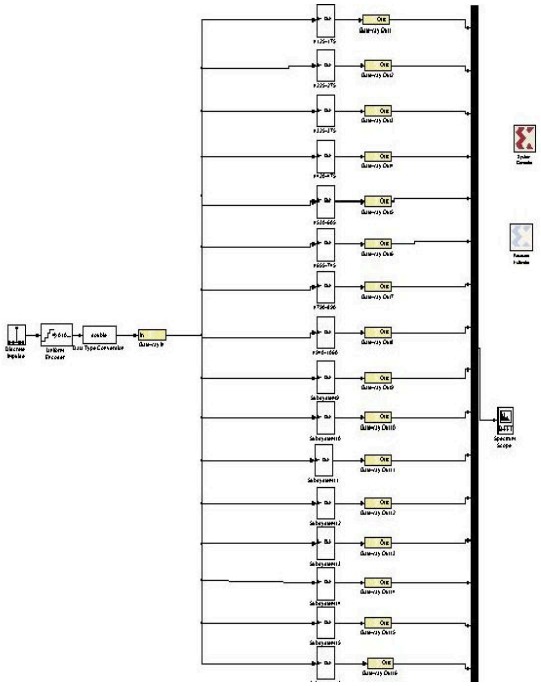

Fig. 3b: 16 channel Bandpass Filter design

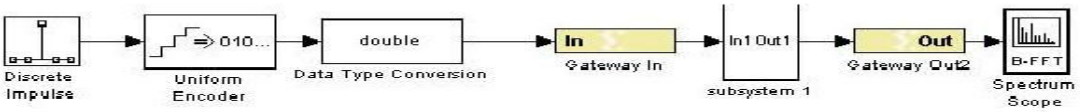

Fig. 3a: Design of a single bandpass filter

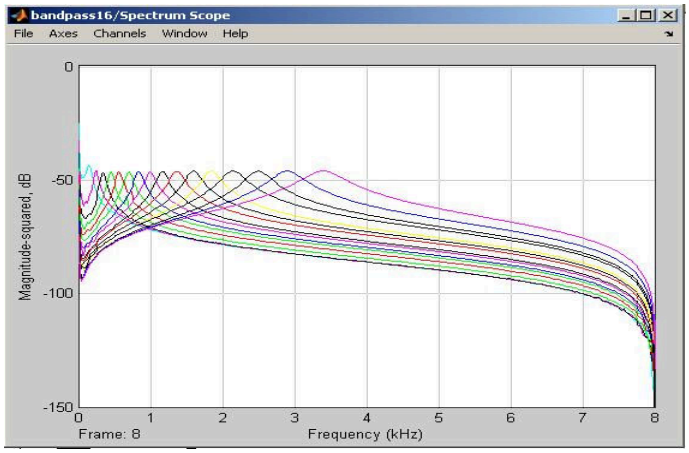

Fig. 4 Magnitude response of the 16 channel bandpass filter

IV. Results and Conclusion

A system of 16-channel digital bandpass filters was designed; the results obtained using simulink was verified using matlab. Several wordlengths like 8,12,14 bits were considered then since data of the target application are 16 bits wide the entire design was constructed with a 16 bit data input. The internal wordlength was chosen to be 40 bits to accommodate maximum possible input multiplied by maximum possible gain. The filter design block diagram is shown in Fig.3a and Fig.3b and its simulation in Fig.4.The simulation results using system generator (Fig.4) match the results obtained from the matlab code.

The Xilinx Resource Estimator block provides fast estimates of FPGA resources required to implement a System Generator subsystem or model. These estimates are computed by invoking block-specific estimators for Xilinx blocks, and summing these values to obtain aggregated estimates of lookup tables (LUTs), flip-flops (FFs), block memories (BRAM), 18x18 multipliers, tristate buffers, and I/Os. The resource estimation results are shown in Fig.5.

The configurable logic block (CLB) of the XC3S500E FPGA constitutes the main logic resource for implementing synchronous as well as combinational circuits. Each CLB contains four slices and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUT in this application is used as a 16-bit shift register(SRL16) for multiplication of coefficients .From the estimator we observe that 11048 slices are utilized. This shows that the cochlear filter can be completely accommodated on the chip. The hardware and the simulation results matched perfectly.

Fig. 6 Compilation status of 16 channel bandpass filter

The lower frequency filters (1-2) did not show a very good response to real time data. This was because a trade off was made between the response and the number of coefficients.

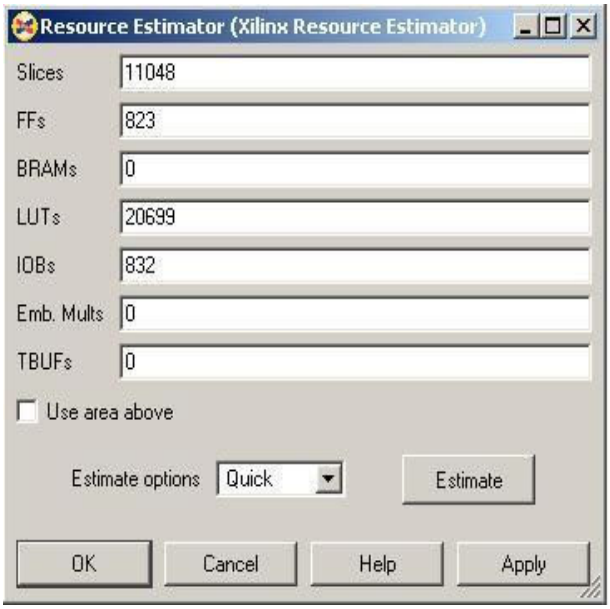

Fig. 5 Resource estimation of 16 channel bandpass Filter

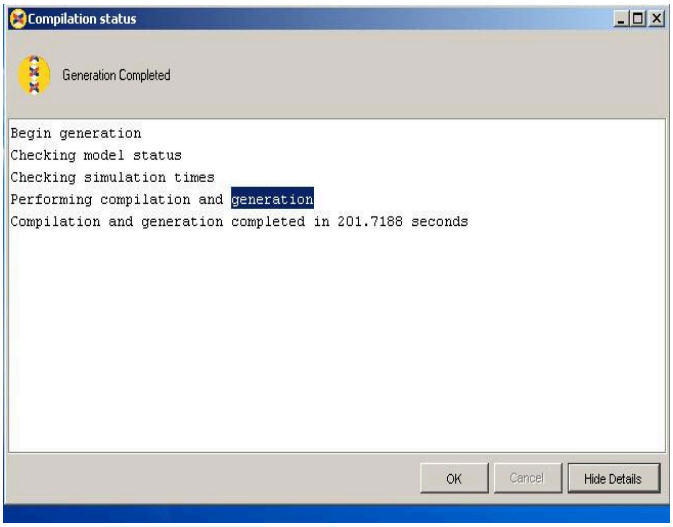

Fig. 6 Compilation status of 16 channel bandpass filter

Since the first two filters are designed well within 300Hz the lower frequency side was not of great interest and fitting it well was not considered important.

The IIR filter is meritorious compared to the traveling-wave amplifier model because the IIR filter computation is in real time and at low cost [3]. Fig. 6 shows the compilation report. It is observed that the compilation and generation of the 16-channel bandpass filter took only 201.78 seconds as compared to 0.1h/ms computational time (DECstation 5000 at approximately 35 VAX11780 equivalents) required for the traveling-wave amplifier model [6], and also to a digital processor [5] in the linear case.

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