International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:5, No:2, 2011

Design of Novel SCR-based ESD Protection Device for I/O Clamp in BCD Process

Yong-Seo Koo, Jin-Woo Jung, Byung-Seok Lee, Dong-Su Kim, Yil-Suk Yang

***Abstract*—**In this paper, a novel LVTSCR-based device for electrostatic discharge (ESD) protection of integrated circuits (ICs) is designed, fabricated and characterized. The proposed device is similar to the conventional LVTSCR but it has an embedded PMOSFET in the anode n-well to enhance the turn on speed, the clamping capability and the robustness. This is possible because the embedded PMOSFET provides the sub-path of ESD discharge current. The TLP, HBM and MM testing are carried out to verify the ESD performance of the proposed devices, which are fabricated in 0.35um (Bipolar-CMOS-DMOS) BCDMOS process. The device has the robustness of 70mA/um that is higher about 60mA/um than the LVTSCR, approximately.

***Keywords*—**ESD Protection, grounded gate NMOS (GGNMOS), low trigger voltage SCR (LVTSCR)

I. Introduction

ELECTROSTATIC discharge (ESD) failure is still a major concern in the electronics industry. As integrated circuit designs migrate toward the sub-micron, on-chip ESD protection design becomes a challenging task, particularly for fast response, low clamping voltage, and area efficient ESD protection solutions [1], [2]. The most common protection structures in advanced CMOS technologies are based on GGNMOS (Gate Grounded NMOS) and lateral SCRs (Silicon controlled rectifier). The GGNMOS has been a simple solution for ESD protection but the area efficiency and the parasitic capacitance inherent to the GGNMOS have limited their use as a protection device for a highly robust and low capacitive ESD protection circuit. Lateral SCRs have been shown to provide an excellent level of ESD protection with a relatively small area and capacitance, making them a viable alternative to GGNMOS based protection circuits in some applications. Although the SCRs provide a higher ESD robustness than the GGNMOS, the high trigger voltage and low turn on speed make these ESD circuits difficult to migrate to new technology. In order to overcome these difficulties, SCR-based ESD protection devices are being developed using various structures. In this paper, we present a LVTSCR-based novel ESD protection device with an additional PMOSFET to enhance the turn on speed, the transient clamping capability, and the robustness. The ESD performance of the proposed device fabricated with the 0.35um BCDMOS process will be discussed.

Yong-Seo Koo is with the Department of Electronics and Electrical Engineering, DanKook University, Gyeonggi-do, Korea.(phone: +82-31-8005-3625, email: yskoo@dankook.ac.kr)
Jin-Woo Jung is with the Department of Electronics and Electrical Engineering, DanKook University, Gyeonggi-do, Korea.(phone: +82-31-8005-3625, email: zinewoo@dankook.ac.kr)
Byung-Seok Lee is is with the Department of Electronics and Electrical Engineering, DanKook University, Gyeonggi-do, Korea.(phone: +82-31-8005-3625, email: bangbang01@dankook.ac.kr)
Hwan-Kyu Ju is is with the Department of Electronics and Electrical Engineering, DanKook University, Gyeonggi-do, Korea.(phone: +82-31-8005-3625, email: jhk0701@dankook.ac.kr)
Yil-Seok Yang is with Electronics and Telecommunications Research Institute , Daejeon, Korea

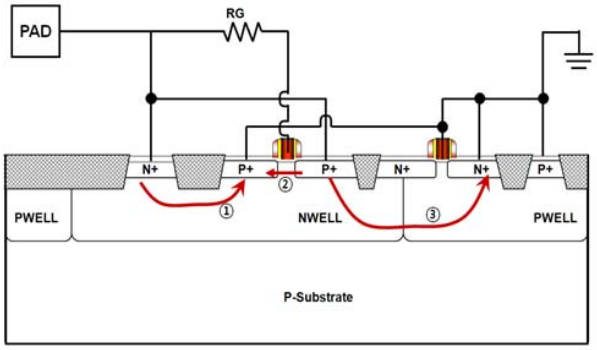
II. Proposed ESD protection circuit

A. Problems of the conventional ESD protection devices

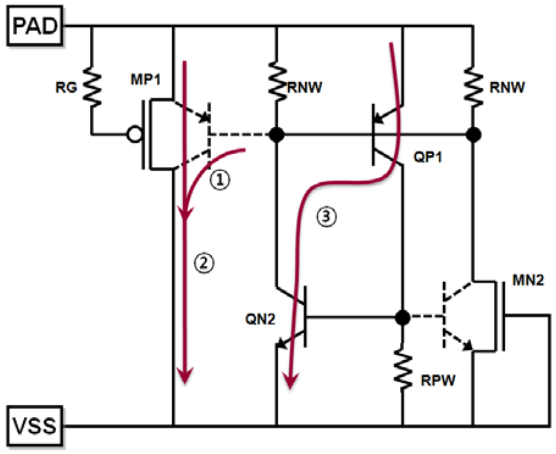
The LVTSCR was developed to reduce the SCR trigger voltage below the N-well/P-well junction breakdown voltage by using a GGNMOS integrated into the SCR as the triggering device. Because of its low trigger voltage, the LVTSCR structure has been widely used for ESD protection for low voltage applications. But there are some problems found in the LVTSCR structure. The first LVTSCR problem is that the inclusion of the GGNMOS integrated directly into the SCR increases the minimum possible value of N+ to P+ spacing (Ld), which limits the transient clamping capability and turn on speed. The second is the transient latch-up problem caused by noise pulses or overshoot surges during the normal operation of the ESD protection power clamps. In order to solve these problems, the various ESD protection structures based on the SCR such as GGSCR [3], DTSCR [4] and HHVSCR [5] have been presented. But each device has problems; the GGSCR has the latch-up problem due to the low holding voltage, the DTSCR is not suitable due to the leakage current, and the HHVSCR has a poor turn-on time because of the additional resistance between the discharge path and the reduced current gain of the parasitic NPN/PNP bipolar transistors, which are used to increase the holding voltage.

B. Device structure and operation of the proposed device

A cross sectional view and equivalent circuit of the proposed device are shown in Figure 1.



(a)



(b)

Fig. 1The cross-sectional view (a) and equivalent circuit (b) of the proposed ESD protection device; the red arrow indicates the discharging current path and the number of each arrow presents the operation sequence.

The basic structure of the proposed device similar to the LVTSCR has the NMOSFET integrated into the device, with the n+ NMOSFET source serving as the SCR cathode. The n+ drain of the NMOSFET begins in the n-well and bridges the n-well/p-well junction. But unlike the LVTSCR, additional PMOSFET is embedded into the anode n-well, with the p+ PMOSFET source serving as the SCR anode. The p+ drain of the PMOSFET is connected to the cathode electrode and the gate of the PMOSFET is connected to the anode electrode (PAD) through the gate resistor RG.

The proposed device has four different operation modes. Under normal operation mode, the gate of the embedded PMOSFET MP1 is biased at VDD to keep itself off and there is no current path through the device. On the other hands, when an overshoot noise pulse is injected to the pad, the gate of the MP1 is biased at low level by the gate resistance RG and the parasitic capacitance Cgs of the MP1 and the MP1 turns on weakly. And the overshoot voltage occurred by overshoot noise pulse on the pad is clamped. Although the gate bias (Vsg) is not enough as the threshold, the parasitic PNP bipolar transistor of the embedded PMOSFET may be turned on because of lower breakdown voltage due to the presence of high field under the gate. Therefore, the noise pulse is bypassed thorough the embedded PMOSFET (see the path #2 in Figure 1).

Under ESD event, like the noise condition, the current path under the gate of MP1 is existed. But dislike the noise condition, this current path is not generated by the weakly biased gate anymore but by the avalanche current path #1 in Figure 1. As the ESD pulse is injected to the PAD, the avalanche breakdown begins at the junction between the p+ source of the PMOSFET and n-well and the current path #1 in Figure 1 is formed. This avalanche current corresponds to the base current of parasitic PNP bipolar transistor of MP1 and the current increase with the voltage on the PAD. If the avalanche current is enough over the threshold current(the junction of the p+ source of MP1 and the anode n-well is forward biased at this current level), the parasitic PNP bipolar transistor turns on and the voltage on the PAD is clamped below the turn-on voltage of the PNP(current path #2). When the ESD current injected to the PAD increases even more, the current of the parasitic PNP bipolar is saturated and the device operates as a SCR with very low impedance (see the path #3 in Figure 1). On the other hand, when a negative bias is applied on the pad with grounded line, the parasitic diode (p+ cathode/p-well or p-substrate /n-well /n+ anode) in the proposed device will be forward biased to discharge the negative ESD current.

III. Experimental Results

A. TLP I-V characteristics

The TLP is typically presented as a plot of the current versus the voltage showing a parameter, such as the turn-on point (V_{t1}, I_{t1}) of the snapback protection structure. Other parameters, such as the on-resistance can also be easily found in the TLP I-V curve [6]. A rectangular pulse can be obtained when discharging an open-ended transmission line width 50 ohm impedance over an attenuator as shown in Figure 2. Th transmission line is charged via a high voltage power supply and discharged via a switch. The current and voltage values are captured after the attenuator. A short coaxial cable connects the attenuator with the device under test (DUT). The I-V characteristic and DC-leakage current has been measured with a transmission line pulse (TLP) tester with a pulse duration of 100ns, rising time of 10ns.

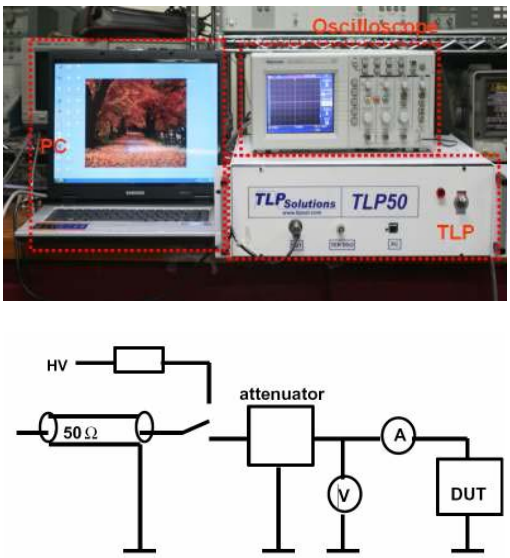


Fig. 2 Transimission line pulse test system

Figure 3 shows the TLP I–V curves of the proposed ESD protection circuit. The TLP-measured the trigger voltage and holding voltage of the proposed device are 12.3V and 3.1V,

respectively. Also, the second breakdown current of the proposed device is 5.15A.

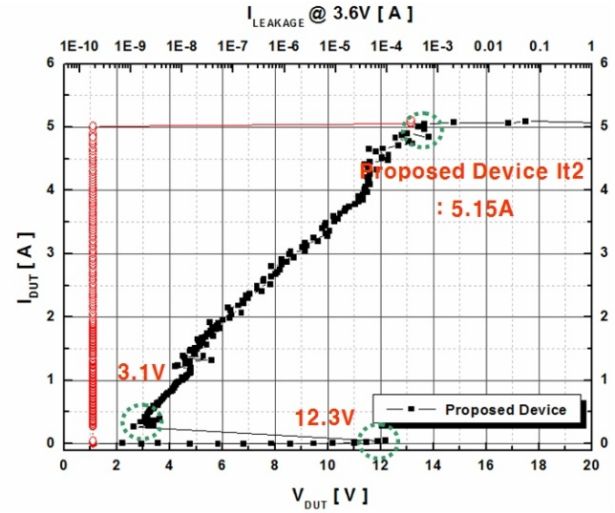


Fig. 3 Measured TLP I-V characteristics of conventional LVTSCR and proposed ESD protection device.

B. ESD Robustness (HBM, MM)

The results from the TLP test with the 100ns pulse width can be well correlated to the HBM (Human Body Model). This has been well established in recent reports. However, a miscorrelation between the TLP and the HBM still exists because of the system's limitation and its testing environments [7], [8].

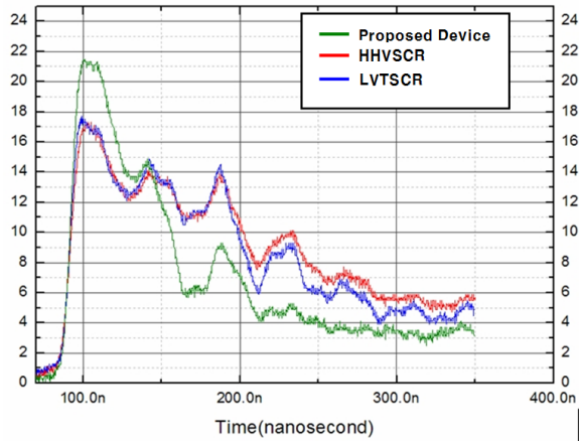
The HBM and MM (Machine Model) ESD robustness of the proposed devices are measured by the ESS-6008 ESD simulator. The failure criterion is defined as a 20% current shift from the original I-V curve at 3.6V (operating voltage+10%). The proposed ESD protection device passes an ESD test of HBM 8kV and 600 V.

C. Turn-on speed

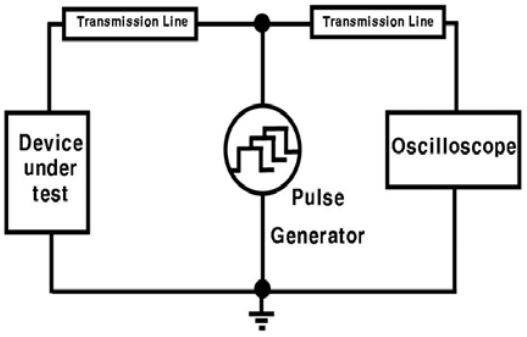
The comparisons of the turn on speeds between the LVTSCR, HHVSCR[9] and the proposed ESD protection device under a 0-10V voltage pulse with a 10 ns pulse rising time are shown in Figure 4. The turn-on time of the proposed ESD protection device(~160ns) is faster than that of the LVTSCR (~280ns) and the HHVSCR (~290ns) under the 0-10V voltage pulse. From these experimental results, the proposed ESD protection device is more suitable than other ESD protection devices for the quick discharge of electrostatic energy.

TABLE I
COMPARISON ON THE ESD ROBUSTNESS OF LVTSCR AND PROPOSED DEVICE

	LVTSCR	***Proposed Device***
HBM	7kV	8kV
MM	400V	600V
I_{t2}	4.6A	5.1A
mA/um	60mA/um	70mA/um



(a)



(b)

Fig. 4 (a) Turn-on wavefrom of LVTSCR, HHVSCR and proposed device. (b) Experimental setup to measure the turn-on speed.

IV. CONCLUSION

In this paper, a novel LVTSCR-based device for electrostatic discharge (ESD) protection of integrated circuits (ICs) is designed, fabricated and characterized. The proposed ESD protection circuit has been verified using the 0.35um BCDMOS process. Compared to the conventional LVTSCR (HBM:7kV/MM:400V), the proposed circuit can provide a much higher robustness (HBM:8kV/MM:600V). The turn-on time of the proposed ESD protection device (~160ns) is faster than that of the LVTSCR (~280ns) and the HHVSCR (~290ns) under a 0-10V voltage pulse. This device is suitable for an ESD

protection structure used for high-speed I/O clmap applications.

ACKNOWLEDGMENT

This work partly supported by the IT R&D program of MKE/KEIT [10035171, Development of High Voltage/Current Power Module and ESD for BLDC Motor] and this work also was supported by “System 2010” project of Korea Ministry of Knowledge Economy.

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Yong-Seo Koo Yong-Seo Koo, Professor, College of Engineering126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea – Yong-Seo Koo is Professor of Electronics and Electrical Engineering Department. He received the BS, MS, and PhD degrees in electronic engineering from Sogang University in 1981, 1983, and 1992, respectively. From 1983 to 1993, he was with Electronics and Telecommunications Research Institute (ETRI), where he worked on semiconductor device and BiCMOS/BCD process development. From 1993 to 2009, he was with the Department of Electronic Engineering, Seokyeong University, Seoul, Korea. He joined the Department of Electronics and Electrical Engineering, Dankook University as a professor in 2009. His current research interests include power semiconductor devices, such as power BJTs, LDMOSs, and IGBTs, as well as high-efficiency power management integrated circuits (PMIC), such as DC-DC converters, in addition to electrostatic discharge (ESD) protection circuit design..