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Design and Layout of Two Stage High Bandwidth Operational Amplifier

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***Abstract*—**This paper presents the design and layout of a two stage, high speed operational amplifiers using standard 0.35um CMOS technology. The design procedure involves designing the bias circuit, the differential input pair, and the gain stage using CAD tools. Both schematic and layout of the operational amplifier along with the comparison in the results of the two has been presented. The operational amplifier designed, has a gain of 93.51db at low frequencies. It has a gain bandwidth product of 55.07MHz, phase margin of 51.9º and a slew rate of 22v/us for a load of capacitor of 10pF.

***Keywords*—**Gain bandwidth product, Operational Amplifier, phase margin, slew rate.

I. Introduction

OPERATIONAL Amplifier (OP-AMPS) have become one of the core components in analog and mixed signal (AMS) design. In modern analog and mixed signal CMOS IC like ADCs, DACs, PLL, etc, op-amp is one of the integral components. With the ever increasing effort and trend towards small area design, and integrating multiple cores on a single chip, so as to have to a system on chip (SOC) and ASIC design, IC fabrication process and technology has also continuously evolved to cope up with the demand. In the last forty years, the semiconductor industry has been trying to cope with the Moore's law and in effect reduce the transistor size and pushing it towards the extreme ends.

The reduction in transistor size, so as to have more transistors on a single chip, introduced various parasitic effects, and the transistor model became much more complex than the conventional model. The simple square law equations [1] of the transistors do not hold below 1um CMOS technology. To account for these parasitic effects various computer aided tools (CAD) developed so as to simulate the CMOS based design more precisely.

A two stage op-amp has been designed using 0.35um CMOS technology in Cadence. The paper presents schematic level design flow of the two stage op-amp design to meet the given specification and then further improving the design for high performance in terms of gain bandwidth product (GBW) in section 2. The design layout using common centroid matching technique is discussed in section 3. In section 4 comparison has been done on the basis of performance parameters at the schematic and the layout level. The circuit is finally tested to show that the design is robust to fluctuations in power supply.

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II. Schematic Level Design

The op-amp design at schematic level is mainly divided into three main parts, the biasing circuit, the input differential pair and the gain stage as shown in Fig. 1. Some op-amp have an output buffer stage also for driving resistive loads [2], but in my case, only capacitive load is present at output, so the buffer stage will not be used.

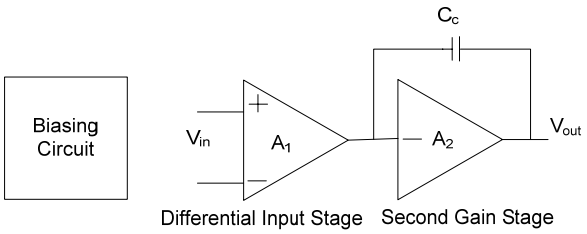

Fig. 1 Block diagram of two stage op-amp

Before beginning with the design, we need to have an understanding of various process parameters of the PMOS or NMOS.

A. Process Parameter Selection

The analog CMOS design is generally governed by the CMOS square law equations [1]:

$$Triode: I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad (1)$$

$$for\ V_{GS} \geq V_{tn}\ and\ V_{DS} \leq V_{GS} - V_{tn}$$

$$Saturation:$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{tn})^2\left[1 + \lambda(V_{DS} - V_{DS,sat})\right] \quad (2)$$

$$for\ V_{GS} \geq V_{tn}\ and\ V_{DS} \geq V_{DS,sat} = V_{GS} - V_{tn}$$

There are a lot of process parameters involved in (1) and (2), but in modern process, all these parameters and many more others are taken into account in the modeling of the MOS in CAD tools. Hence, the square law equations are only used for proportional relationship.

For the selection of width W and length L of the transistor, it is diode connected and biased at a fixed current of 8μA as shown in Fig. 2 and a DC analysis is performed in Cadence,

with DC operating points being saved. Then various parameters of the transistor like transconductance g_m, output resistance $r_o = 1/g_{ds}$, saturation voltage Vd_{sat}, are observed. It is also observed that transistor is operating in saturation region and that is stated as region 2 in Cadence. The DC analysis is repeated with different lengths L and the width W is adjusted corresponding to each length to ensure that $Vd_{sat} \approx 5\%$ Vdd ≈ 167mV-172mV. The values of the process parameters g_m and g_{ds} are recorded as shown in Table I. The gain A_v of the single transistor when used as a common source amplifier is given in (3) [3].

$$A_v = \frac{g_m}{g_{ds}} \tag{3}$$

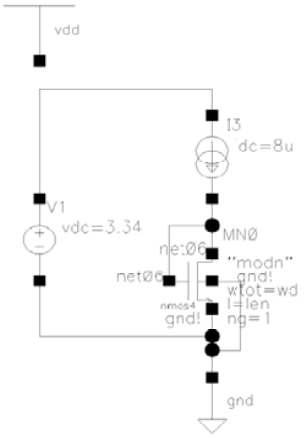

Fig. 2 NMOS Biasing Circuit

TABLE I
TRANSISTOR BIASING

L	W	g_m	g_{ds}	A_v	Vd_{sat}
0.35µm	1µm	64.29µ	1.129µ	56.944	172.4mV
0.4µm	1.2µm	67.04µ	940.2n	71.3	167mV
0.6µm	1.6µm	65.71µ	483.7n	135.9	170.6mV
0.8µm	2µ	65.17µ	325.9n	200	171.6mV
0.9µm	2.4µm	66.59µ	291.3n	228.6	168.1mV
1µm	2.5µm	66.32µ	265.9n	249.4	168.5mV

Table I shows that with increasing length L of the transistor, the open loop gain A_v. We will choose the transistor with length L = 0.9µm and width W = 2.4µm. with open loop gain A_v of 228.6.

B. Current Mirror

The biasing circuit is based on the basic idea of current mirror as shown in Fig. 3. The drain current in diode connected transistor M1 is the reference current I_{ref} and the current in the drain of M2 is the output current I_o. The two currents are related by the ratios of W/L as follows [4].

$$\frac{I_o}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \tag{4}$$

Hence, in effect if I_{ref} is present, any required output current I_o can be generated by just changing the ratio of W and L.

Cadence provides us with the option of adjusting the width W using multiples of width strip, using the concept of finger and number of gates. If the transistor M1 is split into two gates, and four gates are used for M2, then M2 draws twice the current of M1, as shown in Fig. 4, where I_{ref} is 8µA and I_o is 16µA.

Ideal current source should have infinite output resistance, so to have an increased output resistance of the current mirror, with wide swing, cascode current mirror is designed as shown in Fig. 5 [5].

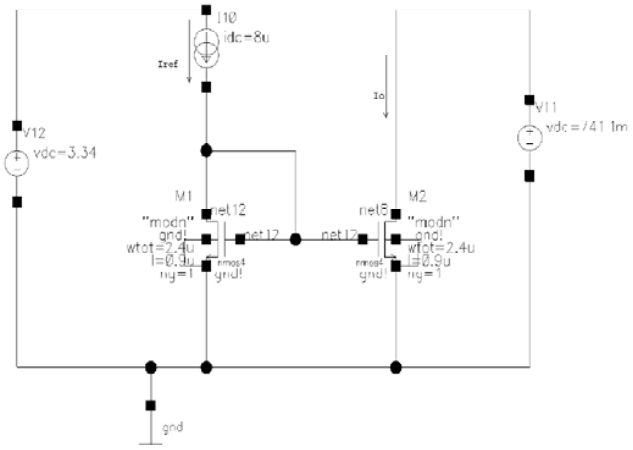

Fig. 3 Basic Current Mirror

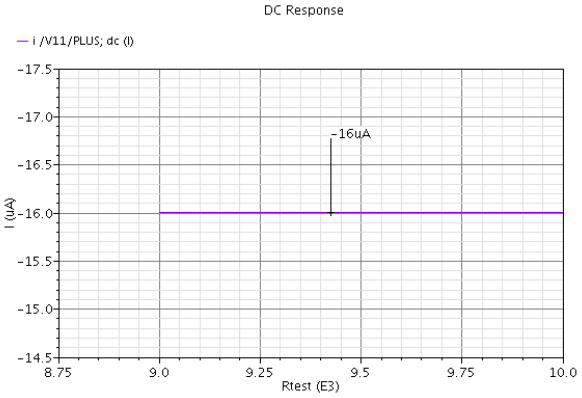

Fig. 4 Current I_o when fingers of M2 are doubled to that of M1

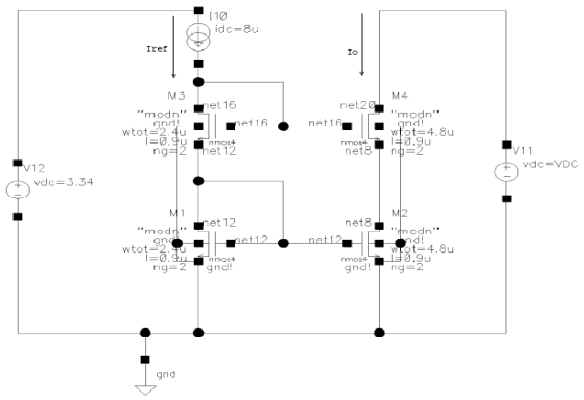

Fig. 5 Cascode Current Mirror

C. Beta-Multiplier and Self Biasing

To provide I_{ref}, in Fig. 5, some constant current source is needed. For this purpose a PMOS cascode current mirror is designed for the reference current of 8μA, as shown in Fig. 6. The length of PMOS used in current mirror is the same as that of the NMOS, but the width is adjusted and found to be 6μm using DC analysis, so it is operating in saturation region with Vd_{sat} of 168mV.

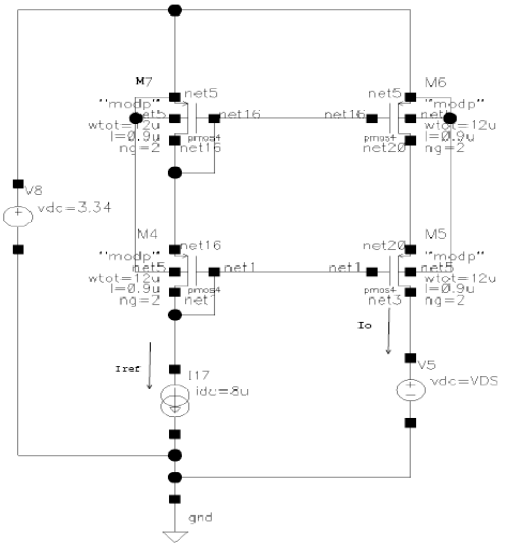

Fig. 6 PMOS Cascode Current Mirror

The two cacsoded current mirrors are connected together as shown in Fig. 7, so as to form what is commonly known as the beta multiplier [6] and is a self biased circuit, where PMOS and NMOS current mirrors are trying to source and sink the biasing current into each other respectively. The resistor R_b is added to make the reference current independent of power supply voltage V_{DD} and hence have a stable transconductance [7]. To determine the value of R_b, DC sweep analysis is performed with R_b as the sweep variable, and the value of R_b is determined that gives the current of 8uA, as shown in Fig. 8. In my case it is found out to be 12k ohms. When R_b is changed to rpolyhc, its value is readjusted by a small factor and changed to set to 11.8K ohms. DC sweep analysis is performed over to supply voltage V_{DD}, and the reference current is observed to verify if it has become independent of changes in supply voltage. As shown in Fig. 9, it is evident that reference bias current changes by very small factor with changes in V_{DD}.

To ensure that transistors are M2 and M4 are operating in saturation region, two voltages are generated in the single rail, by inserting two the resistance R_a as shown in Fig. 10. DC sweep analysis is performed to determine the value of R_a which gives the reference current of 8μA in the rails. The value of R_a is found to be 27.5K ohms as shown in graph in Fig. 11. Table II summarizes all the values and sizes of the transistors for the beta-multiplier for current of 8μA.

D. Differential Input Stage

A input differential stage is shown in Fig. 12. The transistor M9 and M10 are the p-channel input pair and the M11 and M12 are the n-channel active load current mirrors. M13 and M14 are the biasing transistors. The choice of having a PMOS or NMOS as the differential pair is based on the following consideration

--PMOS input differential pair gives a better slew rate for a given bias current, as compared to NMOS differential pair [8].

--PMOS differential pair implies that there will be a NMOS amplifier in the second stage. As the NMOS amplifier gives better transconductance g_m, which will provide improved gain and gain bandwidth product [8].

--1/f noise is one of the motivating factors for using PMOS for first stage input, as PMOS devices exhibit low 1/f noise in comparison to their NMOS counter parts [8].

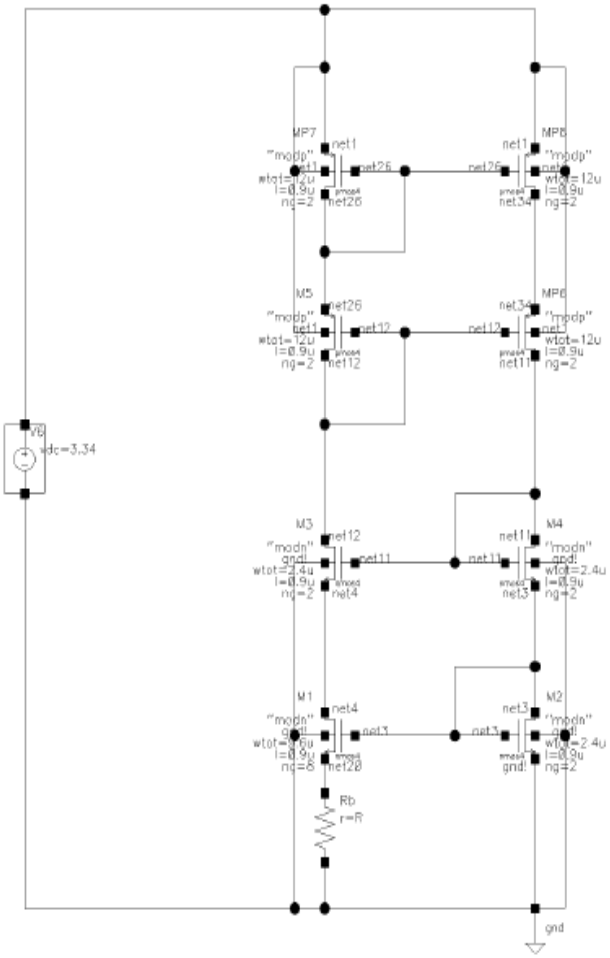

Fig. 7 Beta-Multiplier

TABLE II
VALUES OF COMPONENTS IN BETA-MULTIPLIER

Component	Value
M1	8x1.2μm/0.9μm
M2	2x1.2μm/0.9μm
M3	2x1.2μm/0.9μm
M4	2x1.2μm/0.9μm
M5	2x6μm/0.9μm
M6	2x6μm/0.9μm
M7	2x6μm/0.9μm
M8	2x6μm/0.9μm
R_b	11.8K ohms
R_a	27.5K ohms

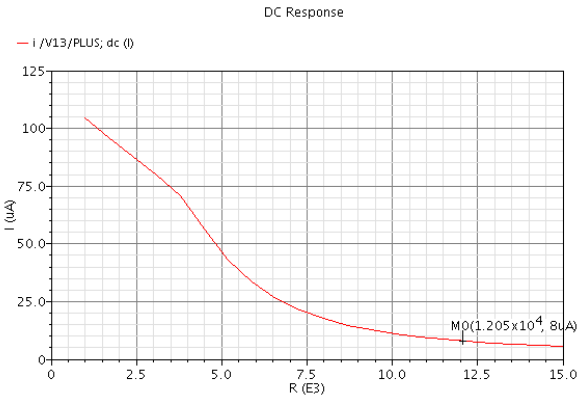

Fig. 8 DC sweep analysis to determine value of R_b

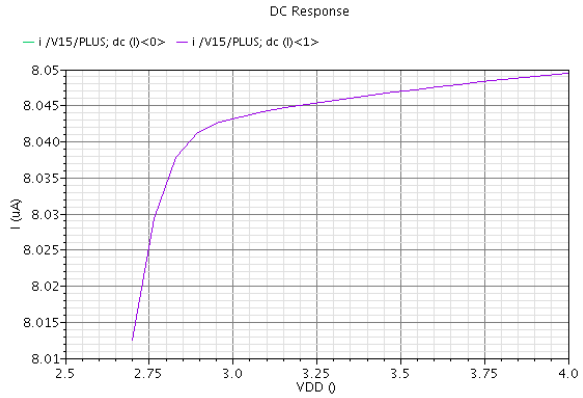

Fig. 9 Variation in Bias current with supply voltage V_{DD}

The differential pair is active loaded with the NMOS current mirror due to the following two reasons

--The active load leads to a differential to single ended conversion, [9]

--The active load gives an increased output impedance of the differential pair [9], given in (5)

$$R_o = r_{ds10} \parallel r_{ds12} \tag{5}$$

$$R_o = \frac{1}{g_{ds10} + g_{ds12}} \tag{6}$$

--The basic differential amplifier requires resistors for the output and gain, and these resistors require large chip area, hence by using active loads, the resistors are replaced by transistors and hence much of the area is saved.

The differential gain of the differential pair is given by (7) [10].

$$A_{v1} = g_{m9}(r_{ds10} \parallel r_{ds12}) \tag{7}$$

The transistors M13 and M14 are the current mirrors of the transistors in beta-multiplier, so their size is determined by the current we want to source in the differential pair changing the number of fingers or gates. For instance, if the beta multiplier transistor has a reference current of 8μA with two fingers, so

to generate a current of 24μA in the differential pair, the number of fingers required for M13 and M14 are

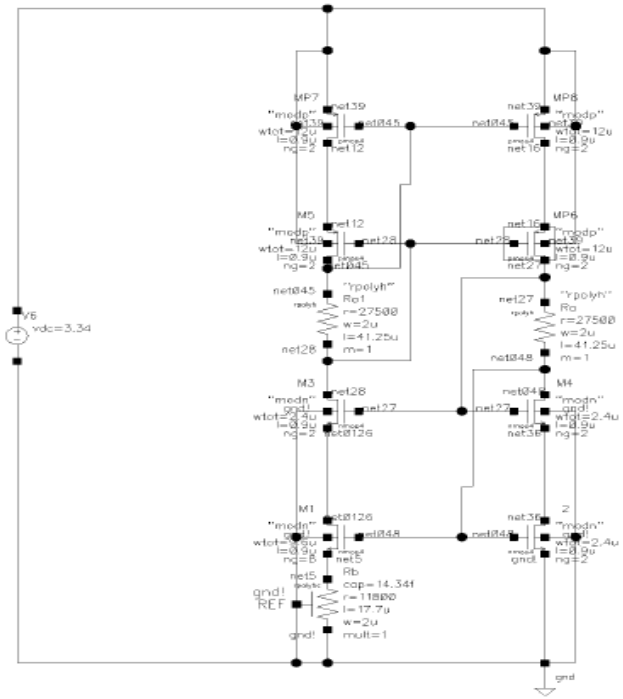

Fig. 10 Stable Beta-Multiplier with Resistance R_a added

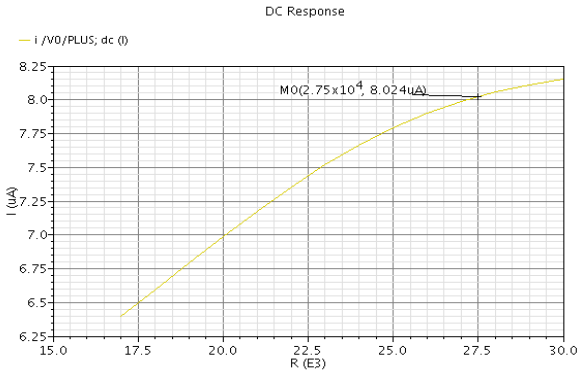

Fig. 11 DC sweep analysis to determine the value of Ra

$$Number\_of\_fingers = \frac{24}{8} \times 2 = 6\ fingers \quad (8)$$

the current at which the input differential pair is biased depends on various factors like gain bandwidth product (GBW), slew rate, and meeting the overall power requirement. The current selection will be discussed in the following sections when we discuss about the slew rate and GBW.

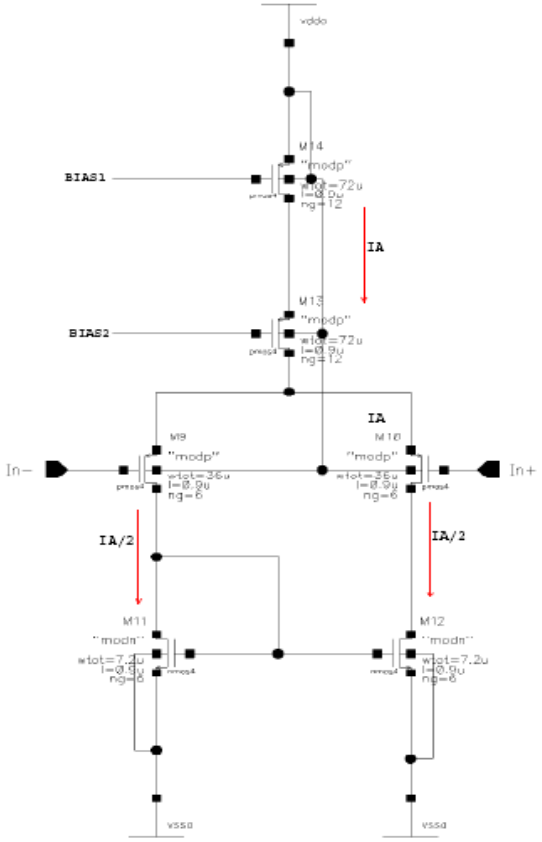

Fig. 12 Differential Input Stage

E. Gain Stage

The gain stage, which is the second stage of the two stage opamp, is a N-channel common source amplifier active loaded with the PMOS current source as shown in Fig. 13. The gain of the active loaded common source amplifier is given in (9) [10].

$$A_{v2} = -g_{m15}\left(r_{ds16} \,\|\, r_{ds15}\right) \quad (9)$$

The biasing current through this stage is also determined by the slew rate requirement, and will be discussed in the following sections.

F. Pole Splitting and Miller Compensation

A miller compensation capacitor is added between the input and the output of the gain stage so as to move the pole lowest in frequencies to lower frequencies and the one at high frequency to higher frequencies and achieve more stability at the cost of reduced speed. To have the required GBW (10) is used [11], [12].

$$f_{un} = \frac{g_{m10}}{2\pi C_c} \quad (10)$$

where f_{un} is the GBW, C_c is the miller compensation capacitor as shown in Fig. 13 and controls the dominant first pole.

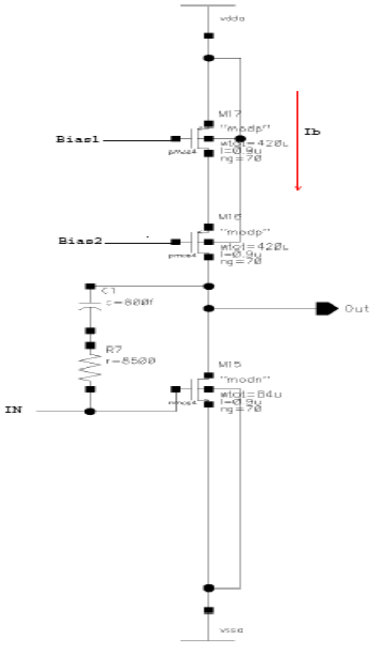

Fig. 13 Common Source Amplifier with Miller Capacitor and Lead Compensation

G.Lead Compensation and Zero Cancellation

To cancel the right half plane zero altogether, resistor R_c is connected in series with C_c with value given by (11) [12]

$$R_c = \frac{1}{g_{m7}} \quad (11)$$

to cancel the effect of left half plane non-dominant zero, the value of R_c is increased further than the one given by equation, to move the zero further into left half plane.

H.Complete Two Stage Op-amp

The complete two stage op-amp with the bias circuit and a load capacitor C_L at the outptut is shown in Fig. 14. The total gain of this two stage op-amp is given by multiplying the gain of each stage as given in (7), (9) as

$$A_v = A_{v1} \times A_{v2} \quad (12)$$

I. Slew-Rate

Slew rate is the maximum rate of change of output voltage in response to a large input differential signal, which causes one transistor of the differential input to turn off completely and the other to completely conduct all the current [13]. Consider the two stage op-amp as shown in Fig. 14 with a load capacitor C_L at the output. The current I_b in the common source amplifier branch is responsible for the charging of the load capacitor C_L. So for the charging cycle slew rate is governed by (13)

$$Slew\,Rate_{rising\,egde} = \frac{I_b}{C_c + C_L} \quad (13)$$

for the falling edge the, slew rate is governed by the current I_a in the differential pair branch given by

$$Slew\,Rate_{Falling\,Edge} = \frac{I_a}{C_c} \quad (14)$$

J. Design Procedure

According to the specifications requirement in Table III, a low frequency gain of greater than 80db is required. As this is a two stage op-amp design, the gain of each stage is determined individually. First the gain of the differential stage is determined only. The differential pair is biased at current of 24μA initially which implies that a current of 12μA will be flowing in the each of the input PMOS M9 and M10, and their active loads also. The sizes can then be easily determined as given in Table IV. The open loop gain of the differential stage is determined using the AC analysis and found to be 42.9dB as shown in Fig. 15.

TABLE III
SPECIFICATION REQUIREMENT

Design Parameter	Value
Open Loop Gain A_{OL}	>80dB
Phase Margin	>50°
Gain Bandwidth Product (GBW)	>15MHz
Slew rate	>20V/μs
Load C_L	10pF
Total Current Idd	< 350μA
Power Supply	V_{DD}=1.67V, V_{SS}=-1.67V, Gnd=0V

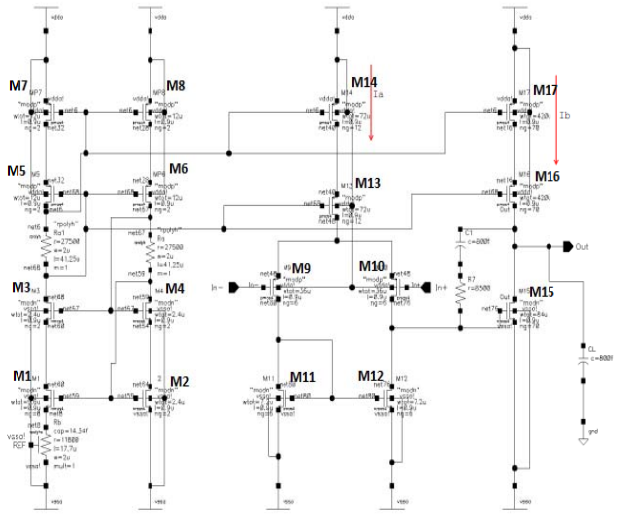

Fig. 14 Two Stage Op-Amp with Load Capacitor C_L

A common source (CS) configuration amplifier is then added to form the complete two stage op-amp. It is also biased at a bias current of 24μA, along with miller compensation capacitor C_c and lead compensation resistor R_c, with values set to 1pF and 1K ohms, respectively. The width of the transistors in CS stage is given in Table IV. The complete open loop gain of the two stage op-amp with a load capacitor C_L of 10pF at the output is found to be 93.72dB as shown in Fig. 16. The test circuit for measuring the open loop gain is shown in Fig. 17.

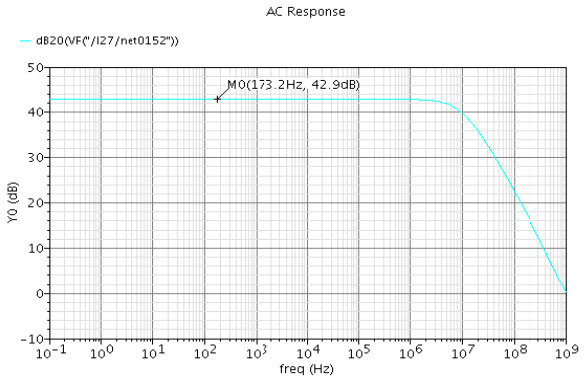

Fig. 15 Differential Stage Gain

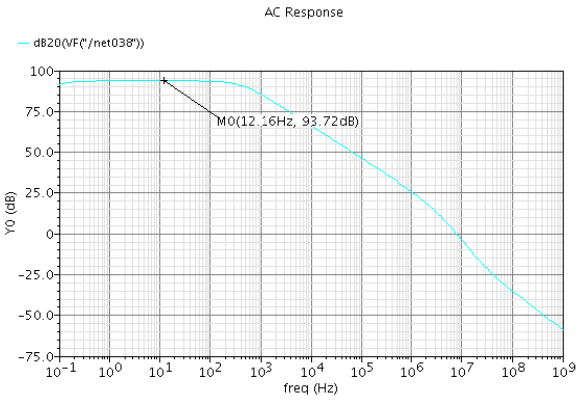

Fig. 16 Gain of Two Stage Op-Amp

TABLE IV
SIZE OF TRANSISTORS FOR I_A AND I_B OF 24μA

Component	Value
M13, M14, M16, M17	6x6μm/0.9μm
M9, M10	3x6μm/0.9μm
M11, M12	3x1.2μm/0.9μm
M15	6x1.2μm/0.9μm
C_c	1pF
R_c	1K Ohm
C_L	10pF

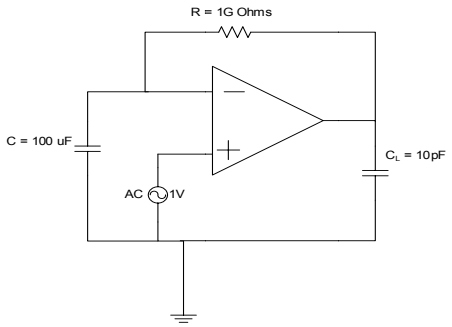

Fig. 17 Test Setup to Measure Open loop Gain

From the (13) and (14), it can be seen that for the slew rate requirement

$$\frac{I_a}{C_c} \geq 20V/\mu s \tag{15}$$

$$\frac{I_b}{C_c + C_L} \geq 20V/\mu s \tag{16}$$

As C_L is 10pF and suppose C_c is 1pF, so

$$I_a \geq 20\mu A, \quad I_b \geq 220\mu A \tag{17}$$

The current I_a in the differential stage is made 24μA and current I_b in the gain stage is adjusted to 260μAby changing number of fingers in the biasing transistors in these stages. The slew rate is then measured with the test circuit shown in Fig. 18.

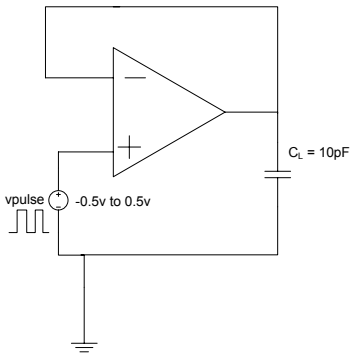

Fig. 18 Test Circuit to Measure Slew Rate

The slew rate for the rising and the falling edge are shown in Fig. 19 and Fig. 20, respectively.

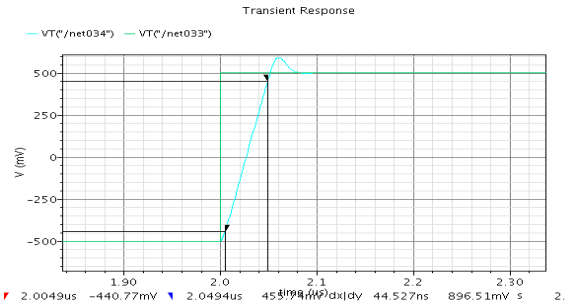

Fig. 19 Slew Rate of 2.01v/us for Rising Edge

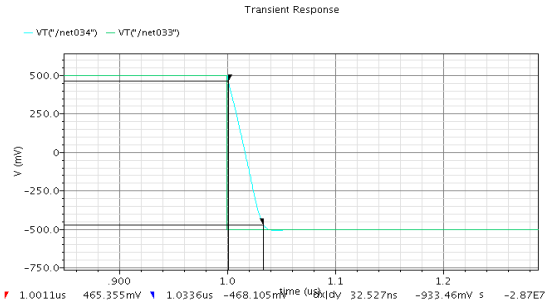

Fig. 20 Slew Rate of 2.87v/us for Falling Edge

To adjust for the value of GBW and phase margin the values of C_c and R_C are determined using (10), (11) and DC analysis which are recorded in Table V. The graph for GBW and phase margin is shown in Fig. 21.

To measure the total current drawn, it is measured at the power supply and averaged using the calculator in the tools.

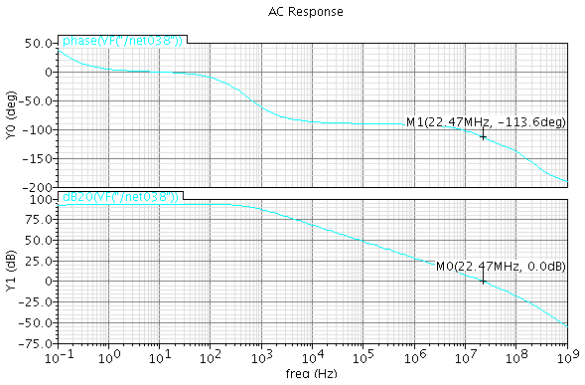

Fig. 21 Gain Bandwidth Product and Phase Margin

TABLE V
RESULTS FOR INITIAL DESIGN

Parameter	Value
Open Loop Gain	93.73dB
Gain Bandwidth Product	22.47MHz
Phase Margin	66.4°
Slew Rate	20.1V/μs(Rising), 28.7V/μs(Falling)
Idd	320μA
I_a (Current in Differential pair)	24μA
I_b (Current in CS Amplifier)	260μA
C_c	800fF
R_c	4K Ohm
C_L	10pF

K. Design Improvement for High Performance

After meeting the design specifications, variations in the design are made, for high performance fastest design in terms of GBW. From (10), it is quite evident that increasing transconductance g_m of the differential pair tends to increase the GBW. So to increase g_m, the biasing current I_a through the differential pair is doubled to make it 48μA, so that GBW increases. The bias current of 280μA is used for the CS amplifier stage. Hence, I try to achieve high performance at the cost of high power and large area. The values of C_c and R_c are determined using (10) and (11) along with the DC analysis, and tweaked to get the best performance. Fig. 22, shows GBW of 57.01MHz and phase margin of 56°. The slew rate has also improved a lot as can be seen in the Fig. 23 and Fig. 24. The results are summarized in Table VII.

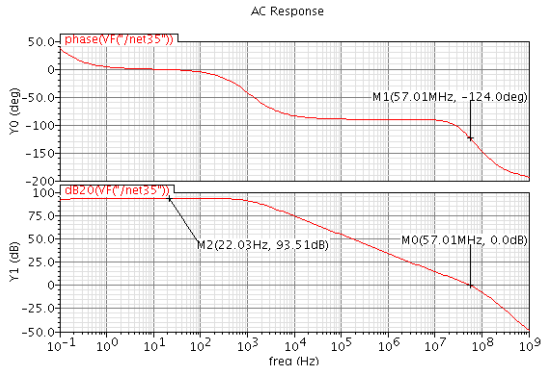

Fig. 22 Gain Bandwidth Product and Phase Mrgin of Improved Design

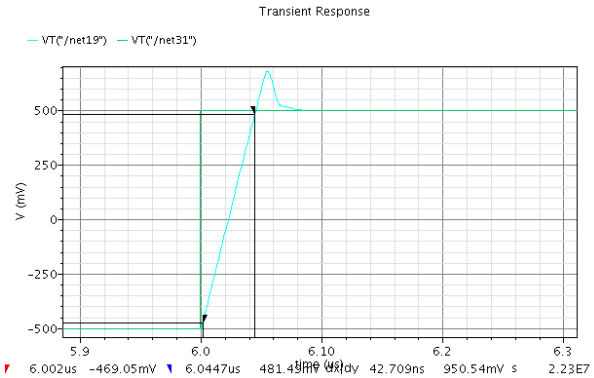

Fig. 23 Improved Rising Edge Slew Rate

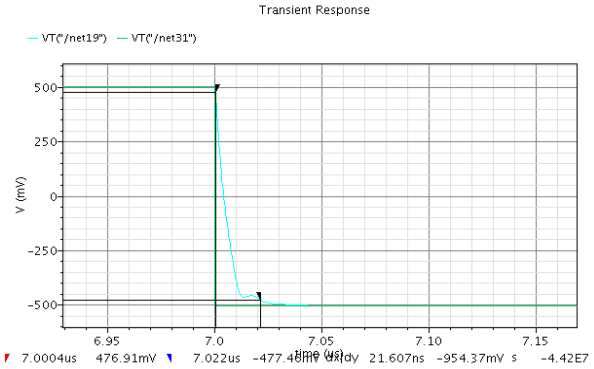

Fig. 24 Improved Falling Edge Slew Rate

It was also observed during various experiments and simulations that increasing the lead compensation resistance R_c, improves the GBW and slew rate, but degrades the phase margin.

TABLE VI
TRANSISTOR SIZE FOR IMPROVED PERFORMANCE DESIGN

Parameter	Value
M9, M10	6x6µm/0.9µm
M11, M12	6x1.2µm/0.9µm
M13, M14	12x1.2µm/0.9µm
M15	70x1.2µm/0.9µm
M16, M17	70x6µm/0.9µm

TABLE VII
RESULTS FOR IMPROVED PERFORMANCE DESIGN

Parameter	Value
Open Loop Gain	93.51dB
Gain Bandwidth Product	57.01MHz
Phase Margin	56°
Slew Rate	22.3V/µs(Rising), 44.2V/µs(Falling)
Idd	347µA
I_a (Current in Differential pair)	48µA
I_b (Current in CS Amplifier)	280µA
C_c	800fF
R_c	8K Ohm
C_L	10pF

III. LAYOUT DESIGN

A. Floor Plan

To have a compact and good layout design, floor planning is done prior to starting the layout [14]. The floor plan for the two stage op-amp designed is shown in Fig. 25.

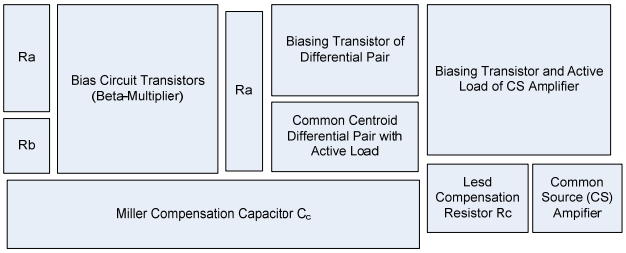

Fig. 25 Floor Plan for Layout Design

B. Resizing of Transistors

The transistors in the common source amplifier stage are of big sizes as given in Table VI, and are absurdly shaped when extracted into schematic, so these transistors are resized to have a more compact square shape [15], but should source the same biasing current for the CS amplifier. DC analysis is again performed to see if the active loads still bias the same current as before resizing. The new sizes are given in Table VIII.

TABLE VIII
RESIZING OF TRANSISTORS IN CS

Parameter	Value
M15	12x5.85µm/0.9µm
M16, M17	12x31.25µm/0.9µm

C. Common Centroid and Matching of the Transistors

During the doping and the fabrication, the substrate cannot be uniformly doped and hence there are slight differences in the parameters of two identical transistors fabricated on the same silicon wafer. But there are some transistors that need to be matched as closely as possible, like the current mirrors in the biasing circuit and differential input pair along with its active load in the differential input stage. The closer the transistors are the more precisely they are matched. Various techniques have been developed like having inter-digitization and common centroid for matching.. I have used the latter

technique for matching, as it provides with a more closely matched pair.

In common centroid, the two transistors to be matched are split into various fingers, which are then placed in an interleaved manner, in a manner to have a common center of the two transistors, as shown in Fig. 26. I have used common centroid for the transistors making up the current mirrors in the biasing circuit, differential input pair and the active load of the differential pair.

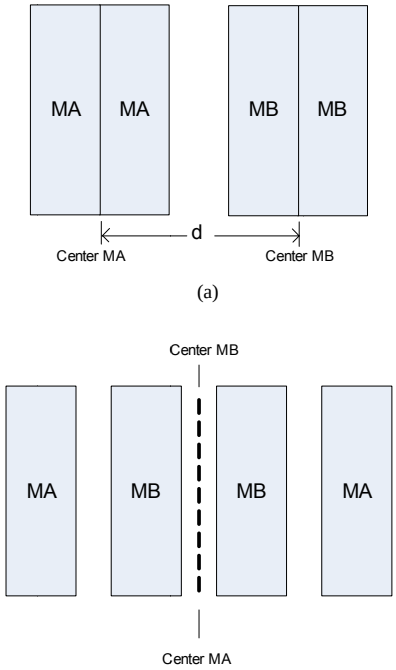

Fig. 26 (a) Transistors A and B with two fingers each and their centers separated by d. (b) Transistors Split to form Common Center point, hence Common Centroid

To break up a transistor into multiple transistors, the transistors were broken into multiple transistors connected in parallel, so to have the same width. A new symbol was created that contained these multiple transistors, which was then extracted into layout. The common centroid structure I use for various transistors is given in Table IX. A layout view of the common centroid differential pair is shown in Fig. 27.

TABLE IX
COMMON CENTROID OF TRANSISTORS

Transistor	Combination
M1, M2	M1M1 M2 M1M1M1M1 M2 M1M1
M3,M4	M4 M3M3 M4
M5, M6	M6 M5M5 M6
M7,M8	M8 M7M7 M8
M9,M10	M9M9 M10M10M10 M9M9 M10M10M10 M9M9
M11,M12	M11M11 M12M12M12 M11M11 M12M12M12 M11M11

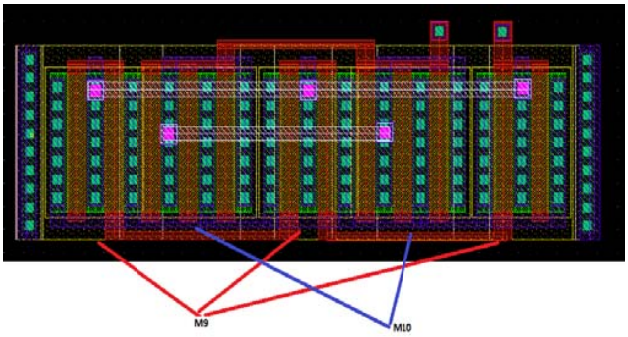

Fig. 27 Differential Pair Common Centroid

D.Layout Area, Extraction and LVS

The complete layout area is 7392 $(\mu m)^2$. After the layout, the extraction was one done successfully. In the extracted view, layout view versus schematic view (LVS) check was done. Initially some mismatches were there related to the mismatch of the resistors, but the issue was resolved by replacing resistor rpolyh by rpolyhc in schematic. LVS was passed successfully, with the net-list of both the views matched. After successful LVS, extraction was done with parasitics, and analog build was generated. The layout view is shown in Fig. 28 The comparison in the results of the schematic and the layout will be done in the following results section.

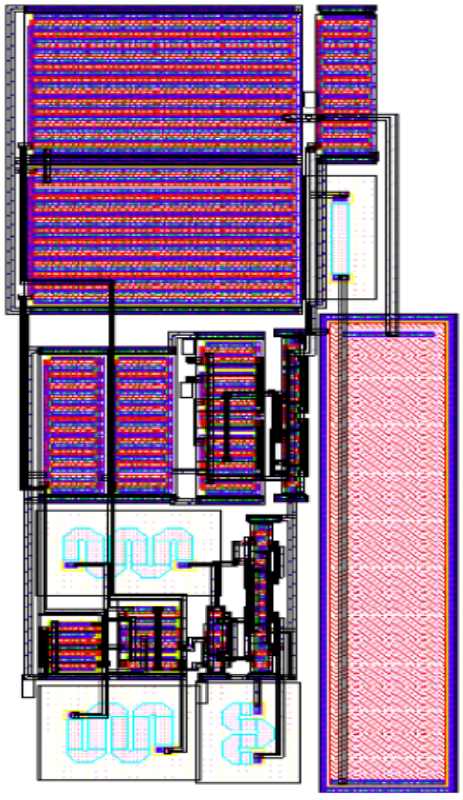

Fig. 28 Complete Layout View

IV. Results and Comparison

The results of the GBW,phase margin and slew rate after parasitic extraction and analog build are shown in Fig. 28, Fig. 29 and Fig. 30.

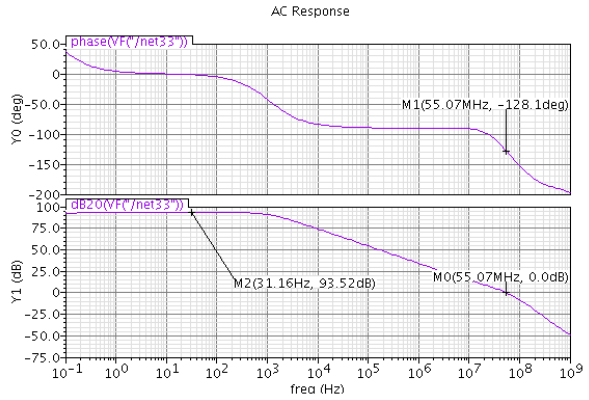

Fig. 29 Gain Bandwidth Product and Phase Margin after Layout and Parasitic Extraction

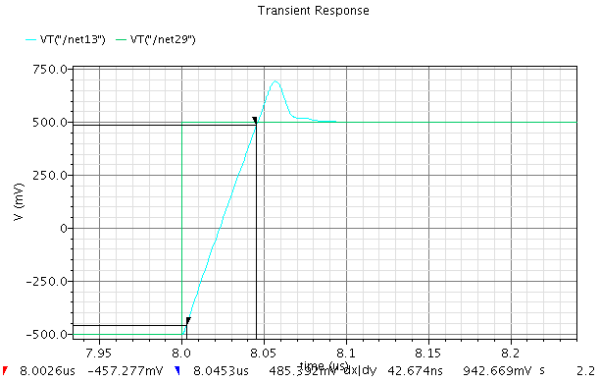

Fig. 30 Slew Rate of Rising Edge after Layout and Parasitic Extraction

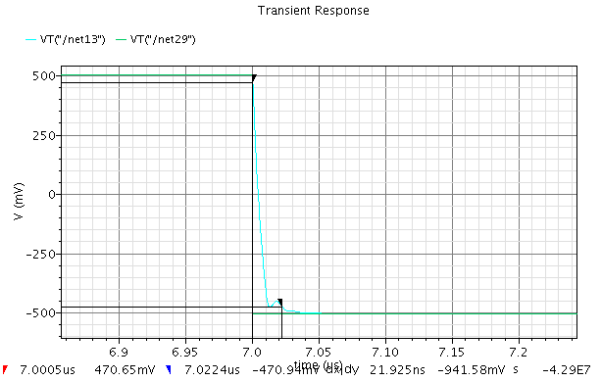

Fig. 31 Slew Rate of Falling Edge after Layout and Parasitic Extraction

It is observed from these results that the GBW, phase margin and slew rate have dropped by small amounts after layout.

The results along with the comparison with schematic results are summarized in Table X.

TABLE X
Results of Layout and Schematic

Parameter	Schematic	Layout	Difference
Open Loop Gain	93.51dB	93.52dB	-0.01dB
Gain Bandwidth Product	57.01MHz	55.07MHz	1.94MHz
Phase Margin	56°	51.9°	4.1°
Slew Rate	22.3V/μs(Rising), 44.2V/μs(Falling)	22.0V/μs(Rising), 42.9V/μs(Falling)	0.3/μs(Rising), 1.3V/μs(Falling)
Idd	347μA	344μA	-3μA

The circuit is also tested for robustness, by changing the supply voltage to ±20% of the given value. The results are summarized in Table XI. From the results in table XI it is quite evident that the overall design is robust to changes in power supply fluctuations.

TABLE XI
RESULTS OF LAYOUT and SCHEMATIC

Parameter	-20% of V_{DD}	+20% of V_{DD}
Open Loop Gain	91.88dB	94.29dB
Gain Bandwidth Product	55.56MHz	58.68 MHz
Phase Margin	56.3°	55.5°
Slew Rate	21.2V/μs(Rising), 42.5V/μs(Falling)	23.0V/μs(Rising), 45.3V/μs(Falling)

V. Conclusion

A two stage op-amp meeting the required specification and then making the design improvement to have high performance in terms of GBW of 55.07MHz was designed and implemented successfully in Cadence. The design is observed to be quite robust to fluctuations in supply voltage.

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