

# Cascaded H-Bridge Five Level Inverter Based Selective Harmonic Eliminated Pulse Width Modulation for Harmonic Elimination

S. Selvaperumal, M. S. Sivagamasundari

**Abstract**—In this paper, selective harmonic elimination pulse width modulation technique is employed to eliminate lower order harmonics like third by determination of solving non-linear equations. The cascaded H-bridge five level inverter is driven by the Peripheral Interface Controlled (PIC) Microcontroller 16F877A. The performance of single phase cascaded H-bridge five level inverter with relevant to harmonics and a variety of switches with solar cell as its input source is simulated by employing MATLAB/Simulink. A hardware model is developed to verify the performance of the developed system.

**Keywords**—Multilevel inverter, cascaded H-Bridge multilevel inverter, total harmonic distortion, selective harmonic elimination pulse width modulation, MATLAB.

## I. INTRODUCTION

THE demand for renewable energy has exaggerated considerably over the years due to a shortage of fossil fuels and atmospheric phenomenon. Among numerous kinds of renewable energy sources, solar energy and wind energy have become more popular and demanding because of advancement in power electronics techniques. Due to less maintenance and pollution free, photovoltaic (PV) sources are used in these days in several applications. The demand of solar electric energy has grown systematically by 20%–25% once a year over the past 20 years, that is especially because of the decreasing prices and costs. This decline has been driven by the following factors: 1) an increasing efficiency of solar cells 2) producing technology enhancements and 3) political economy of scale [1].

Multilevel inverter is employed to convert DC power obtained from PV modules into AC power to be fed into the grid. Rising the output waveform of the inverter reduces its harmonic content and, hence, the dimensions of the filter used and the level of magnetic force interference generated by on and off operation of the inverter. In recent years, multilevel inverters have become more popular for researchers and producers because of their benefits over existing three-level inverters. They provide improved output waveforms, smaller filter size, lower EMI and lower total harmonic distortion

(THD) [2].

The results of a patent search show that the structures of multilevel inverter circuits are around for over 25 years [16].

Today, multilevel inverters are employed in medium voltage levels with high-power applications [3]. The sector applications embody use in laminates, pumps, conveyors, compressors, fans, blowers, and mills. Many multilevel converter topologies are developed [4], [5]. Totally, three different topologies are proposed for multilevel inverters: cascaded multi cell with separate DC sources, diode clamped (neutral-clamped) and capacitor-clamped (flying capacitors) [6]. Each of those topologies incorporates a totally different mechanism for providing the voltage level. The primary topology introduced was the series H-bridge style, however many configurations are obtained for this topology [5]. Since this topology consists of series power conversion cells, the voltage and power levels are also scaled simply. The H-bridge topology was followed by the diode-clamped converter that utilized a bank of series capacitors [7]. The flying capacitor topology followed diode-clamped once few years rather than series connected capacitors, this topology uses floating capacitors to clamp the voltage levels [8]. H-bridge inverters have isolation transformers to isolate the voltage supply; however, they do not need either clamping diode or flying capacitor inverters. Moreover, several modulation techniques and control paradigms are developed for structures of multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic eliminated pulse width modulation (SHE-PWM), space vector modulation (SVM), and others [9], [10]. Additionally, several structures of multilevel converter applications target industrial medium-voltage motor drives [11], utility interface for renewable energy systems [12], flexible AC transmission system (FACTS) and traction drive systems [13], [14].

A typical single-phase two-level electrical inverter adopts full-bridge configuration by employing an approximate sinusoidal modulation technique as the power circuits. The output voltage has five voltage levels: zero, positive ( $+V_{dc}$ ,  $+2V_{dc}$ ) and negative ( $-V_{dc}$ ,  $-2V_{dc}$ ) DC voltage. The harmonic elements of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is prescribed to a certain degree. To overcome these demerits, this paper presents a five-level inverter whose output voltage can be explained in five levels because the variety of output levels will increase, the harmonic content is often reduced.

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This paper is organized as follows. After the introduction in Section I, Section II gives a top level view of cascaded h-bridge multilevel inverter structure topology. Then, the cascaded H-bridge five level inverter with PIC Microcontroller 16F877A is explained in Section III. Sections IV and V show the simulation and experimental results that validate the proper operation of the inverter. Conclusion and final remarks are given in Section VI.

## II. CASCADED H-BRIDGE FIVE LEVEL INVERTER TOPOLOGY

Fig. 1 shows the schematic of a single-phase cascaded h-bridge five level inverter. Cascaded h-bridge multilevel inverters are shaped by the series connection of additional two or several H-Bridge inverters. Each h-bridge has two phase legs with voltage source, wherever the L-L voltage is the converter output. Therefore, a single H-bridge inverter is ready to come up with three totally different voltage levels. Every leg has solely two possible on and off states, preventing short circuit capacitor. Here two legs are available, which consist of four switching states, though two of them have redundant output voltage. When two or more H-Bridges are connected in series, their output voltages are combined to make totally different output levels, increasing the total inverter output voltage and conjointly its rated power. The two H-Bridges connected in series is shown in Fig. 1.

## III. CASCADED MULTILEVEL INVERTER WITH PIC MICROCONTROLLER

The block diagram of proposed cascaded H-bridge inverter structure topology with SHE PWM is shown in Fig. 2. This method consists of multistage DC/AC power converter, filter and load. The cascaded h-bridge inverter is connected with DC sources. The five level inverter output is AC voltage which is connected to load through filter [15]. The load is considered as resistive and an inductive. The cascaded h-

bridge multilevel inverter is driven by the PIC microcontroller 16F877A. SHE PWM technique is employed to eliminate third order harmonics by determination of non-linear equations. SHE PWM technique is employed to seek out applicable shift angles specifically  $\theta_1, \theta_2, \theta_3, \dots$  therefore, that the (N-1) odd harmonics will be eliminated and control of the fundamental voltage is additionally achieved.

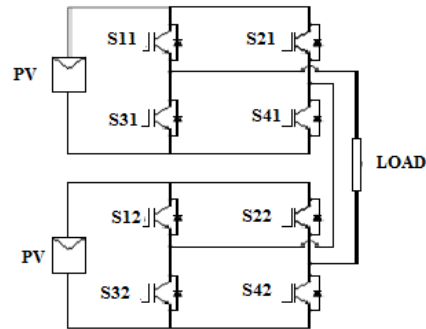


Fig. 1 Schematic of a single-phase cascaded five level inverter

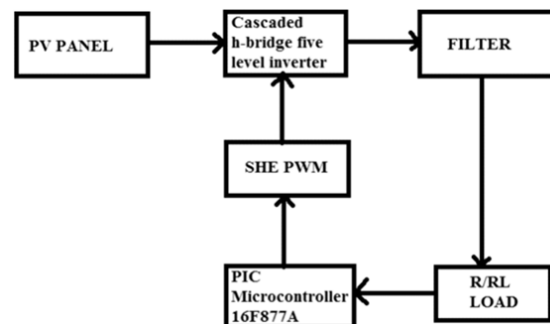


Fig. 2 Schematic of a single-phase cascaded five level inverter

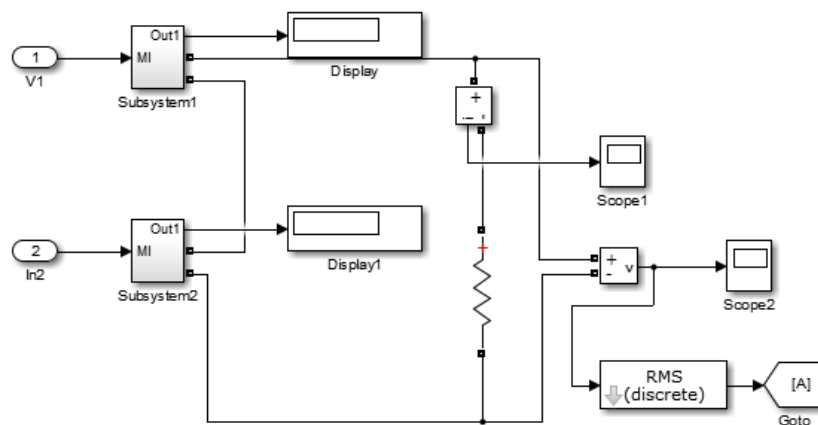


Fig. 3 Simulink model of the Cascaded MLI

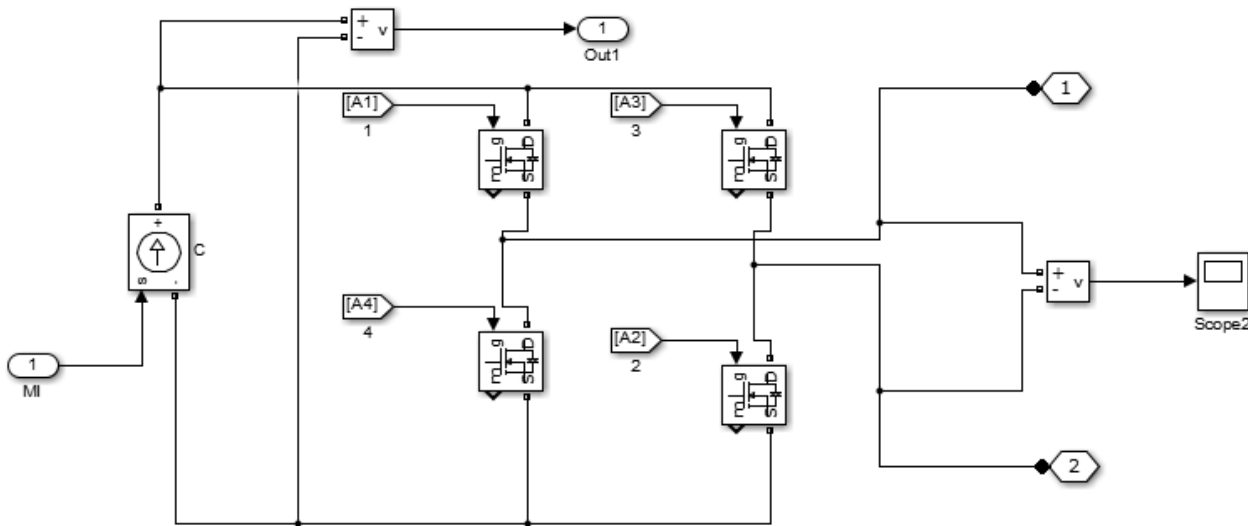


Fig. 4 Subsystem

#### IV. SIMULATION RESULTS

A simulation is carried out in MATLAB/Simulink software for a five level cascaded H-bridge inverter with isolated DC sources. The simulation model of cascaded h-bridge five level inverter topology is shown in Fig. 3 and the subsystem scheme is shown in FIG. 4. The power circuit consists of two h-bridges whose nominal DC voltage is taken into account as 18 V and therefore the five level stepped output voltages are obtained and the harmonics are reduced. Conjointly, it consists of a PWM generator block that has parameters as amplitude, pulse width period and phase delay which is used to determine the shape of the output.

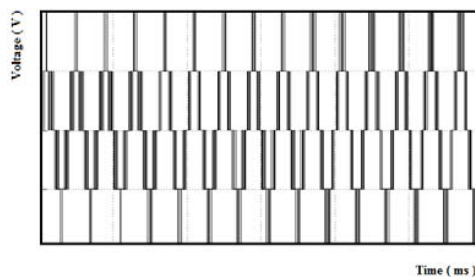


Fig. 5 Load voltage waveform

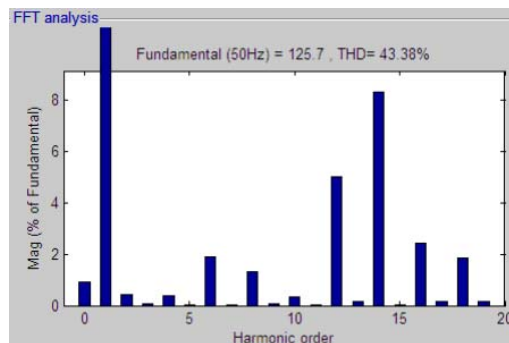


Fig. 6 THD

The response of the MLI with SHEPWM is satisfactory and the load voltage scheme is shown in Fig. 5. The THD waveform is shown in Fig. 6. It is determined from the results that the THD is 43.38%.

#### V. EXPERIMENTAL RESULTS

The experimental block diagram of proposed Cascaded H-bridge inverter topology with SHE PWM is shown in Fig. 7. This system consists of multistage DC/AC inverter, Optocoupler, PIC Microcontroller, filter and a load. The Cascaded H-bridge inverter is connected with DC sources. The five level inverter output is AC voltage that is connected to load through the filter.

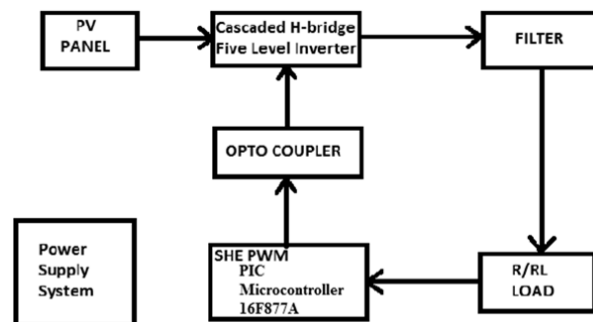


Fig. 7 Experimental block diagram

A single phase 100 W hardware prototype 5-level inverter as shown in Fig. 8 is built. It consists of two full-bridge inverters that are connected in an exceedingly series type. The inverter employs 8-A, 500-V MOSFETs and DC voltage of every h-bridge inverter is constant and is selected to be 34.8 V. Also, the frequency of the output is assumed to be 50 Hz. Six transformers (0-24 V, 2 A) are employed to power up the individual h-bridge inverters. Three transformers (6 V-0-6 V, 500 mA) are employed to power up the Optocouplers.

The real time implementation for choosing an inverter using PIC Microcontroller 16F877A is carried out during this work. SHEPWM generators and conjointly the control strategies for the chosen inverter are developed using MATLAB software.



Fig. 8 Load voltage waveform

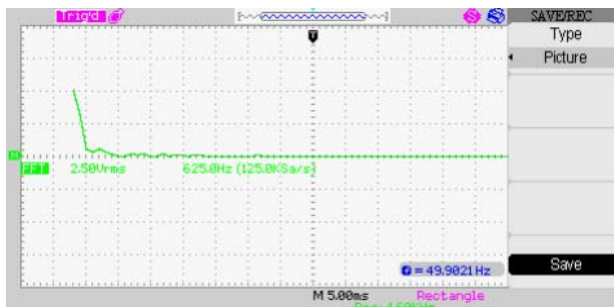


Fig. 9 Harmonic spectrum of the five level inverter output voltage

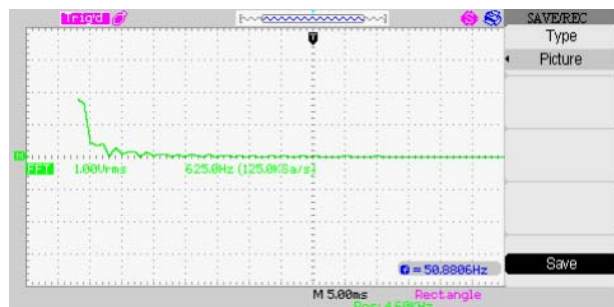


Fig. 10 Harmonic spectrum of the three level inverter output voltage

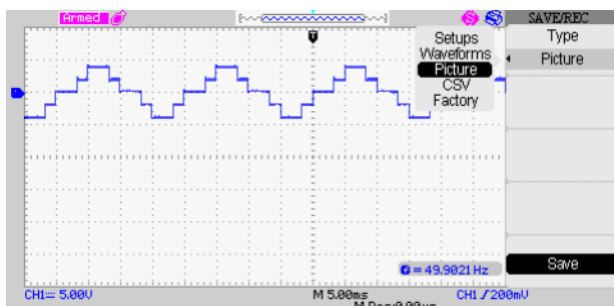


Fig. 11 Output voltage waveform (five level inverter)

Figs. 9 and 10 show the harmonic spectrum of the five levels and three level inverter output voltage. Figs. 11 and 12 show the output voltage waveform of the five levels and three level inverter. The elements and the parameters considered for

implementation are presented in below for the cascaded h-bridge five level inverter topology (see Table I).

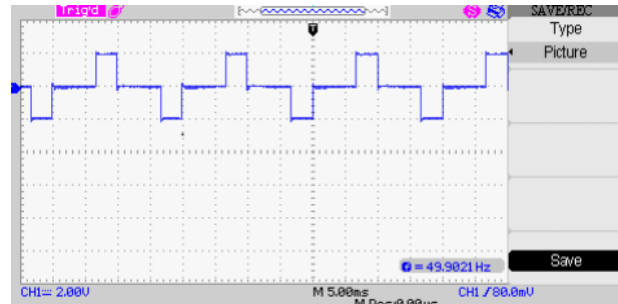


Fig. 13 IOutput voltage waveform (three level inverter)

TABLE I  
PARAMETERS OF THE CASCADED H-BRIDGE INVERTER

Parameters	Values
No. of H-Bridge levels	2
No. of Switches MOSFET IRF840 – 8Nos.	500 V, 8 A
DC source voltage for individual H- bridge	34.8 V/2 A
Fundamental frequency	50 Hz
R Load	100 Ohm
RL Load	100 Ohm, 10 mH
Optocouplers MCT2E (8 Nos.)	30 V, 3 A
Filter Capacitor	1000 $\mu$ F
Transformers (6 Nos.)	0-24 V, 2 A
Transformers (3 Nos.)	6 V-0-6 V, 500 mA

With reference to Table II a comparison of THD of the output voltage under modulation index  $M = 0.81$  has been done. It is evident that the results of simulation are closer to the experimental values.

TABLE II  
COMPARISON OF THD OF THE OUTPUT VOLTAGE

Controllers	Experimental	Simulation
PIC	43.33	43.38

## VI. CONCLUSION

In this paper, cascaded h-bridge five level inverter Simulink model has been proposed using MATLAB. The model includes the power circuit of cascaded h-bridge five level inverter, PIC Microcontroller and PV panel. The cascaded h-bridge five level inverter with PIC micro controller employing SHE PWM is found to be better when compared with the existing two level inverter. Experimental results are bestowed to verify the simulation results and evidenced that with this inverter strategy, third order harmonics are reduced.

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