International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:4, No:9, 2010

Analysis of a Novel Strained Silicon RF LDMOS

V.Fathipour*, M. A. Malakootian*, S. Fathipour* and M. Fathipour*

***Abstract*—**In this paper we propose a novel RF LDMOS structure which employs a thin strained silicon layer at the top of the channel and the N-Drift region. The strain is induced by a relaxed $Si_{0.8}$ $Ge_{0.2}$ layer which is on top of a compositionally graded SiGe buffer. We explain the underlying physics of the device and compare the proposed device with a conventional LDMOS in terms of energy band diagram and carrier concentration. Numerical simulations of the proposed strained silicon laterally diffused MOS using a 2 dimensional device simulator indicate improvements in saturation and linear transconductance, current drivability, cut off frequency and on resistance. These improvements are however accompanied with a suppression in the break down voltage.

***Keywords*—**High Frequency MOSFET, Design of RF LDMOS, Strained-Silicon, LDMOS.

I. Introduction

THE demand for cost effective, high linearity, high gain RF power transistors in applications such as base station power amplifiers as a result of broad implementation of wireless communications has urged the development of submicron high voltage Laterally Diffused MOS (LDMOS) transistor.

High voltage capability of this device is achieved by employing an n^--type diffusion region referred to as N-Drift to sustain most of the drain voltage. The N-Drift region however, degrades the on resistance and thus the RF performance of the device. A loss of 10% to 20% in drain source current, I_{DS}, and transconductance, g_m, is usually present in the extended drain power MOSFETs as compared to conventional MOSFETS [1]. Various techniques have been proposed for reducing the on resistance and improving other performance parameters of the LDMOS structure [2]-[5].The good high frequency response of this device is due to the laterally diffused graded channel referred to as "P-Base". The improved device transconductance, linearity and prevention of punch-through are other advantages of this laterally diffused channel and are due to the presence of a built-in electric field which accelerates the electrons towards the drain [6].

Enhancing the electron mobility in the channel of a MOSFET could potentially extend the performance limits of the existing MOS technology. In this paper we propose a novel Strained Silicon Laterally Diffused MOS (SS LDMOS) structure to enhance the high frequency response, high power performance and linearity of the conventional LDMOS. Furthermore, this technique provides the advantage of keeping the same circuit configuration as in standard Si technology [7].

Biaxial tensile stress in the silicon is attained when pseudomorphical silicon epitaxial-layers are grown on SiGe layers. The six fold degeneracy in the silicon conduction band minimum are split into two groups due to the applied tensile stress: two lowered valleys (Δ_2) with a longitudinal mass axis normal to interface and four raised valleys (Δ_4) with a longitudinal mass axis parallel to the interface. Due to the shifting of the relative energies of each band, most of the inversion electrons will occupy the two lower valleys [8]. This redistribution of electron population in which more electrons populate the lower valleys, results in the reduction of carrier conductivity effective mass in the direction of transport as well as reduction of the internally scattering rates [9]-[11]. The energy splitting between the lowered Δ_2 and raised Δ_4 valleys is given by $\Delta E_{strain} \approx 0.67x$, where x is the Ge fraction in the $Si_{1-x}Ge_x$ buffer layer. The strain also modifies the energy band gap E_G, which is empirically given by $E_G(x) = 1.11 - 0.4x$ (eV) [8].

In the next section, we discuss device fabrication steps. Section III is devoted to an extensive analysis of the device physics and its comparison with a conventional LDMOS device. We show that the proposed device exhibits improved drive current, transconductance, on resistance, R_{on} and cut off frequency, f_T as compared to the conventional LDMOS. Finally a conclusion is provided in section IV.

II. Fabrication process

The cross sectional view of the proposed device is shown in Fig. 1. The fabrication process starts by growing a p-type epitaxial layer ($N_A = 7\times10^{14}$ cm^{-3}) over a p^+ substrate. The graded SiGe buffer of 2.3μm thick is then grown with x composition varying from 0% to 20%. This layer adjusts the

Vala Fathipour is the postgraduate student of the Department of Electrical and Computer Engineering of the University of Tehran, P.O. Box 14395-515, Tehran, Iran (email:valafathi@gmail.com).

M. A. Malakoutian is the postgraduate student of the Department of Electrical and Computer Engineering of the University of Tehran, P.O. Box 14395-515, Tehran, Iran (e-mail: m.a.malakoutian@gmail.com).

S. Fathipour is the undergraduate student of the Department of Electrical and Computer Engineering of the University of Tehran, P.O. Box 14395-515, Tehran, Iran (e-mail: sarafathipour@yahoo.com).

M. Fathipour is the head of the Device and Simulation Lab., he is an IEEE member and is the associate professor of the Department of Electrical and Computer Engineering of the University of Tehran, P.O. Box 14395-515,Tehran, Iran (corresponding author to provide mobile: (+98 912) 147 32 09; phone: (+98 21) 88 02 04 03; e-mail: mfathi@ut.ac.ir).

*This research was carried out at the Device Modeling and Simulation Laboratory of the Department of Electrical and Computer Engineering of the University of Tehran.

intermediate lattice constant of the Si and SiGe materials and provides a defect free $Si_{0.8}Ge_{0.2}$ layer allowing structures of arbitrary thickness to lie on top of each other. The growth of the 4.04µm relaxed $Si_{0.8}Ge_{0.2}$ layer is followed by the epitaxial growth of a 38 nm thick silicon layer. The 38 nm silicon thickness accounts for the screening oxide and the thin dry gate oxide growth in the steps that follow. The optimized strained silicon thickness is left to be 16 nm. The strain layer in the channel and the N-Drift region allows a smooth transition of the conduction energy bands between these two regions.

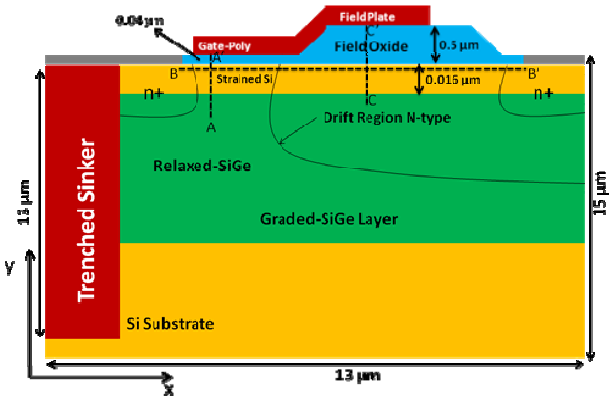


Fig. 1 Cross sectional view of the proposed SS LDMOS

Sinker structure is widely used for lateral power devices to decrease the number of contacts, reduce the source inductance and improve the RF performance. Furthermore, it makes the LDMOS integration easier. It is usually created by a high dose and high energy implant followed by a thermal drive step until it merges with the heavily doped p^+ substrate. However, due to the lateral diffusion a wide gate to sinker space is required and the sinker takes up much of the chip area [6]. In this structure instead of creating the heat sink via diffusion, a trenched-sinker of height 9µm is created by etching the relative locations and filling it with doped polysilicon [12]. Advantages of this method include the reduction of sinker area, lowering of the source resistance (which is due to the refilling of the sinker with heavily doped poly silicon), ability to be scaled to deep submicron regime and good RF performance. After the formation of sinker and growth of the 10 nm screen oxide, phosphorous is implanted (N_D= 7×10^{14} cm^{-3}) in the epitaxial layer to create the N-Drift region. To minimize the consumption of the underlying strained silicon layer, the growth of the gate oxide and field oxide is carried out in two steps: after etching the previous screen oxide layer, a thin dry oxide of 40 nm thick is grown, then the Field Oxide is deposited to a thickness of 500 nm at appropriate locations. The poly gate which extends over the 40 nm thick gate oxide and terminates on the field oxide is then deposited. This is followed by the source/drain region implantation. The annealing times and temperatures were properly chosen to achieve the desired profiles.

III. Modelling and Discussions

To implement the device with the 2D device simulator, following models are employed: the unstrained energy band model is chosen for the relaxed $Si_{0.8}Ge_{0.2}$ layer. The strained-Si structure is implemented by defining the energy band structure i.e. electron affinity, E_G, conduction band discontinuity, ΔE_C and valence band discontinuity, ΔE_V as well as the mobility. The mobility enhancement factor is chosen based on the experimental results given in [13]. The field dependant mobility model is chosen to take into account the mobility degradation which arises due to both large vertical and lateral electric fields. For transport, the drift diffusion and the impact ionization models are employed. A comparison between the electrical characteristics of the proposed device with those of a conventional LDMOS is provided next. The devices under consideration have the same doping profiles and physical dimensions.

A. Energy band Diagram

The energy band profile is modified by the strain in the channel and N-Drift region of the SS LDMOS. The simulated energy band diagrams for V_{GS}=0V and V_{DS}=0V calculated along the cut lines AA' and BB' in Fig. 1 are plotted in Fig. 2 and Fig. 4. Fig. 2 compares the energy band diagram of the proposed device with that of the conventional LDMOS along cut line AA'. A band edge discontinuity arises at the strained silicon and $Si_{0.8}Ge_{0.2}$ alloy heterojunction. The higher electron affinity of the strained silicon device as compared with that of the unstrained silicon device together with the negative valence band offset at the strained Si/SiGe interface [14] causes the conduction band to shift towards the Fermi level and results in the contribution of more electrons in the channel for the same gate bias. This is verified by the greater carrier concentration in the strained silicon layer calculated along cutline AA' as shown in Fig. 3. As a result the threshold voltage reduces for the SS LDMOS as compared to the conventional LDMOS [14]. The threshold voltages of the conventional LDMOS and the SS LDMOS are 3.5 and 3 respectively.

Fig. 4 gives a comparison between the conduction band energy for the proposed and conventional devices along the cutline BB'. As well as indicating the greater electron affinity of the strained silicon device as compared with the conventional device, this figure shows the fact that the use of strain both in the top layer of the channel and the N-Drift region eliminates the energy spike at the heterojunction. Presence of this spike reduces the electron speed towards the drain [1].

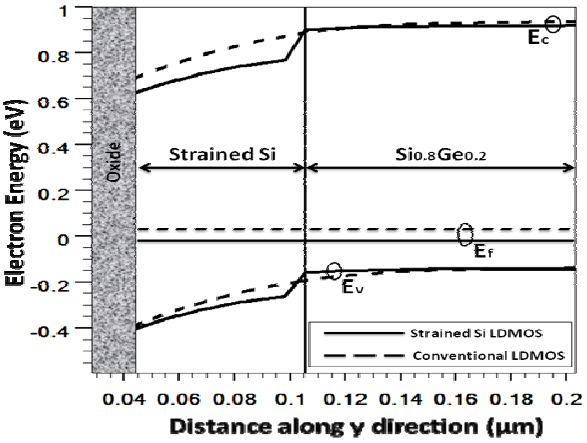


Fig. 2 Energy band diagrams of the SS LDMOS and conventional LDMOS calculated along cutline AA'.

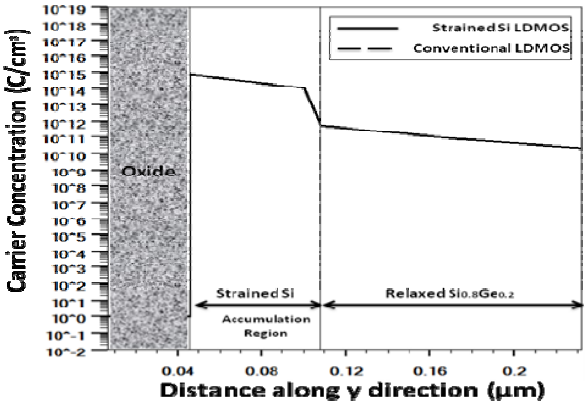


Fig. 3 Carrier concentration profile of SS LDMOS calculated along cut line AA'.

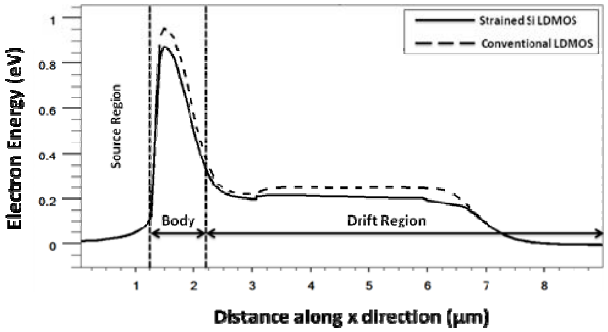
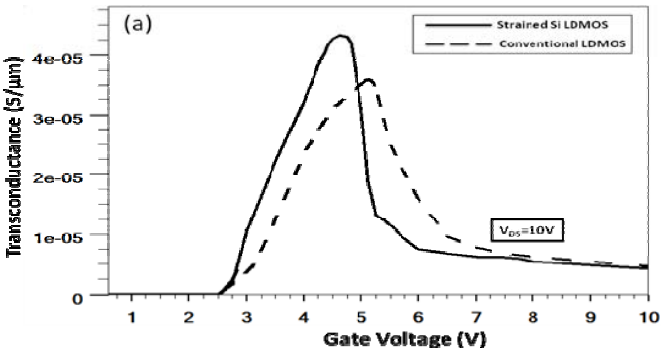
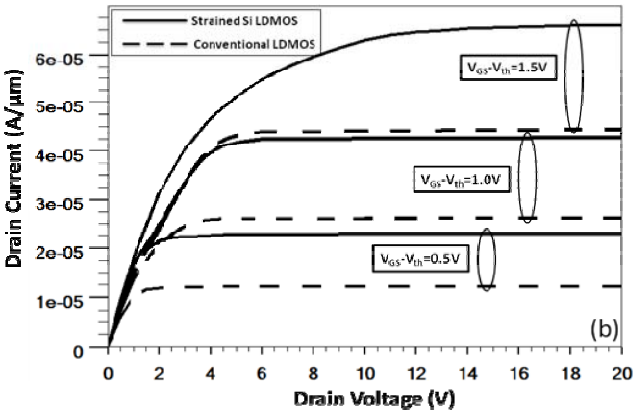


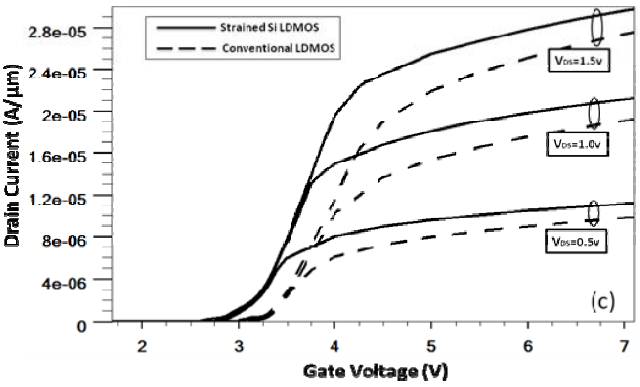
Fig. 4 Energy band diagrams of the SS LDMOS and conventional LDMOS calculated along cutline BB'.

B. Current –Voltage Characteristics

Fig. 5.a shows a comparison between the g_m-V_{GS} characteristics of the conventional LDMOS and the SS LDMOS in the saturation region. The peak saturation transcondutance of the proposed SS LDMOS occur at a 0.8V lower gate voltage compared to the conventional device. As mentioned earlier in section A, this voltage reduction is due to the carrier confinement which results due to the conduction band bending at the hetrojunction. The carrier confinement causes a larger number of carriers to respond to the small signal voltage applied at the gate as compared to the conventional device. Thus the transconductance of SS LDMOS is improved by 45.5% and 19.3%in the linear and saturation regions respectively. However, after a certain gate voltage the g_m improvement rate decreases and even starts to degrade. This is due to the degradation of the mobility enhancement factor beyond a certain gate voltage which is a result of increased on resistance of the device and is discussed next.







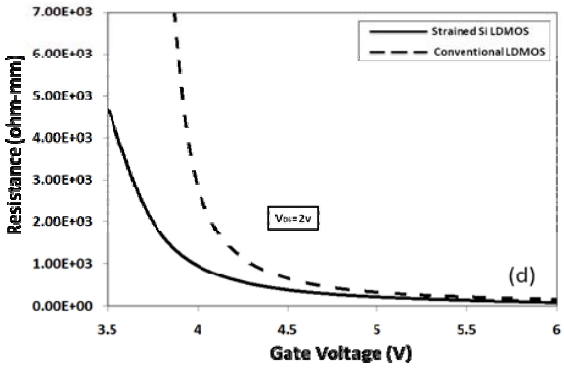


Fig. 5 (a) Saturation transconductance (b) I_{DS}-V_{DS} characteristic (c) I_{DS}-V_{GS} characteristics and (d) On resistance of the SS LDMOS as compared to conventional LDMOS

Fig. 5. b compares I_{DS}-V_{DS} characteristics of the SS LDMOS and conventional LDMOS structures. Due to the enhancement of the effective electron mobility at low transverse fields and the reduction of threshold voltage a significant increase in current for the SS LDMOS is observed from the figure. The improvement in current decreases as the gate voltage increases. This is attributed to the degradation of mobility enhancement factor. The transfer characteristic (I_{DS}-V_{GS}) for the devices under consideration is depicted in Fig. 5.c. The 2 sets of curves for the SS LDMOS and the conventional LDMOS, tend to get closer and will meet each other for large gate voltages (not indicated in this figure). This can be explained by examining the on resistance of the device for different V_{GS} values. Fig.5. d shows the on resistance for devices under consideration. R_{on} is the ratio of applied V_{DS} to I_{DS} in the triode region of operation. For low V_{GS} values R_{on} of SS LDMOS is much lower than the conventional LDMOS. Detailed investigation of data indicates that for V_{DS}=2V, as V_{GS} increases above 12 V the on resistance of SS LDMOS becomes larger than the conventional LDMOS.

C. Cut off Frequency

Results obtained from simulation analysis confirm the fact that the cut off frequency for the SS LDMOS is enhanced by a factor of 22.3% at V_{DS}=10V as compared with the conventional LDMOS. This may be attributed to the enhancement in g_m for this device.

A. Drain Breakdown voltage

Breakdown occurs when avalanche multiplication results in a significant current to flow between the source and drain. The smaller energy band gap and longer mean free path of strained-Si devices result in higher impact ionisation rates for these devices as compared with those of the bulk silicon devices [1]. The breakdown, voltage, VB of a strained-silicon/SiGe heterostructure can be degraded by a positive temperature coefficient of impact-ionization rate [15]. Irisawa *et al.* [16] reported a higher impact-ionization current for a strained-silicon MOSFET as compared to a conventional MOSFET.

In this paper the breakdown is reported as the drain to source voltage at which I_{DS} crosses the 10pA/μm limit when the device is off [12]. The band gap narrowing causes the breakdown voltage of the SS LDMOS to be degraded by 15.6% as compared with the conventional LDMOS device. This is shown in Fig. 6.

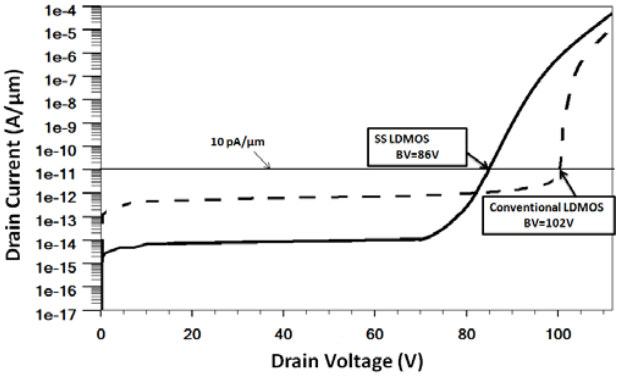


Fig. 6 Comparison of the breakdown voltage curves for the SS LDMOS and conventional LDMOS

The percentage improvements obtained in the output characteristics of the proposed SS LDMOS is given in table I.

TABLE I
A COMPARISON BETWEEN THE OUTPUT CHARACTERISTICS OF THE SSLDMOS AND THE CONVENTIONAL LDMOS

Output Characteristics	Bias Condition	Percentage improvement
I_D	V_{GS}=5V	51.1%
I_D	V_{GS}=4.5V	64.7%
I_D	V_{GS}=4V	83.3%
f_T	V_{DS}=10V	22.3%
VB	I_{DS}=10pA/μm	-15.6%
g_m	saturation	19.3%
g_m	linear	45.5%
R_{on}	V_{GS}=4.5V, V_{DS}=2V	27.7%

IV. Conclusion

With the aid of a 2D device simulator, we have shown that the strain layer in the channel and N-Drift region of an LDMOS structure leads to great improvements in the device performance. The carrier confinement in the strained silicon layer which is the result of 20% Ge content in the underlying SiGe layer causes improvements of 19.3%, 45.5%, 51.1%, 22.3% and 27.7% in saturation and linear transconductance, current drivability at V_{GS}=5V, cut off frequency at V_{DS}=10V and on resistance at V_{GS}=4.5V respectively for low transverse fields. However, at the same time the breakdown voltage is

degraded by 15.6%. As a result the SS LDMOS may prove as a good candidate for future higher-speed CMOS devices and applications like display drivers due to their needs for large current drivability and small chip area consumption.

REFERENCES

[1] Y. K. Cho, T. M. Roh and J. Kim, "A New Strained –Si Channel Power MOSFET for High perfor,ance Applications," ETRI Journal , vol. 28, no. 2, pp. 253-256, April 2006.

[2] D. Ueda, H. Takagi, and G. Kano, "An ultra-low on-resistance power MOSFET fabricated by using a fully self-aligned process," *IEEE Trans. Electron Devices*, vol. ED-34, no. 4, pp. 926–930, Apr. 1987.

[3] R. P. Zingg, "On the specific on-resistance of high-voltage and power devices," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 492–499, Mar. 2004.

[4] P. Li, Y. Su, M. You, and X. Li, "Novel power MOS devices with SiGe/Si heterojunctions," in *Proc. ISPSD*, Toulouse, France, May 22–25, 2000, pp. 109–112.

[5] C. Hu, M. H. Chi, and V. M. Patel, "Optimum design of power MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-31, no. 12, pp. 1693–1700, Dec. 1984.

[6] F.M. Rotella at al., "Modeling, Analysis and design of RF LDMOS Devices Using Harmonic-Balance Device *Simulation,"* IEEE Transactions on microwave theory and techniques, Vol.48, No.6, June 2000.

[7] D. Vasileska, G. Formicone and D. Ferry, "Doping dependence of the mobility enhancement in surface-channel strained-Si layers," Nanotechnology 10 (1999) 147–152. Printed in the UK.

[8] J. B. Rold´any, F. G´amiz, J. A. L´opez-Villanueva and J. E. Carceller, "Understanding the improved performance of strained $Si/Si_{1-x}Ge_x$ channel MOSFETs," Semicond. Sci. Technol. **12** (1997) 1603–1608. Printed in the UK.

[9] J. Welser, J. L. Hoyt and J.F. Gibbons, "Electron mobility enhancement in strained Si n-type metal-oxide semiconductor field-effect transistors," *IEEE Electron* Device Lett. 15 100, 1994.

[10] F. G´amiz, J.B. Rold´an, J.A. L´opez-Villanueva and P. Cartujo, "Coulomb scattering in strained-silicon inversion layers on $Si_{1-x}Ge_x$ substrates," *Appl. Phys. Lett.* **69** 797, 1996.

[11] J.B. Rold´an, F. G´amiz, J.A. L´opez-Villanueva and J.E. Carceller, "A Monte Carlo study on the electron-transport properties of high-performance strained Si on relaxed Si1−*x*Gex channel MOSFETs," J. Appl. Phys. 80 5121–8, 1996.

[12] C. S. Kim, S. D. Kim, M. Y. Park, and H. K. Yu, "Trenched sinker LDMOSFET(TS-LDMOS) Structure for High Power Amplifier Application above2GHz," *ETRI Journal,* vol. 25, no. 3, June 2003.

[13] C. K. Maitiy, L. K. Bera and S. Chattopadhyay "Strained-Si heterostructure field effect transistors," Semicond. Sci. Technol. 13, 1225–1246, 1998.

[14] H. Nayfeh, J. L. Hoyt and D. A. Antoniadis, "A Physically Based Analytical Model for the Threshold Voltage of Strained -Si n-MOSFETs," IEEE Transactions on electron Devices, vol. 51, no. 12, Dec. 2004

[15] N. S. Waldron, A. J. Pitera, M. L. Lee, E. A. Fitzgerald, and J. A. del Alamo, "Positive temperature coefficient of impact ionization in strained-Si," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1627–1633, Jul. 2005

[16] T. Irisawa, T. Numata, N. Sugiyama, and S. Takagi, "Physical origin of increase in substrate current and impact ionization efficiency in strained Si n- and p-MOSFETs," in *Proc. ICSI-4*, May 2005, pp. 102–103.