

An Optimization Tool-Based Design Strategy Applied to Divide-by-2 Circuits with Unbalanced Loads

Agord M. Pinto Jr., Yuzo Iano, Leandro T. Manera, Raphael R. N. Souza

Abstract—This paper describes an optimization tool-based design strategy for a Current Mode Logic CML divide-by-2 circuit. Representing a building block for output frequency generation in a RFID protocol based-frequency synthesizer, the circuit was designed to minimize the power consumption for driving of multiple loads with unbalancing (at transceiver level). Implemented with XFAB XC08 180 nm technology, the circuit was optimized through MunEDA WiCkeD tool at Cadence Virtuoso Analog Design Environment ADE.

Keywords—Divide-by-2 circuit, CMOS technology, PLL phase locked-loop, optimization tool, CML current mode logic, RF transceiver.

I. INTRODUCTION

IN the last decades, radio frequency waves have attracted the interest from academia and industry due to a number of attractive features of radio frequency wave-based devices to provide gigabit level transmission rate through wireless communication systems. In this context, phase-locked loop PLL-based frequency synthesizers play a critical role [1] for stable reference frequency generation with precise channel spacing and acceptable level of phase noise.

Widely utilized in communication systems for transceiver implementation operating at radio frequency RF range, PLL-based circuits perform a precise output frequency generation by establishing a stable correlation (in phase and frequency) between output and input frequencies by phase comparison. Working through large signal operation, frequency dividers are the building blocks responsible for interfacing different frequency levels with the required precision.

In this particular application context, divide-by-2 circuits generate the set of PLL outputs for the connection and driving of the loads at transmitter and receiver level to ensure the system operation with the required reference frequency and with acceptable levels of harmonic degradation.

This paper aims to describe the structure, operating features

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and design strategy applied for the implementation of a divide-by-2 circuit, PLL building block for System on Chip SoC design in a RFID protocol based-transceiver. PLL structure is composed by a phase-frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage controlled oscillator (VCO), and a divide-by-2 circuit (DIV2) in the feed forward path, and a programmable loop divider in the feedback path, according to the block diagram on Fig. 1.

Defined for high frequency applications, the system comprises a set of technical features specified from ISO/IEC 18000-4, by applying a frequency range based on the unlicensed Industrial, Scientific and Medical ISM band (used in item management applications) centered at 2.4375 GHz. In this case, the general set of PLL operating features includes 16 communication channels, 5 MHz-based channel spacing and frequency range from 2.4 GHz to 2.475 GHz. Design process was performed at Cadence Virtuoso Analog Design Environment ADE and optimized at MunEDA WiCkeD by applying XFAB XC08 180 nm CMOS technology.

Thus, Section II presents the project description, Section III describes the design procedures for divide-by-2 circuit, Section IV presents the obtained results, and finally Section V proposes the final conclusions.

II. PROJECT DESCRIPTION

A. System Level

Designed as a RFID protocol-based RF transceiver, the system architecture is composed by 3 operating modules, as illustrated from the block diagram (with the corresponding pattern of connections), on Fig 2. According to the block diagram, divide-by-2 circuit DIV2 is highlighted in gray and the building blocks to be driven are highlighted in white.

Homodyne receiver (on the bottom of the diagram) demands two balanced pairs of differential signals for driving the pair of down-conversion mixers (in different architecture branches): one pair in phase for I branch (LO_I and LO_In), and one pair in quadrature for Q branch (LO_Q and LO_Qn). With a single-ended structure, transmitter (on the top of the diagram) demands only one connection from DIV2 (LO_I) for driving the modulator (for up-conversion operation). Third-order type II PLL-based frequency synthesizer (on the middle of the diagram) requires one pair of differential signals (LO_Q and LO_Qn) from DIV2 for driving the programmable loop divider on feedback path.

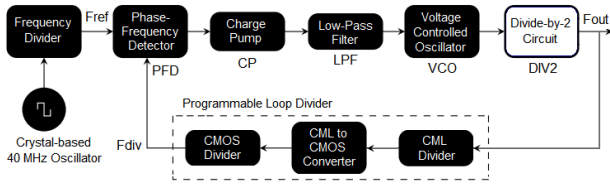


Fig. 1 PLL architecture block diagram

Hence, the resulting unbalancing in the input impedances from the loads to be driven (highlighted in white on Fig. 2) is a critical operating feature to be considered for DIV2 design.

B. Building Block Level

With flip-flop based-architecture in a feedback operation, DIV2 is composed by two latches in master/slave configuration, as illustrated on the Fig. 3. The unbalancing of the loads to be driven through DIV2 establishes a corresponding unbalancing on the loads impedance, generating a corresponding unbalancing on the output signals and, as a result, compromising the desired operation of the system: availability of balanced signals for frequency conversion through the pair of down-conversion mixers at receiver level. The applied design strategy to overcome this architecture-based limitation involves two implementation features, as illustrated on Fig. 3.

- Unbalanced latches (latches A and B) with same topology and different sizing.
- Compensation capacitance C_{comp} (at LO_In - latch B output) to balance the complementary signal connected at modulator (LO_I).

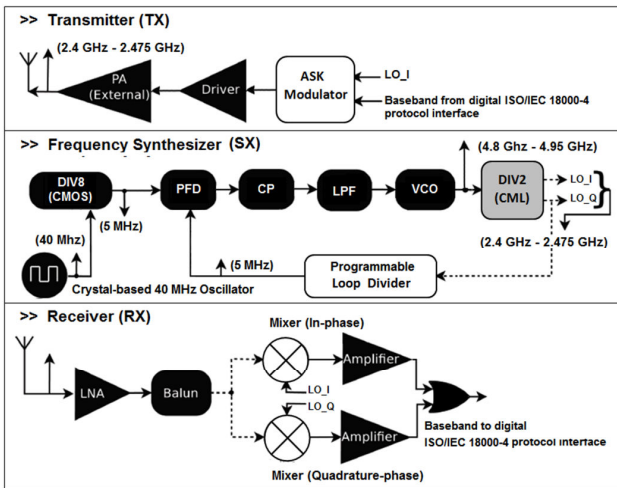


Fig. 2 RF transceiver block diagram - loads for driving

C. Topology Level

Representing a proper structure for implementing high speed logic circuits [2], a CML-based latch topology consists of three main parts, according to Fig. 4: the pull-up drain resistors R (highlighted in the upper dashed rectangle) for defining the maximum output voltage swing, the pull-down switching network (in the lower dashed rectangle) for defining

the logic operation by controlling the current flow, and the current source (in the dashed circle) whose dc current determines the resulting static power consumption by operating in saturation mode [3].

Switching network is composed by two differential pairs structured in a way to steer the current in one branch and switch off the complementary branch, according to the applied input state (differential signals from VCO). The design of high speed structures for large signal operation must consider the signal propagation delay that limits the switching speed of the gate. This delay can be improved through the proper sizing of the components: small sized components and high power consumption result in a faster switching operation.

The extremes of the output voltage levels are $V_H = V_{DD}$ at logic high and $V_L = V_{DD} - \Delta V$ at logic low, where $\Delta V = I_{SS} \cdot R$ is the output voltage swing. As a result, lower current-based CML implementations may require larger load resistors for generating a proper output swing [4]. The required dc current through a differential pair for proper operation at a given frequency range is dependent on the load capacitance and the desired output voltage swing. Generally, the output swing must be large enough to drive the set of loads, and any additional swing is a waste of power. However, considering that output waveforms are not perfectly square, additional swing is required to ensure that the fully switched condition is satisfied over a longer period of time.

The load capacitance will determine the slew rate of the block. For a capacitance C, the voltage slew rate is given by (1), where q is the charge on the capacitor:

$$SR = \frac{dV}{dt} = \frac{1}{C} \frac{dq}{dt} \tag{1}$$

Assuming that each side of the differential pairs has a load capacitance C_L , the corresponding slew rate is given by (2), where I_{CL} is the current through the capacitor:

$$SR = \frac{I_{CL}}{C_L} \tag{2}$$

The time required for the output to fully switch should be a small percentage of the period of the square wave [5].

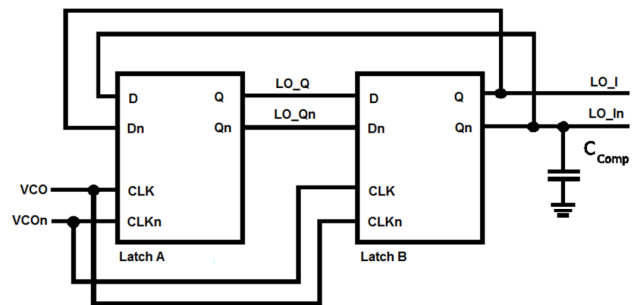


Fig. 3 Divide-by-2 circuit with unbalanced latches

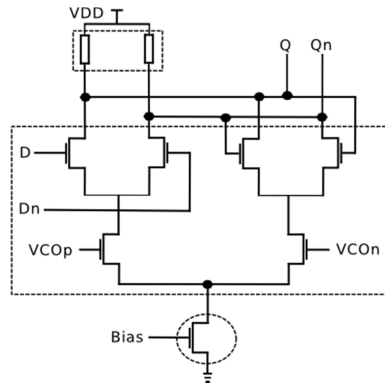


Fig. 4 CML latch topology

III. DESIGN PROCEDURES

Optimization tool-based design techniques represent an effective method for building blocks implementation at critical design restrictions: area, power consumption, and driving of multiple loads with balanced waveforms.

A. Design Flow

The adopted process for DIV2 implementation is illustrated on the Fig. 5 (stages highlighted in white were performed at Cadence simulation environment and stages highlighted in black were performed at MunEDA WiCkeD). According to the block diagram, the same design flow (represented inside each dashed rectangle) was accomplished in sequence for each latch: schematic capture and components sizing, schematic level design optimization, and physical layout level implementation. Hence, the first design flow application was implemented for latch A and, in a subsequent stage, the second application was implemented for latch B. Thus, the sequence of design tool based-procedures are described as follows.

B. Design at Virtuoso Analog Design Environment

In this context, after defining the reference block level specifications, a first stage of schematic level design is performed for frequency division implementation without loads to be driven (first block of the diagram in the dashed rectangle on Fig. 5).

In this stage, a proper configuration of analyses for performance parameters measurement is required for verification and optimization, according to the second block (in the dashed rectangle) of the diagram. The optimized operation condition of the circuit is defined according to the application features: output signal generation with precise frequency division, proper output voltage swing, balanced waveforms and lowest power consumption. As a result, the following set of performance parameters are defined for measurement at ADE environment:

- DC current consumption.
- Input frequency (differential signals).
- Output frequency (2 pairs of differential signals).
- AC output voltage amplitude.
- DC output voltage.

- Output signal propagation delay.
- Output capacitance from the loads.

Each performance parameter is evaluated through a corresponding equation for results generation at number and curves format.

C. Design at MunEDA WiCkeD

After the measurement configuration of the performance parameters at ADE environment, the next step in the design flow at schematic level is based on constraint editor configuration at WiCkeD environment. In this design stage, parameter setup section-based interface allows the specification of the range for the reference parameters:

- Design parameters: W/L and bias levels for active components, and R/L/C for passive components.
- Operating parameters: voltage and temperature.
- Performance Parameters: parameters previously defined for measurement at Cadence ADE with the corresponding analysis specification.

In this stage, a proper configuration is provided for independent sizing of the latches (through independent design variables - W_A for latch A and W_B for latch B), creating an unbalanced structure at size level to compensate the unbalancing of the loads. Additionally, complementary variables are provided to be properly sized to allow 2 independent schemes for compensation capacitance for hardware emulation, as follows:

- Emulation of the effect of input capacitance from modulator (signal LO_I) over the complementary pair (signal LO_In).
- Emulation of the physical (capacitive) effect of the tracks defined from block level and top level layout over the two pairs of output signals.

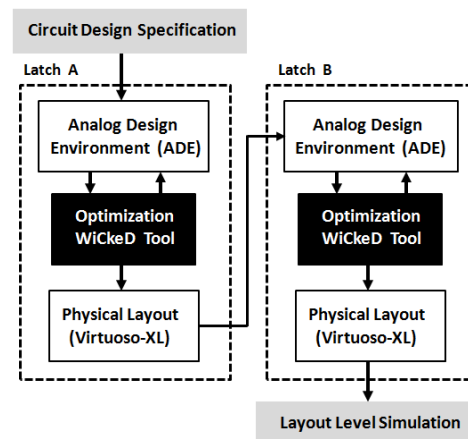


Fig. 5 Adopted design flow for divide-by-2 implementation

Thus, the applied sequence of simulations performed for verification and optimization at WiCkeD environment is illustrated from the diagram on Fig. 6. According to the diagram, verification-based simulations are highlighted in white, and the applied optimization-based simulation is highlighted in black. Responsible for circuit verification, the

applied analyses can be described as follows [6]:

- Simulation: performance parameters verification under nominal conditions.
- Sensitivity: evaluation of the percentage contribution for each design and operating parameter over the specified performance parameters.

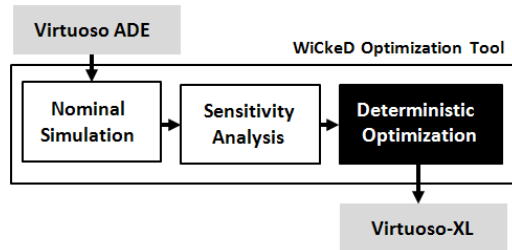


Fig. 6 MunEDA WiCkeD - applied verification and design flow

Responsible for providing optimality condition for circuit operation at schematic level (considering a previous set of specifications and design restrictions), the reference optimization (deterministic nominal optimization) can be characterized by applying three possible algorithms (independently executable) for circuit sizing through design and operating parameters control.

- SQP (sequential quadratic programming): especially suitable for nonlinear performances, it solves the optimization problem by creating quadratic sub-models of performances in every algorithm iteration.
- Least square: this algorithm changes the values of the selected design parameters as little as necessary in order to meet the reference specifications.
- Parameter distance: this algorithm tries to exceed the specifications limits in order to achieve a better convergence.

Least square and parameter distance represent linear process for the solution of the optimization problem by creating linear sub-models of the performances in every iteration. Deterministic nominal optimization is useful, above all, for circuits with a negligible sensitivity regarding the process tolerances.

IV. RESULTS

DIV2 physical implementation at simulation level was accomplished through layout, according to Fig. 7. From the illustration, it is possible to verify the applied unbalancing in sizing between the CML-based latches A (on the lower left) and B (on the lower right), the resulting difference in area, and the additional capacitive structure for compensation capacitance (on the left top). During layout design phase, strict criteria were applied to minimize parasitic effects from the tracks over the circuit operation.

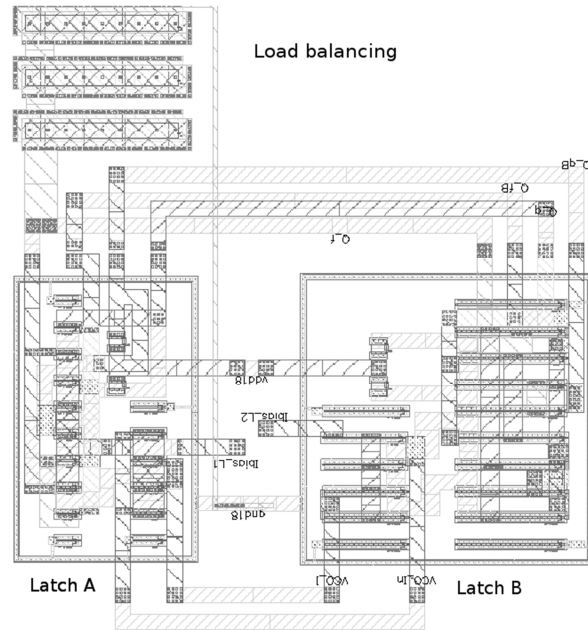


Fig. 7 Divide-by-2 circuit - layout level representation

A critical step during layout implementation involves the coupling with the loads to be driven. An additional factor is the current level of the block: to higher the current, the greater become the resulting parasitic effects. Thus, the routing was performed in a way to maximize the geometric symmetry between the tracks (considering tracks with thicker metal layers to reduce the degradation of interconnections and avoiding efficiency losses in the operation of the circuit).

From differential inputs generated through VCO, DIV2 output waveforms (with the half frequency) are plotted at simulation environment, considering 2 operating states from PLL programming: channel 1 at Fig. 8 and channel 16 (last channel) at Fig. 9. For both illustrations, the set of waveforms can be identified as follows: LO_I at lower solid line, LO_In at lower dashed line, LO_Q at upper solid line and LO_Qn at upper dashed line.

Considering voltage supply $V_{DD} = 1.8$ V, Table I compares the resulting performance parameters obtained per latch. From Table I, it is possible to verify the unbalancing involving the latches (area and static dc power consumption) resulting from the different sizing applied during design stage. Additionally, the total area estimated for DIV2 includes compensation capacitor (at LO_In) and routing lines applied for connection of the latches.

Table II summarizes the large signal-based operating features for DIV2, considering the first and the last channel for PLL frequency generation: input frequency, output frequency and output voltage swing.

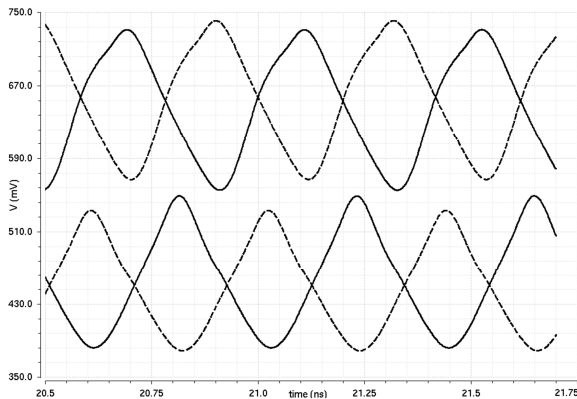


Fig. 8 Divide-by-2 circuit outputs (PLL channel 1)

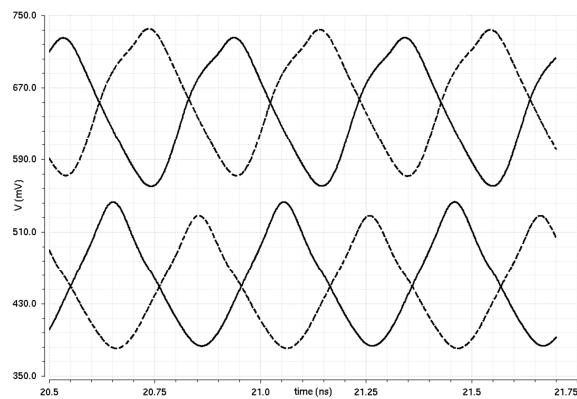


Fig. 9 Divide-by-2 circuit outputs (PLL channel 16)

TABLE I
DIV2-LATCHES COMPARISON

Circuit	Static Power Consumption	Area
Latch A	3.21 mW	0.0015 mm ²
Latch B	3.57 mW	0.0022 mm ²
DIV2	6.78 mW	0.0048 mm ²

TABLE II
DIV2-OPERATING FEATURES

PLL Channel	Input Frequency	Output Frequency	Swing LO I/In	Swing LO Q/Qn
1	4.8 GHz	2.399 GHz	319.4 mV	346.8 mV
16	4.95 GHz	2.475 GHz	306.1 mV	326.4 mV

Considering the full loads-based operation, the corresponding input frequency locking range is 500 kHz to 5 GHz (5 MHz above the maximum operating frequency required for application), demonstrating the proper and strict sizing of the structure for the required operating conditions.

V. CONCLUSION

A proper driving of multiple loads represents one of the most challenging operating features to be implemented from PLL-based frequency synthesizers. The output voltage swing derived from frequency dividers trades with the frequency range as well as the current consumption for defining the output waveforms with the required frequency. In this context,

the presence of architecture based-unbalancing in the loads introduces an additional operating restriction for obtaining a suitable driving capability. These characteristics of operation involving multiple trade-offs applied to a complex system with many design restrictions creates a suitable context for applying optimization tools.

In this context, this paper described an optimization tool-based design strategy for divide-by-2 circuit implementation. The modularity and asymmetry of its structure (based on unbalanced latches) were applied for managing a set of unbalanced loads to be driven. As an additional design strategy, after the layout of the first latch (latch A), the second latch (latch B) was optimized at schematic level in a subsequent design stage, enabling a further optimization for the robustness of the project. From this design strategy, a set of output waveforms were obtained with proper balancing, frequency and voltage swing for driving the loads at transceiver level, allowing satisfactory results in an optimized operation condition.

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