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An Improved Design of Area Efficient Two Bit Comparator

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***Abstract*—**In present era, development of digital circuits, signal processors and other integrated circuits, magnitude comparators are challenged by large area and more power consumption. Comparator is most basic circuit that performs comparison. This paper presents a technique to design a two bit comparator which consumes less area and power. DSCH and MICROWIND version 3 are used to design the schematic and design the layout of the schematic, observe the performance parameters at different nanometer technologies respectively.

***Keywords*—**Chip design, consumed power, layout area, two bit comparator.

I. Introduction

COMPARATOR is commonly known as amplitude or magnitude comparator. Magnitude comparator is a combinational logic circuit and is very useful and basic circuitry that performs comparison in digital devices such as signal processors (DSP) and microprocessors [1]. Basically, comparator is a logic circuit which is able to compare the magnitude of the input lines and provides the corresponding result at the output. The output obtained is basically the relation between the two numbers i.e. (less than, greater than, equal to) (Fig. 1).

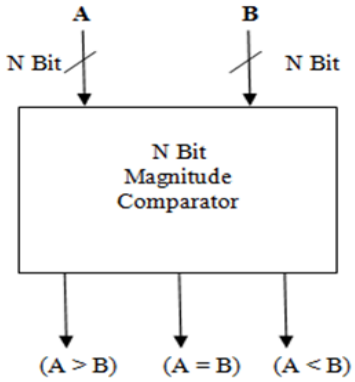

Fig. 1 Block diagram of N bit magnitude comparator

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II. Two Bit Magnitude Comparator

Two bit magnitude comparator is a combinational logic circuit. This circuit has three output lines i.e. (A less than B), (A greater than B) and (A equal to B). For this type of arrangement truth table consists of four inputs variables and sixteen entries as shown in Table I [2], [3].

TABLE I
Truth Table for Two Bit Comparator

A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table I provides the output state for every possible value of input of two bit magnitude comparator. Truth table of two bit comparator was simplified using K-map and obtained equations were used to design the circuit of two bit comparator with CMOS logic. Fig. 2 shows the circuit diagram of two bit magnitude comparator designed with the help of CMOS technology. Fig. 3 shows the waveform diagram of two bit magnitude comparator showing different states of inputs and outputs [4].

III. Proposed Approach

Using technique described in this paper, an area efficient layout of two bit magnitude comparator is designed. In the approach, we prepare two different tables for both (A<B) and (A=B).

A. Occurrence for A<B

Using the truth table of two bit comparator four situations can be derived. Using these four conditions, circuit for (A<B) can be designed:

- If A1 = 0 = A0; (A < B) = B1 + B0
- If A1 = 0 and A0 =1; (A < B) = B1
- If A1 = 1 and A0 =0; (A < B) = B1.B0
- If A1 = 1 = A0; (A < B) = 0

Conditions derived for (A<B) clearly describe that for

(A<B) we make use of one AND logic gate and one OR logic gate and hence less number of transistors will be used.

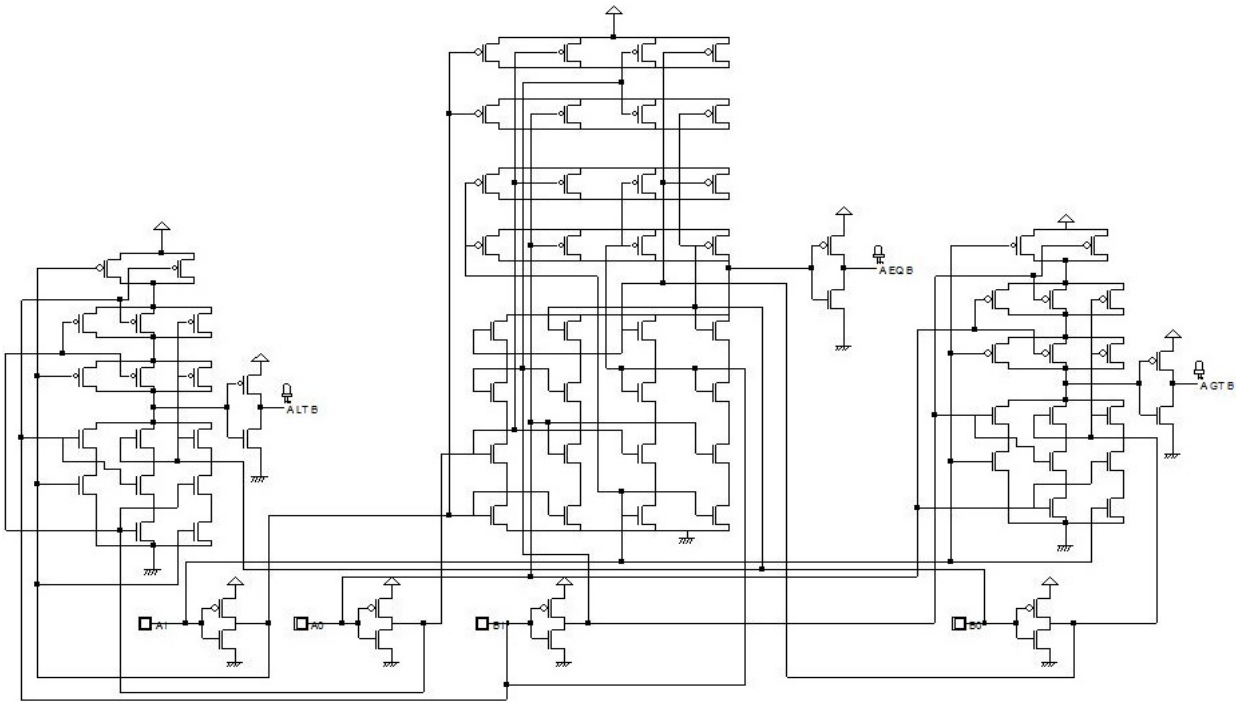

Fig. 2 Two bit magnitude comparator circuit by CMOS approach

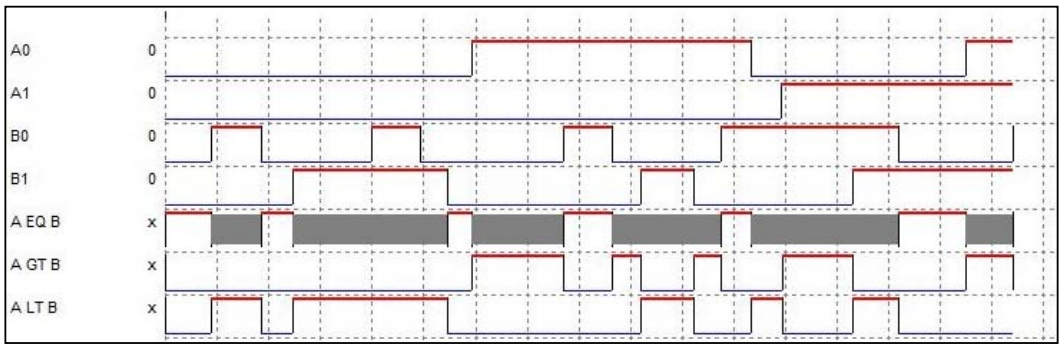

Fig. 3 Two bit magnitude comparator circuit waveform diagram

TABLE II
REARRANGED TRUTH TABLE FOR A=B

A_0	B_0	A_1	B_1	A = B
0	0	0	0	1
0	1	0	0	0
0	0	0	1	0
0	1	0	1	0
1	0	0	0	0
1	1	0	0	1
1	0	0	1	0
1	1	0	1	0
0	0	1	0	0
0	1	1	0	0
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	1	0	0
1	0	1	1	0
1	1	1	1	1

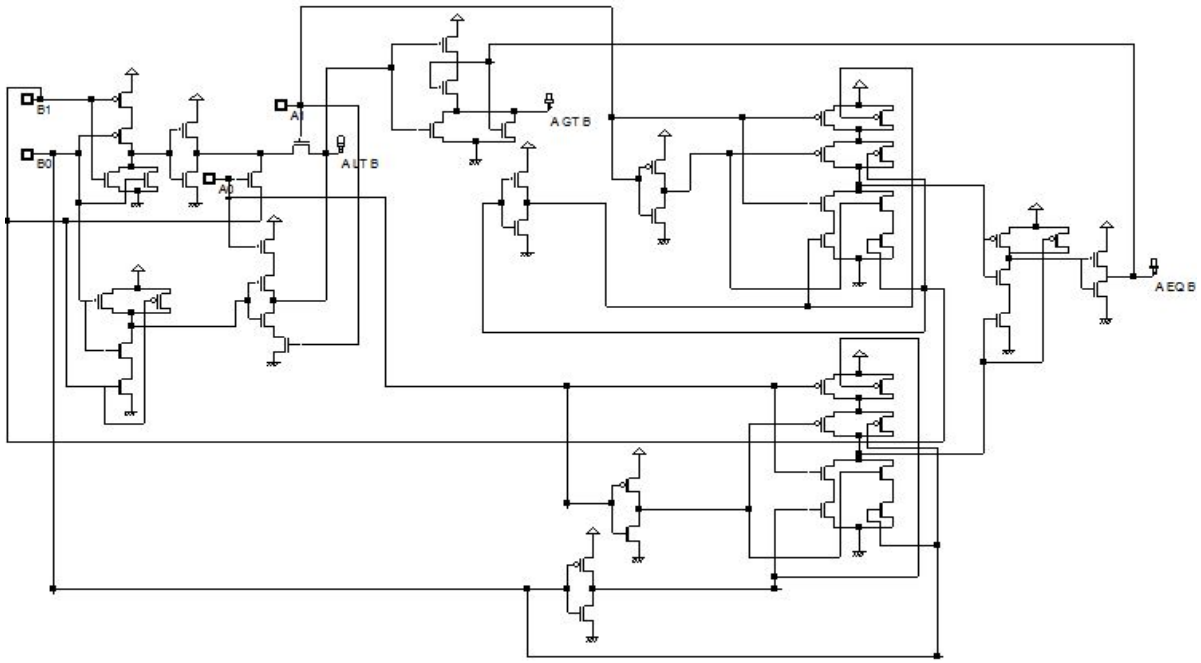

Fig. 4 Two bit comparator circuit using presented technique

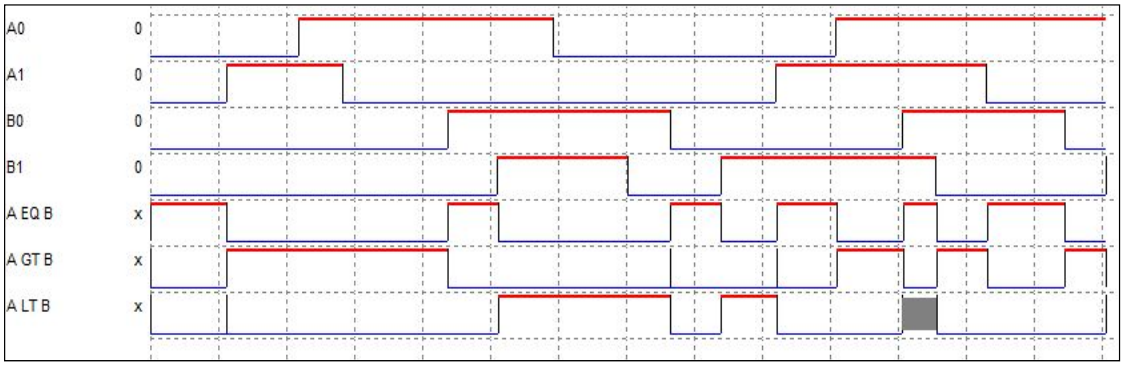

Fig. 5 Waveform diagram of two bit comparator designed using presented technique

B. Occurrence for A=B

To determine the occurrence for (A=B), we rearrange the inputs of the truth table of two bit magnitude comparator as shown in Table II. From Table II, we can easily derive the states for (A = B)

- If A0 = B0; (A = B) = A1 (EXNOR) B1
- If (A0=0 and B0=1) or (A0=1 and B0=0); (A = B) = 0

It is very clear from the occurrence that circuit for (A = B) will be made by two EXNOR logic gates and require less number of transistors.

C. Occurrence for A>B

For acquiring the result for (A>B), NOR function is utilized. NOR operation is performed on the two obtained outputs. It is evident from the conditions for (A<B), (A=B), (A>B) will use minimum transistor count hence an area efficient two bit magnitude comparator can be designed using described approach.

The circuit diagram of two bit magnitude comparator designed using presented technique is shown in Fig. 4. It is evident from the circuit diagram of two bit magnitude comparator designed by both approaches that two bit magnitude comparator designed by presented technique comprises of less number of transistors than magnitude comparator designed by using preexisting CMOS logic approach. Fig. 5 shows the waveform of two bit magnitude comparator designed using presented approach. It can be concluded from the figure that comparator designed using presented work gives same results as the previous one.

IV. Layout Designing

Designing the layout of the circuit previously developed using CMOS approach and presented technique is a significant part of the research work since all the results related to power consumed and area consumed by the circuit can only be done on the fabricated layout of the two bit comparator. After

designing the circuit or schematic on DSCH (Data Schematic version 2) it is being tested and verified according to the truth table. Further, MICROWIND version 3.1 is used to develop the layout and is being analyzed on different technologies which are 90 nm, 65 nm, 45 nm and 32 nm [5].

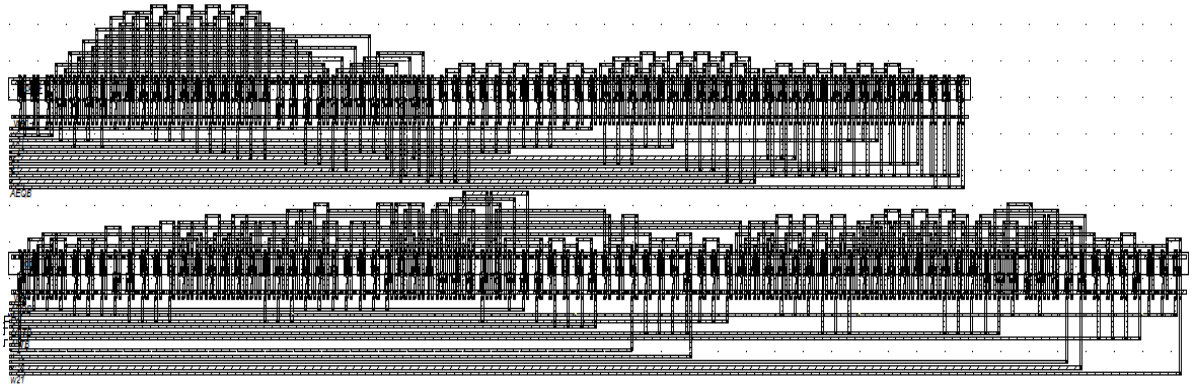

Fig. 6 Layout of two bit comparator designed using CMOS approach at 90 nm technology

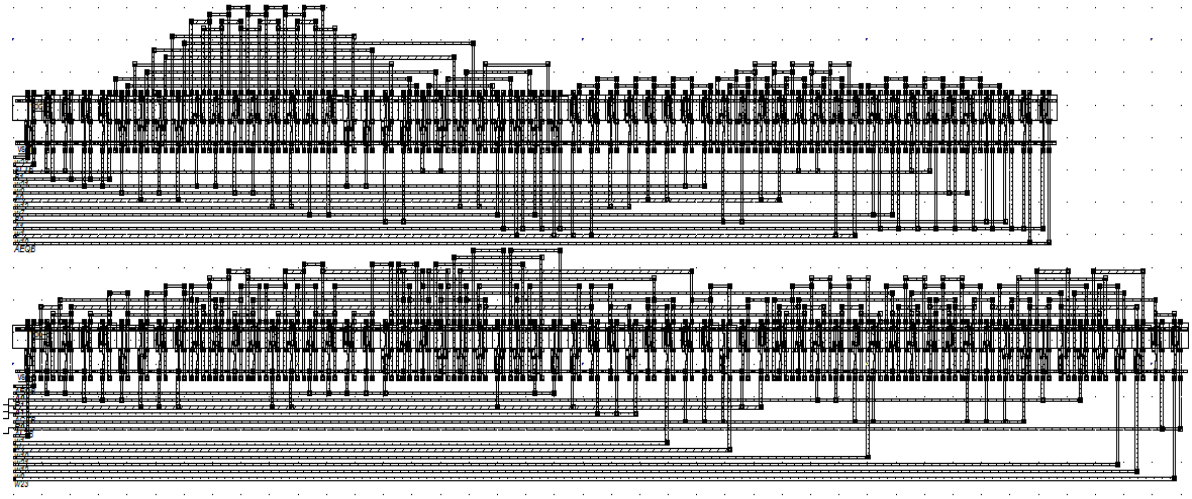

Fig. 7 Layout of two bit comparator designed using CMOS approach at 65 nm technology

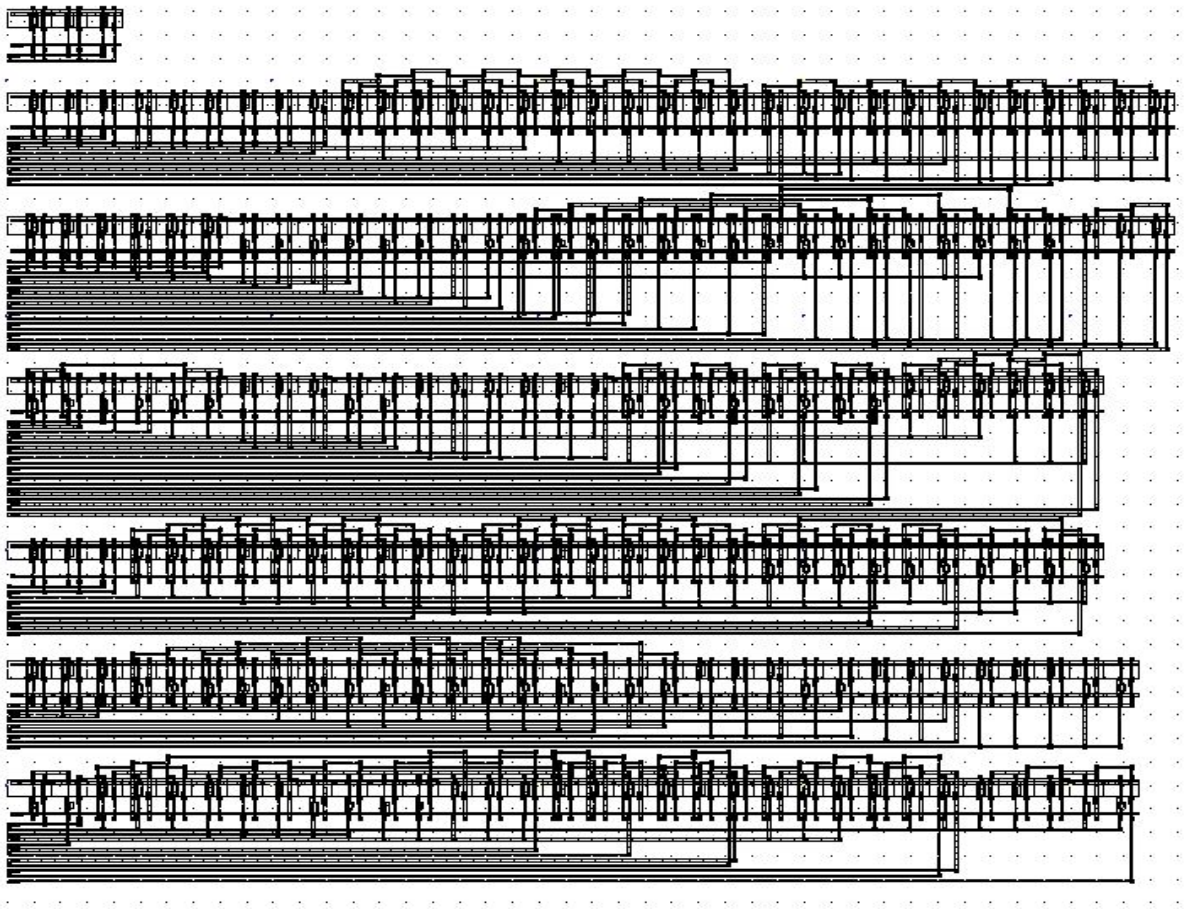

Fig. 8 Layout of two bit comparator designed using CMOS approach at 45 nm technology

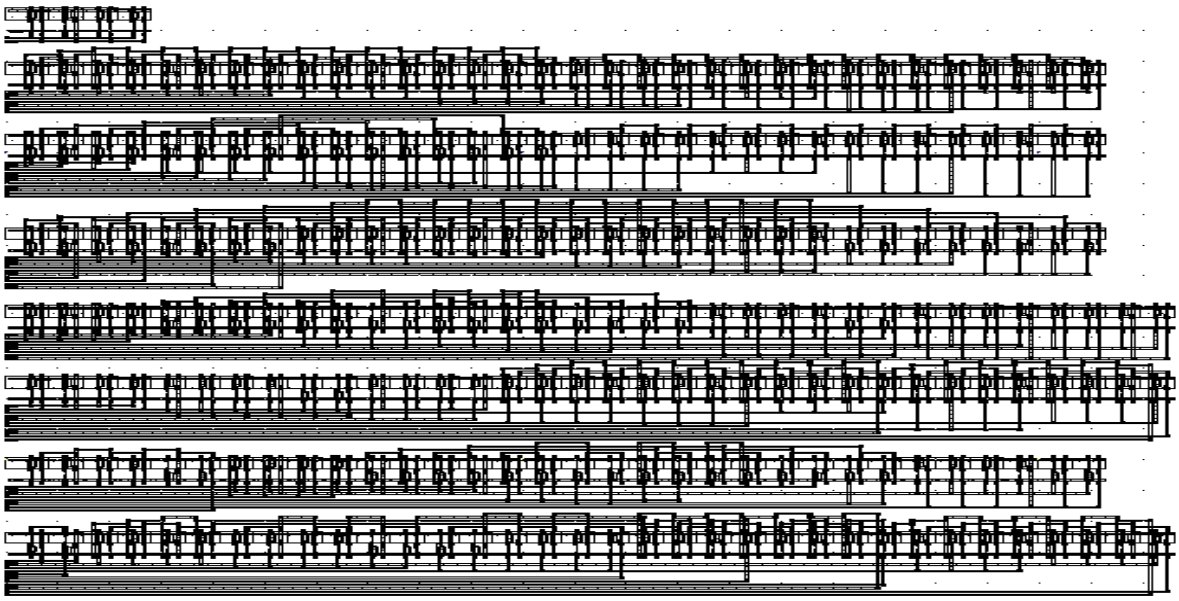

Fig. 9 Layout of two bit comparator designed using CMOS approach at 32 nm technology

Layout of two bit comparator designed using CMOS approach at 90 nm is shown in Fig. 6. Layout of two bit comparator designed using CMOS approach at 65 nm is shown in Fig. 7. Layout of two bit comparator designed using

CMOS approach at 45 nm is shown in Fig. 8. Layout of two bit comparator designed using CMOS approach at 32 nm is shown in Fig. 9. Further, these layouts were analyzed for on chip area and consumed power.

Fig. 10 shows the layout of the two bit magnitude comparator designed using presented approach as stated in this paper and fabricated at 90 nm technology. Layout of two bit comparator designed using presented approach at 65 nm is shown in Fig. 11. Layout of two bit comparator designed using presented approach at 45 nm is shown in Fig. 12. Layout of two bit comparator designed by making use of presented approach at 65 nm technology is depicted in Fig. 13. Further, these layouts were also analyzed and simulated for calculation of on chip area and power consumption so that a comparative study can be done.

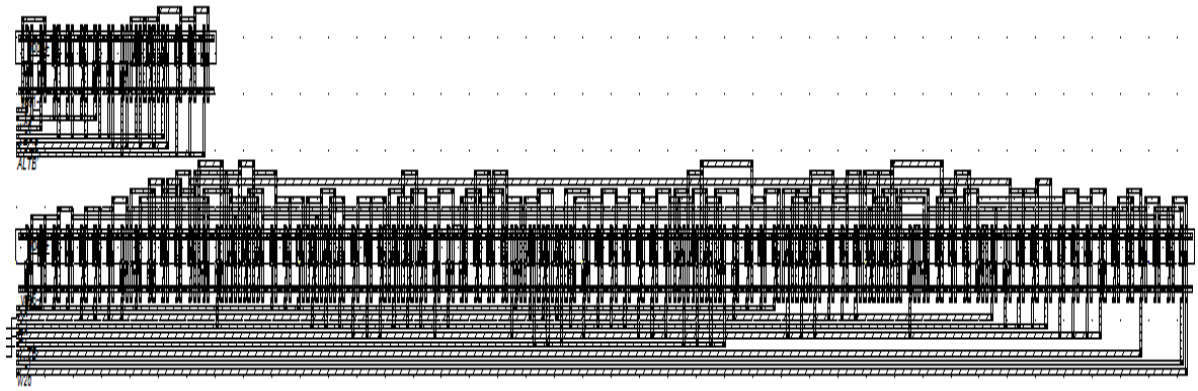

Fig. 10 Layout of two bit comparator designed by presented approach at 90 nm technology

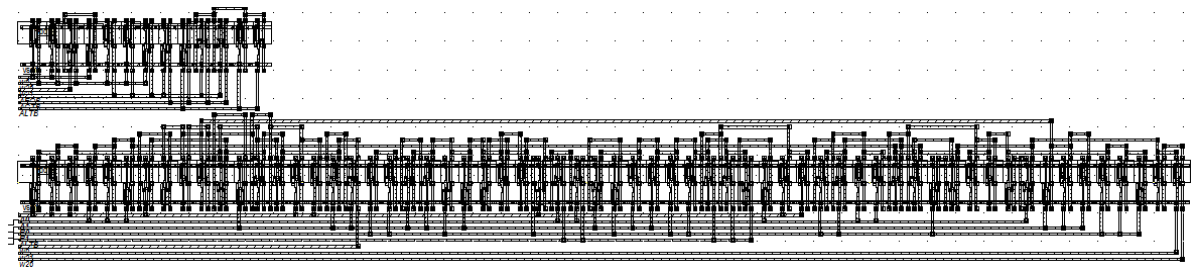

Fig. 11 Layout of two bit comparator designed by presented approach at 65 nm technology

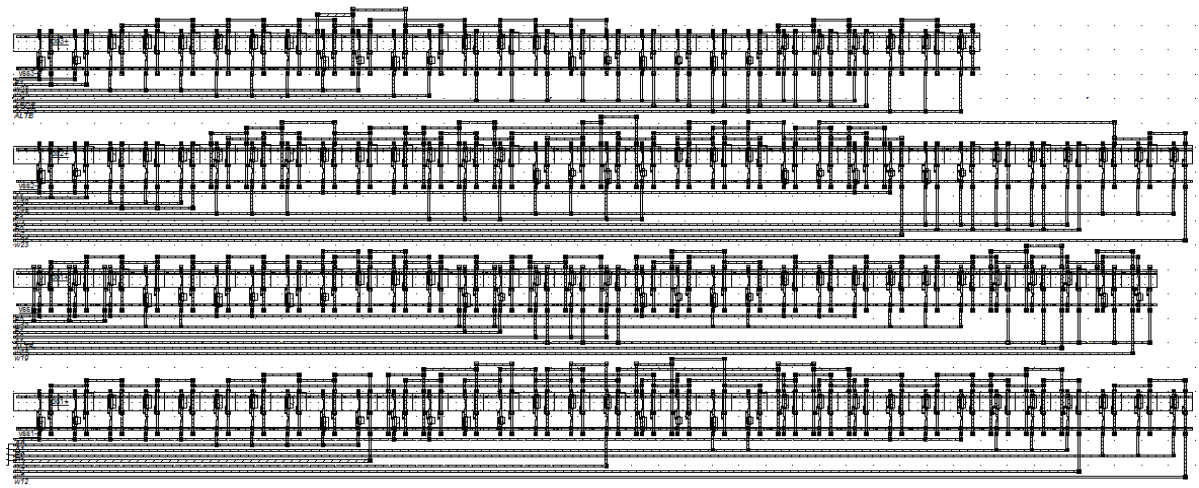

Fig. 12 Layout of two bit comparator designed by presented approach at 45 nm technology

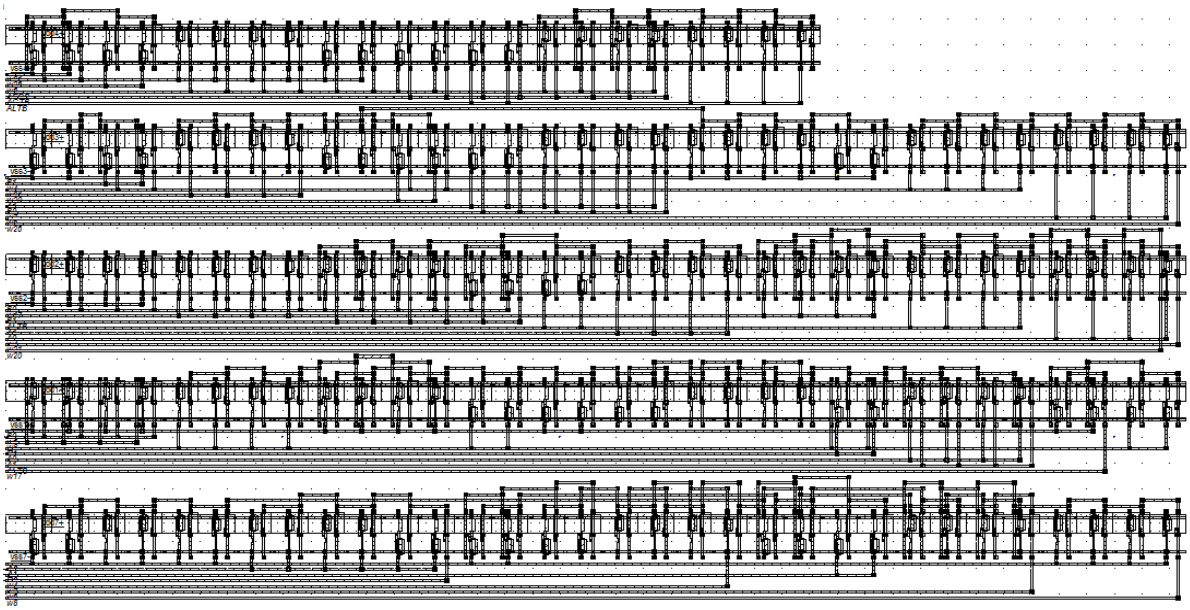

Fig. 13 Layout of two bit comparator designed by presented approach at 32 nm technology

V. Result and Discussion

Comparator designed by CMOS approach requires 78 transistors while designing of the circuit using presented approach makes use of only 50 transistors which is a remarkable reduction in transistor count. Layout structure of the circuits is designed and fabricated at various nm technologies. Analysis is done at BSim4 level and operating temperature is taken as 27 °C. Results for both the approaches were compared.

Comparative results of power consumption for both approaches are shown in Table III. Comparative results of area consumption for both approaches are shown in Table IV.

TABLE III
Power Consumed by Both Techniques

	CMOS	Presented Technique
90 nm	73.24 µW	229.0 µW
65 nm	13.72 µW	39.96 µW
45 nm	0.030 µW	0.039 µW
32 nm	0.025 µW	0.029 µW

TABLE IV
Area Consumed by Both Techniques

	CMOS	Presented Technique
90 nm	2644.1 μm^2	1686.4 μm^2
65 nm	1853.3 μm^2	1130.2 μm^2
45 nm	2561.1 μm^2	1323.1 μm^2
32 nm	1738.1 μm^2	961.9 μm^2

VI. Conclusion

Two bit magnitude comparator designed using presented approach is found to be much more efficient from comparator designed by CMOS approach. The chip area and power consumed by two bit comparator is reduced and minimized to a very large extent using different nanometer technologies. On chip area of presented circuit comes out to be 44.66% less than the circuit designed by CMOS approach. Power consumption of comparator designed by CMOS technique and presented technique is nearly same.

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