

An Energy Efficient Digital Baseband for Batteryless Remote Control

Wei-Da Toh, Yuan Gao, and Minkyu Je

Abstract—In this paper, an energy efficient digital baseband circuit for piezoelectric (PE) harvester powered batteryless remote control system is presented. Pulse mode PE harvester, which provides short duration of energy, is adopted to replace conventional chemical battery in wireless remote controller. The transmitter digital baseband repeats the control command transmission once the digital circuit is initiated by the power-on-reset. A power efficient data frame format is proposed to maximize the transmission repetition time. By using the proposed frame format and receiver clock and data recovery method, the receiver baseband is able to decode the command even when the received data has 20% error. The proposed transmitter and receiver baseband are implemented using FPGA and simulation results are presented.

Keywords—Clock and Data Recovery (CDR), Correlator, Digital Baseband, Gold Code, Power-On-Reset.

I. INTRODUCTION

ENERGY autonomous electrical device powered by ambient energy sources such as light, heat, vibration and radiation attracted significant research efforts recently [1], [2]. Among various applications, batteryless remote controller for home appliance such as TV, air-conditioner control has huge potential market. By powering the remote controller with ambient energy sources, conventional chemical battery can be totally removed from the controller so that the usage cost is reduced. More importantly, environmental pollution due to the leakage of chemicals from disposed batteries can be greatly alleviated. Compared to other energy sources, vibration energy harvested using piezoelectric (PE) harvester is well suited for this type of application. First of all, the force applied on the controller push buttons can be directly harvested to power the electrical circuit. Secondly, piezoelectric material exhibits higher energy density and output voltage swing which are desired properties for system miniaturization.

Because there is no auxiliary energy source in the system, the circuits will be fully powered off during the idle state when the stored energy is depleted. Therefore, a self startup procedure is required to reset the electrical circuits back to normal operation during the cold startup of the system. For reliable wireless transmission, the control command must be protected by forward error correction (FEC) coding to avoid wrong reception. Furthermore, conventional frame format [3], [4] contains media access control (MAC) header and frame check sequence introduce significant overhead. However, due to the

energy limitation, this application cannot afford sophisticated coding algorithm which consumes high power. In addition, longer command code requires longer transmission time, leading to higher energy consumption of the radio frequency (RF) transmitter. Therefore, a dedicated digital baseband with high energy efficiency is required for the batteryless remote controller application.

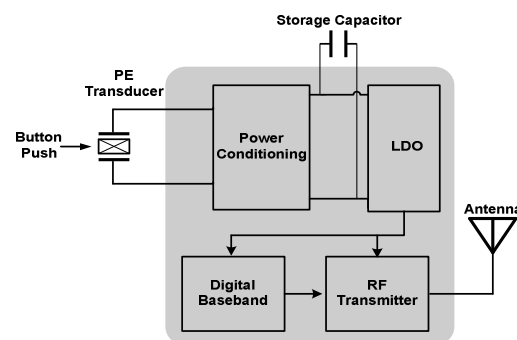


Fig. 1 Block diagram of the proposed batteryless remote controller system

In this paper, an energy efficient digital baseband circuit is designed for the PE harvester powered batteryless remote controller as well as the corresponding receiver. Power-on-reset function is designed to initiate the digital circuit during the self start-up procedure. An energy efficient baseband coding and decoding method is proposed for reliable command transmission.

II. SYSTEM DESIGN

A. System Architecture

The proposed batteryless remote controller system consists of 4 major blocks, namely the power conditioning, low-dropout regulator (LDO), digital baseband and the RF transmitter as shown in Fig. 1. A PE transducer harvests the mechanical vibration energy from the push button event and converts it to AC electrical energy. A power conditioning block provides impedance matching to the PE transducer for maximum energy extraction and converts AC energy to DC [5]. The harvested energy is stored in a capacitor to power a LDO to provide stable DC power for digital baseband and RF transmitter. A low data rate, ultra-low power radio frequency (RF) transmitter is used to match with the energy limitation [6]. To reduce the power consumption, it is advantageous to use a radio architecture that can rapidly turn on/off and transmit data in a short duration of time. In this paper, the focus will be on the baseband circuit

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design for the batteryless remote controller.

TABLE I
COMMANDS DEFINITION

Command	Symbol
1	000
2	001,010, 100
3	011,110,101
4	111

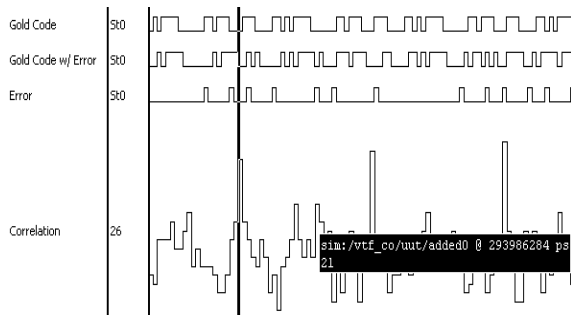


Fig. 2 Gold code correlation simulation results

B. Transmitter Digital Baseband

Since the application of the proposed system is only for control command transmission, the baseband design does not need to follow the conventional frame format [3], [4] as there are too much overhead. The proposed baseband spreads each bit of the symbol by using a 31-bit Gold code. The 31-bit Gold code is being bitwise inverted to represent data '0' or "low",

otherwise it will be data '1' or "high". Each symbol contains 3 bits, which are used to represent a command as shown in Table I. The numbers of '1' or the numbers of '0' are used to distinguish the different commands.

Gold code is used due to the fact that it exhibits good autocorrelation properties and low cross-correlation properties [7]. Gold Codes are generated by linear combination of two pseudo-noise (PN) sequences. One preferred polynomial pair used is z^5+z^2+1 and $z^5+z^4+z^3+z^2+1$. The Gold code produced by the preferred polynomial pair is shown in Fig. 2. A 10% error, which is generated by a PN sequence, is introduced into the Gold code and the result is being correlated with the template Gold code. The correlation simulation, which is shown in Fig. 2, yields a margin of 5, having a minimum correct peak value of 26 and maximum side-lobe value of 21. In other words, the correlation threshold can be 22, 23, 24, 25 and 26 to detect the presence of the Gold code.

C. Receiver Digital Baseband

With the above simplified frame format, the decoder algorithm will be a bit more sophisticated in order to correctly decode the command received. The simplified flowchart of the decoder algorithm is shown in Fig. 3. The decoder will correlate every received data. There are 2 templates for the correlation namely, the positive Gold code and 62 bits of "low". The positive Gold code template is used to detect for data '1' while the 62 bits of "low" template is used to detect the end of transmission. The decoder algorithm will first determine whether the transmission had ended.

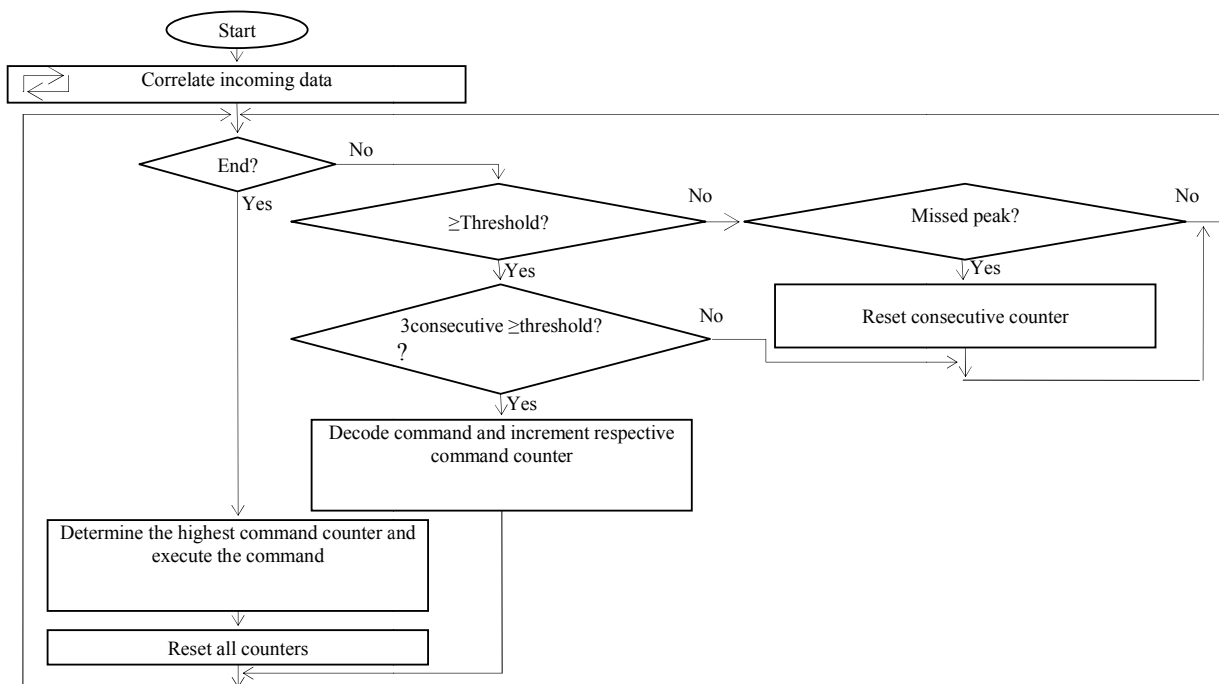


Fig. 3 Decoder flowchart

If the 62 bits of “low” correlation result is lower than the user defined threshold, the decoder will check the correlation result of the 31-bit Gold code. Whenever the 31-bit Gold code correlation result is lower than the user defined threshold, the decoder will check whether a peak should appear at that moment. The peak is defined as the 31-bit Gold code correlation result which is equal or higher than the user defined threshold. The next time slot when the peak should occur is predicted by using the current peak of the 31-bit Gold code correlation result, adding in the known period of the incoming data. If the decoder did not detect a peak during the predicted time frame, it will reset a counter, which tracks for 3 consecutive peaks, and the decode will loop back to check for end of transmission.

If the 31-bit Gold code correlation result is higher than the user defined threshold, the decoder will check the counter which is tracking for 3 consecutive peaks. If there are 3 consecutive peak detected, the decoder will increment the respective command counter which is assigned to each different commands. The command counters are indicators which will increment their value when each of their respective symbols has been successfully received.

If the 62 bits of “low” correlation result is higher than the user defined threshold, this indicates that most of the received data are “low”, thus the decoder will assume that the transmission had ended. If there is at least one completed command received, the decoder will look through the entire command counter and search for the one with the highest value. This is the way the decoder determines which command had been sent.

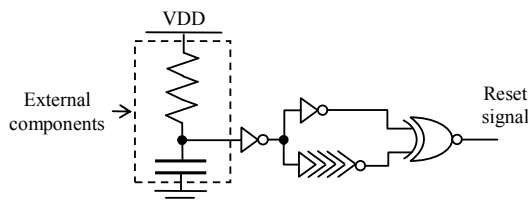


Fig. 4 Power on reset circuit

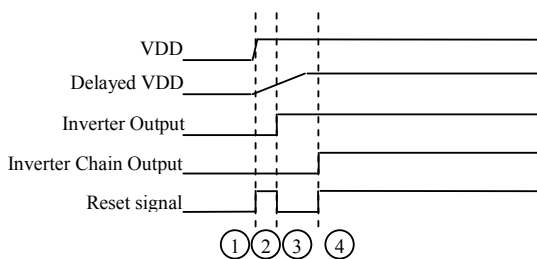


Fig. 5 Power on reset timing diagram

III. DIGITAL IMPLEMENTATION

A. Transmitter Digital Baseband

The transmitter digital baseband consists of 2 major modules, namely the power-on-reset and the 31-bits Gold code

encoder. When the transmitter is powered up, the transmitter will send the desired command. Manual reset of the digital circuit is not possible due to the very short duration of power on which is around 1 ms. The power-on-reset (POR) is used to solve the above issue which is realized through generating an active low reset pulse of 10 ns. It is implemented by delaying one of the inputs of a XNOR gate and it consists of 2 inverters, an inverter delay chain and a XNOR gate as shown in Fig. 4. An external resistor and capacitor are needed to delay the power supply, VDD. The delay of the VDD has to be sufficiently long enough whereby the whole system is being powered up before logic high can be recognized by the digital circuit. This delayed VDD is fed to both the input of the XNOR gate but one of the inputs is being delayed by the inverter chain. The timing diagram of the POR is shown in Fig. 5. Section I of the timing diagram shows that the system is not powered up. When the system is powered up, VDD rises to rail voltage and delayed VDD rises slowly. Before the delayed VDD rises to logic high, both input of the XNOR gate will be logic low and thus the power on reset signal will be logic high which is as illustrated in Section II of the timing diagram. The external capacitor will continue to charge up to logic high and to rail voltage. The input of the XNOR gate without the inverter chain will be logic high and the input of the XNOR gate drives by the inverter chain will be logic low. This results the power on reset to generate a logic low output as shown in Section III of the timing diagram. The logic high delayed VDD will propagate through the inverter chain and eventually the output of the inverter chain will be logic high. The POR will then generate a logic high output as illustrated in Section IV of the timing diagram. This completes the reset pulse generation.

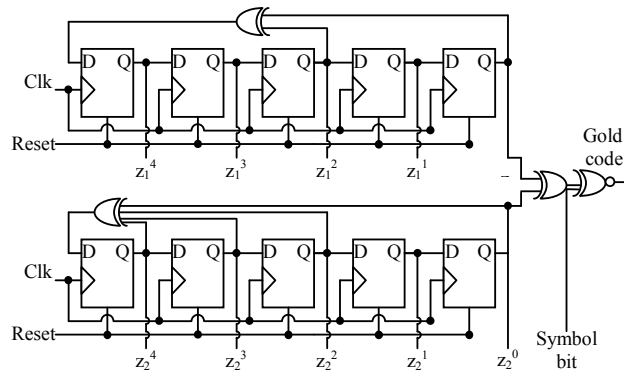


Fig. 6 Gold code encoder

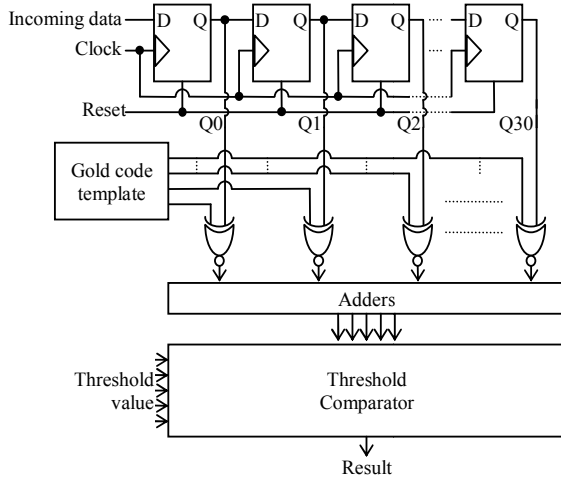


Fig. 7 Gold code correlator

The 31-bits Gold code encoder is implemented by using two linear feedback shift registers (LFSRs) as the two polynomials and the outputs are logically XOR as shown in Fig. 6. As mentioned in Section II, one of the polynomials used is $z^5 + z^2 + 1$ and the other polynomial used is $z^5 + z^4 + z^3 + z^2 + 1$. They are implemented with an initial state of [0 0 0 0 1] and [0 0 0 1 0] respectively in the shift registers. The code generated after the XOR is 31'b10001001111110000101001111100011. The Gold code is bit-wise inverted when the symbol bit is '0' and remain the same when the symbol bit is '1' which can be achieved by using a XNOR gate.

B. Receiver Digital Baseband

The receiver digital baseband consist of 2 major modules namely, the oversampling clock and data recovery (CDR) and the Gold code decoder. The oversampling CDR block uses a correlator to calculate the amount of low and high oversampled data for deciding whether the received data is a logic low or logic high in a more accurate manner when spurs appear in the data. When there is a rising or falling edge, the oversampling CDR will readjust the tracking counter by resetting it.

The gold code decoder is a correlator which is implemented using serial in parallel out shift register as shown in Fig. 7. The received bit is serially shifted in to the registers and the parallel outputs are XOR with the Gold code template in every shift.

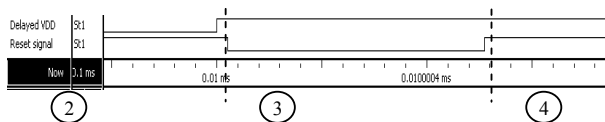


Fig. 8 Power on reset simulation

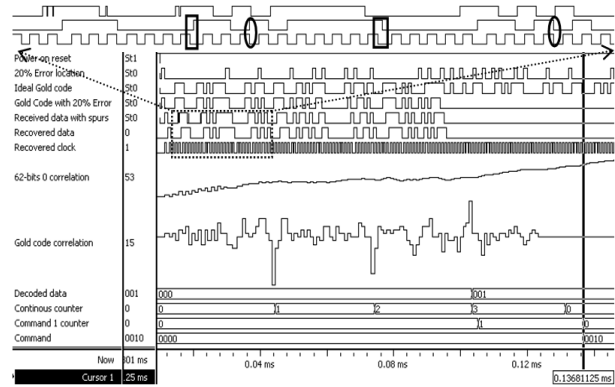


Fig. 9 System simulation 1

After which, bitwise addition is executed to obtain the correlated result between the received data and the Gold Code. The result of the summation is being compared with the user defined threshold to determine the result of the correlator is high, low or no data. The threshold value of the correlator can be changed for different channel noise condition.

IV. SIMULATION RESULTS

The transmitter and receiver digital baseband are co-simulated. The POR simulation, as shown in Fig. 8, simulated only the logic part of the circuit. Section II of Fig. 8 shows when the delayed VDD is low, the output of the power-on-reset is high. Section III shows that the delayed VDD is high and one of the input of the XNOR gate had become logic high and results in a low output. Section IV shows that the other input of the XNOR gate had become logic high as well and results in a high output. This completes the functional simulation of the POR.

To show the CDR capability, the transmitter and receiver are simulated with different data rate. The transmitter is clocked at 1.042MHz, whereas the receiver is clocked at, 16.667 MHz where the oversampling is 15 times the data rate of 1.111 MHz. In Fig. 9, the top 3 waveforms shown are the zoomed in section of the received data with spur, recovered data and recovered clock respectively. The zoomed in waveform clearly shows that there are 4 spurs in the received data and the oversampling algorithm is able to recover the data and clock. Furthermore, the data rate of the transmitter and receiver are different. The recovered clock is out of sync when there is consecutive logic high or logic low data which is outlined by rectangular boxes in the zoomed in waveform. The clock is re-sync to the data when there is no consecutive logic high or logic low data which is outlined by oval-shaped boxes in the zoomed in waveform.

The Gold code correlator, the 62-bits 0 correlator together with the decoder algorithm is simulated to recover the command1 with Gold code which has 20% error in the code as shown in Fig. 9. There is no missing peak of the Gold code correlation in Fig. 9 when the Gold code correlation threshold is set at 25. The simulation is extended to show that even when there are missing peaks, the decoder algorithm will still able to decode the command received. The extended simulation is

shown in Fig. 10 and the missing peak is outlined by dotted rectangular boxes. The continuous counter is being reset when there is a missing peak. The command counter stops to increment when there are no 3 consecutive peaks. The end of transmission 62-bits 0 correlation threshold is set at 52. The decoder algorithm has one clock cycle latency to execute the received command as shown in both Figs. 9 and 10 which is marked by the time cursor. Due to the one clock cycle latency, the 62-bits 0 correlation is 53 at the time cursor instead of 52.

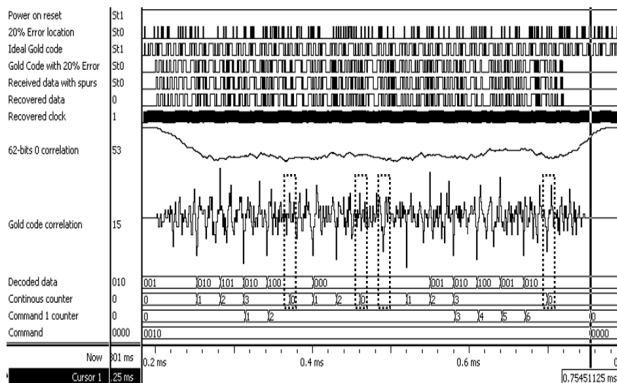


Fig. 10 System simulation 2

V.CONCLUSION

An energy efficient digital baseband circuit for PE harvester powered batteryless remote controller is presented in this paper. The simulation results shows that the digital baseband is capable of decoding the command even when there are spurs, 20% error in the Gold code and clock different between the transmitter and receiver.

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