# An Efficient Digital Baseband ASIC for Wireless Biomedical Signals Monitoring

Kah-Hyong Chang, Xin Liu, Jia Hao Cheong, Saisundar Sankaranarayanan, Dexing Pang, Hongzhao Zheng

**Abstract**—A digital baseband Application-Specific Integrated Circuit (ASIC) is developed for a microchip transponder to transmit signals and temperature levels from biomedical monitoring devices. The transmission protocol is adapted from the ISO/IEC 11784/85 standard. The module has a decimation filter that employs only a single adder-subtractor in its datapath. The filtered output is coded with cyclic redundancy check and transmitted through backscattering Load Shift Keying (LSK) modulation to a reader. Fabricated using the 0.18-μm CMOS technology, the module occupies 0.116 mm$^2$ in chip area (digital baseband: 0.060 mm$^2$, decimation filter: 0.056 mm$^2$), and consumes a total of less than 0.9 μW of power (digital baseband: 0.75 μW, decimation filter: 0.14 μW).

*Keywords*—Biomedical sensor, decimation filter, Radio Frequency Integrated Circuit (RFIC) baseband, temperature sensor.

## I. Introduction

CONTINUOUS monitoring of Biomedical (BM) signals, such as Electrocardiogram (ECG), Electroencephalogram (EEG) [1], and blood glucose levels [2], is fast becoming a ubiquitous and essential routine in daily healthcare management. To work with these non-invasive or implantable sensors, we have developed a miniaturized device that has enabled ultra-low power signal acquisition and highly-efficient wireless data transmission. Once surgically implanted into the patient, it will automatically monitor and transmit readings wirelessly to an external reader. The device includes a digital baseband module which is both area- and energy-efficient. Large logic elements are time-shared to reduce the chip area. A large counter is also shared between different phases of the operation, as wait time as long as 3 minutes is involved. The communication protocol of the implantable biomedical signals monitoring system is developed based on the ISO/IEC 11784/85 Radio Frequency Identification (RFID) standard in Full Duplex (FDX) mode [3], [4]. Adaptions are made in terms of the start-up time and the backscattering data type.

In the next section, a brief outline of the system and the building blocks of the digital circuits are described. The detailed descriptions of the digital blocks will be given in

Kah-Hyong Chang, Xin Liu, Jia-Hao Cheong, and Saisundar Sankaranarayanan, are with the Institute of Microelectronics (IME), 11 Science Park Road, Singapore 117685 (phone: 65-6770-5529; e-mail: changkh@ime.a-star.edu.sg).

Dexing Pang and Hongzhao Zheng are with Biomicro Pte. Ltd., 10 Anson Road, #14-19/20 International Plaza, Singapore 079903 (e-mail: reachpang@biomicro.com.sg).

Sections III and IV. Verification results will be presented in Section V, which is followed by a conclusion in Section VI.

## II. System Architecture

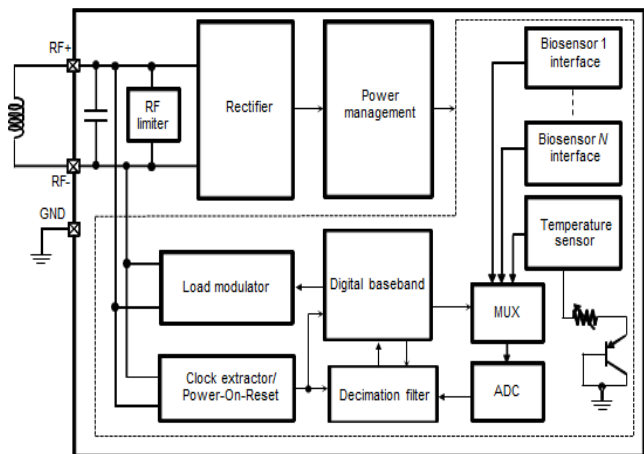The system architecture is shown in Fig. 1.



Fig. 1 Block diagram of the monitoring system

### A. System Description

The system is powered wirelessly through coupling coils by an RFID reader. The estimated power received through the coil is about 100 $\mu$W. A rectifier extracts the power from the 134.2 kHz carrier, harnessing it for the system, and for the power management block to provide a stable 1.8 V DC supply to the digital circuits. A 67.1 kHz clock is extracted by the clock extractor from the Radio Frequency (RF) carrier.

Multiple channels of sensor interface circuits are utilized to obtain the biomedical signals information from different biosensors. A temperature sensor is also deployed to obtain the temperature measurement data for interpreting some of the temperature-dependent biomedical signal levels. The outputs of these sensor interface circuits are multiplexed to a 10-bit resolution Successive Approximation (SAR) ADC.

### B. Adaptation to the ISO/IEC 11784/85 Standard

The communication protocol used in the system is adapted from the FDX mode of ISO/IEC 11784/85 standard, with modifications in the start-up time and the format of data.

#### 1. Start-Up Time

The phases involved in the operation are given in the timing diagram shown in Fig. 2, in which it can be seen that four main states exist: WAIT, CALIBRATE, NORMAL, and TRANSMIT. The start-up time, upon system reset, has been

extended to 3 minutes prior to wireless data transmission, to allow sufficient time for the temperature and BM sensors to stabilize before the measurements are taken.
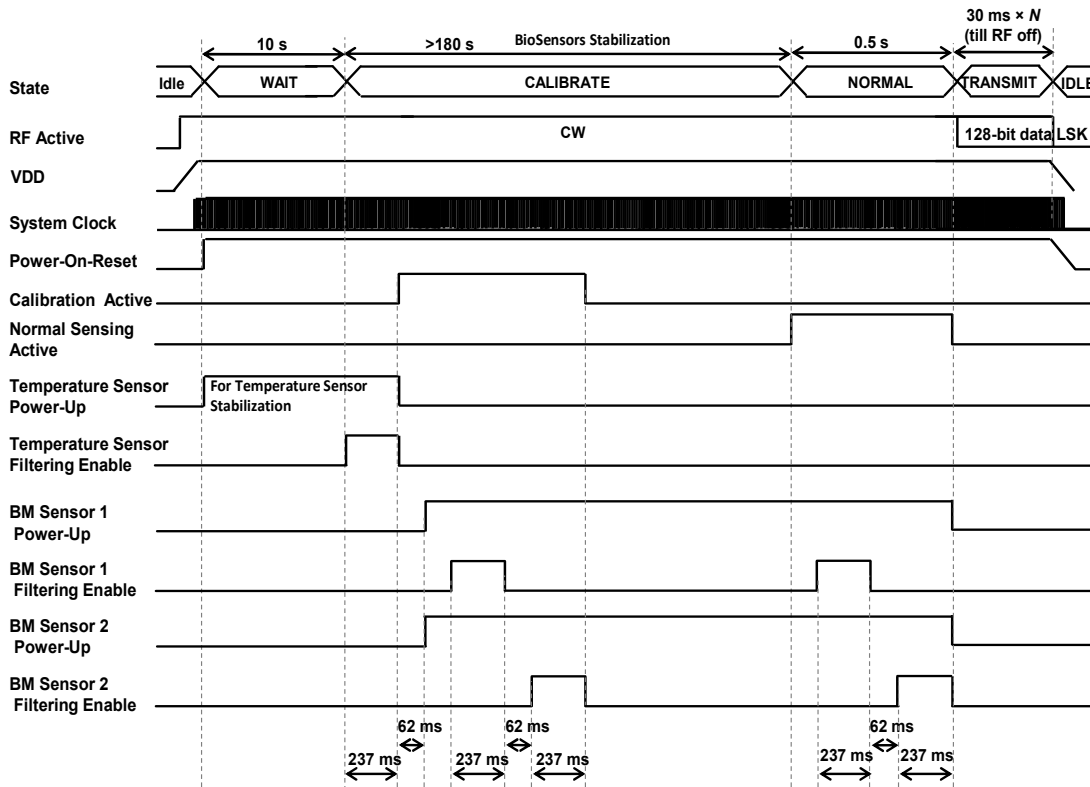


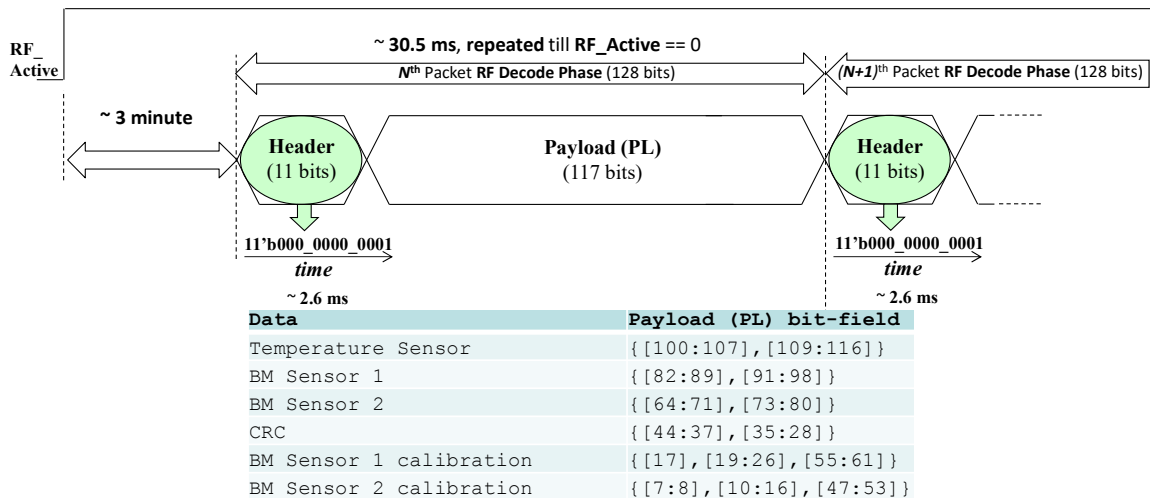Fig. 2 System-level timing diagram



Fig. 3 Contents of the payload data

## 2. Data Format

The format of the backscattered data has been adapted too. The original data fields, such as the country code and the trailer, have been replaced with the measurement data. The contents of the payload data adapted from the standard are as shown in Fig. 3.

These data are packetized and transmitted by the load modulator to an external interrogator or reader during the TRANSMIT state.

### C. System Description

The system-level block diagram of the overall digital circuits is depicted in Fig. 4.
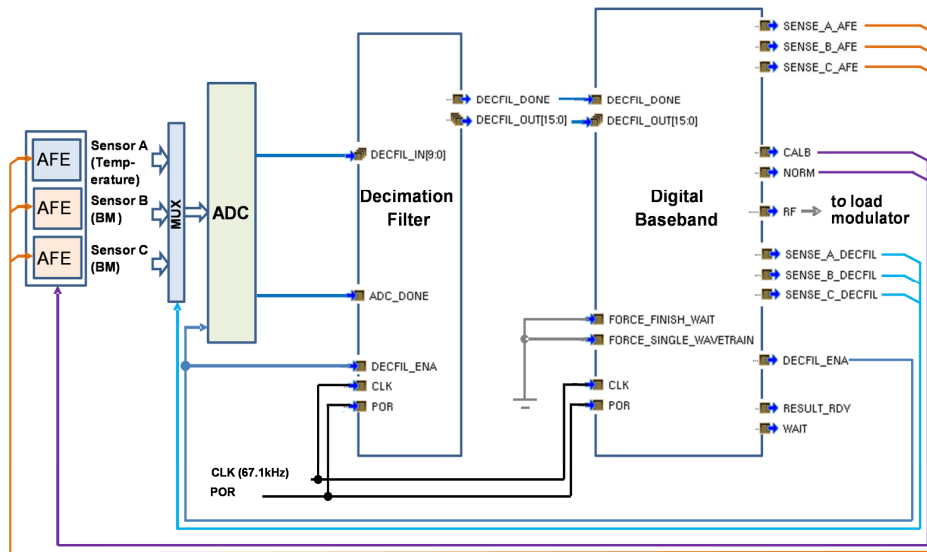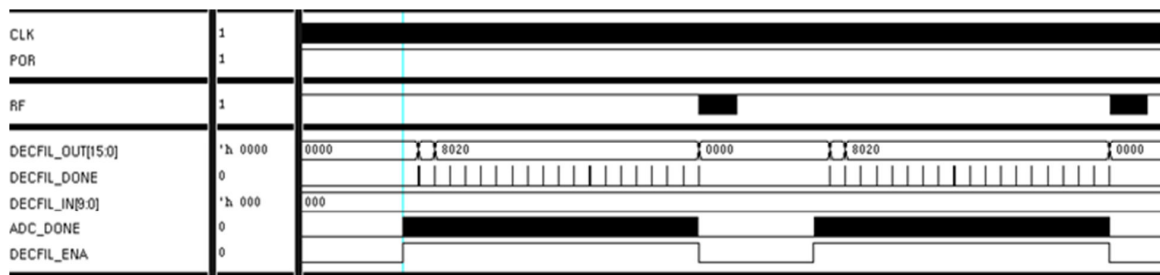
Fig. 4 Block diagram of the digital circuits



Fig. 5 Handshaking signals between the ADC, the decimation filter, the digital baseband core, and the load modulator
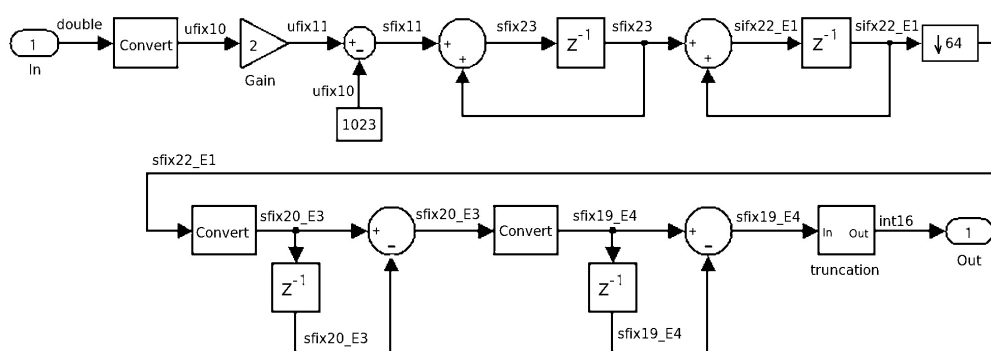


Fig. 6 Conventional structure of the CIC decimation filter

### D. Digital Circuits

The system-level block diagram of the overall digital circuits is depicted in Fig. 4. The main cores of the digital circuits are the decimation filter and the digital baseband.

#### 1. Decimation Filter

The decimation filter receives the raw measurement data from the temperature and BM sensors via the SAR ADC. Oversampling technique is used with the SAR ADC to achieve an Equivalent Number of Bits (ENOB) of 12-bit. The output from the decimation filter is then channelled to the digital baseband core to generate the packetized data for transmission. The handshaking signals between the two cores are DECFIL_ENA and DECFIL_DONE, as shown in Fig. 4, which the decimation filter receives from, and transmits to, the digital baseband core respectively. A typical behavior of their waveforms can be seen in Fig. 5.

2. Digital Baseband Core

The digital baseband core acts as the main controller module for the system. It also contains a packer which frames the payload data into a series of packets, and transmits the packets to a load modulator, which is shown in Fig. 1. The load modulator is utilized to backscatter the data to the external reader.

### III. DECIMATION FILTER

Decimation is the process of reducing the sampling rate of a signal [5], [6]. It utilizes filtering to mitigate aliasing distortion which may exist when simply down-sampling a signal [6].

Prior to its implementation, the decimation function is first modeled in MATLAB. The model used is shown in Fig. 6. It is a two-section Cascaded Integrator Comb (CIC) filter, which is an optimized class of Finite Impulse Response (FIR) filter combined with an interpolator or decimator [7], [8]. The filter is a moving average filter which takes in 10-bit inputs and generates 16-bit two's complement outputs, at a rate of 80 samples per second. It decimates the outputs by 64.

After taking into consideration the available clock rate and the throughput requirement of the decimation filter, in order to achieve area efficiency, we use only one adder-subtractor as shown in Fig. 7, instead of five as shown in Fig. 6. Selectors are used to select from a plurality of inputs to this one adder-subtractor, based on the state the filter is operating in.

### IV. DIGITAL BASEBAND CORE

The detailed architecture of the digital baseband core is as depicted in Fig. 8. It contains only one main adder in this datapath, which is parameterized to 20-bits wide. In this module there exists a set of registers which stores the filtered and averaged measurement data from the sensors. These stored data are the already processed data from the sampled outputs of the preceding decimation filter. The process is given as follows. The data received from the decimation filter are grouped into sets of 64 data each. After discarding the first 3 sets at the start of the sampling activity, the adder shown in Fig. 8 is used to average out the subsequent 16 sets of input data pertaining to a sensor. This process is repeated for all the sensors. On another note, there are a couple of submodules in the digital baseband module. One of the two submodules is the Cyclic Redundancy Check (CRC) generator. The other is the response generator, which contains a packer that packetizes the payload data according to the ISO/IEC 11784/85 standard for backscattering out of the chip.
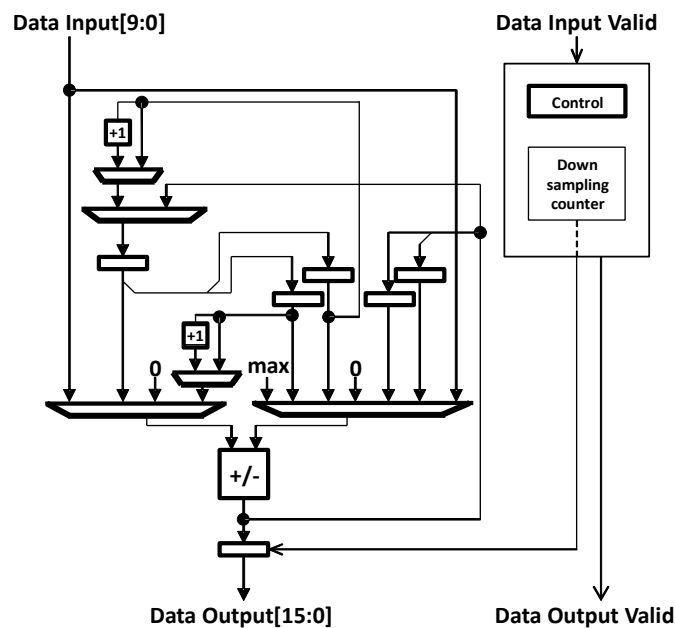


Fig. 7 An optimized structure of the CIC decimation filter

**CRC Generator:** The CRC generator is implemented based on the CRC technique, whereby an error-detecting code is inserted within the payload, as shown in Fig. 3, to detect, at the reader side, if any corruption has occurred in the received data during the wireless transmission process. The type of CRC method we use is the CCITT-16 method proposed by the ISO/IEC 11784/85 standard [3], [4]. Its polynomial representation is given by:

$$x^{16} + x^{12} + x^5 + 1 \qquad (1)$$

The implementation of the CRC generator is a simple and straightforward structure as shown in Fig. 9.

#### A. Response Generator

The response generator generates a series of packets formatted based on the description found in Fig. 3. It has only one main counter, which is 20 bits wide. The counter is reused

in different phases of the operation, as determined by a Finite-State Machine (FSM).



Fig. 8 Digital baseband core



Fig. 9 CRC generator



Fig. 10 Finite-state machine

## B. Finite-State Machine

To coordinate the digital circuits of the decimation filter and the digital baseband cores shown in Figs. 7 and 8 respectively, an FSM was implemented. Its outline is shown in Fig. 10. The shaded states chained by the solid path, when executed, generate the signals required to control the Analog Front-End (AFE) circuits in a predefined sequence.

The shaded states chained by the dotted paths are related to the backscattering process, wherein the relevant modulating signal is sent to the RF modulator according to the protocol as stipulated in the ISO/IEC 11784/85 standard. The rest of the paths are related to the test modes, included for testing the sensors, one sensor at a time.

After the RF power is cut-off, the baseband module will start from the IDLE state when the RF is resumed.

## V. SIMULATIONS AND SYSTEM VERIFICATION

For simulating the digital cores, we use Cadence *NC Verilog* and *NC Sim*. For synthesis, place and route, and sign-off checks, we use Cadence *Encounter*, *Virtuoso*, *Calibre DRC*, and *Assura LVS*. As for power analyses, we use Synopsys *PrimeTime*.

After the decimation filter and the digital baseband cores have been simulated separately, they are integrated. Further simulations are performed. After the synthesis and place-and-route procedures, their power consumptions are analyzed. Further integration work is then carried out with the rest of the system. This yields a full system as outlined in Fig. 1. The design is then fabricated, the prototype of which is later verified.

## A. Timing Simulations

Timing simulations are performed using Cadence *NC Verilog* and *NC Sim*. With Standard Delay Format (SDF) timing data back-annotation applied to the netlist, both hold and setup times are checked. No timing violation is found. The simulation waveforms and the testbench functions generated results are then captured, analyzed, and compared with the expected behavior and data.
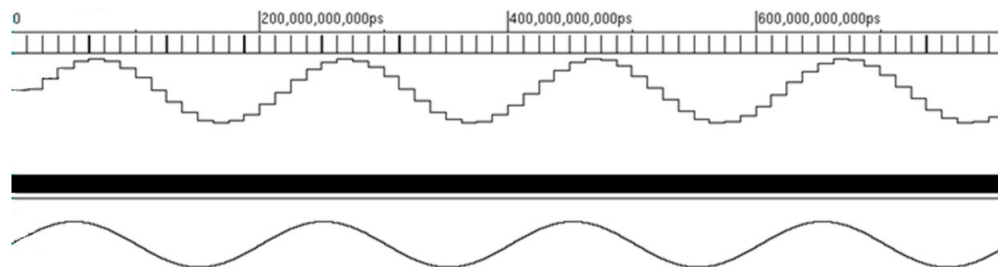


Fig. 11 Decimation filter's output (top sinusoidal stepped waveform) *vs.* input (bottom sinusoidal waveform)

### 1. Decimation Filter

The simulation results generated while simulating the decimation filter show an exact, bit-accurate match with the MATLAB generated results.

A series of input data are used. One typical type of input data has a waveform as shown in Fig. 11. The sinusoidal series have frequencies of 1 Hz, 5 Hz, 10 Hz, and 20 Hz. Other constant values are also used in the simulations. They include all maximum, and all minimum 11-bit artificial data that are not found in real-life BM signals measurement.

### 2. Digital Baseband Core

Similar timing simulation procedure described above is also applied to simulating the digital baseband core. Its stand-alone testbench has a decimation filter instantiated, which outputs serve as the inputs to the digital baseband core.

In addition to the packet data and CRC checks, which are performed by the self-checking modules instantiated in the testbench, the waveforms dumped are also visually compared with the adapted ISO/IEC 11784/85 standard specifications and the requirements specified by the AFEs and the SAR ADC. The captured waveforms are also used in power analyses, which are performed to estimate the power consumptions of the digital baseband as well as the decimation filter cores.

## B. Power Analyses

After the synthesis and place-and-route procedures are performed, the post-route netlist generated is used in Synopsys *PrimeTime* environment for power analyses. The typical waveforms generated from the timing simulations are also used as an input to the power analysis tool. Time-base technique is used, the results of which are summarized in Tables I and II.

Table I tabulates the results of the power analysis performed on the two main digital modules, when the size of the output buffers used in the digital baseband core is ×20.

Reduction in power consumption can be made in the future by utilizing output buffers of smaller sizes, specified according to the requirements of the interfacing AFEs. The reduction in power consumption that can be achieved is approximately 6%, as shown in Table II.

## C. Implementation

The system as depicted in Fig. 1 is fabricated using the 0.18-μm CMOS technology. The full-chip micrograph of the microchip, with the decimation filter and digital baseband cores depicted as layout figures as captured from the Cadence *Encounter* tool, is shown in Fig. 12.

TABLE I
POWER ANALYSIS RESULTS OF THE DIGITAL MODULES

|  | Type | Power (μW) |
|---|---|---|
| Decimation Filter | Internal | 0.1150 |
|  | Switch | 0.0122 |
|  | Leak | 0.0137 |
|  | *Sub-total* | *0.1409* |
| Digital Baseband | Internal | 0.6270 |
|  | Switch | 0.0892 |
|  | Leak | 0.0319 |
|  | *Sub-total* | *0.7481* |
|  | *Total* | *0.8890* |

TABLE II
POWER CONSUMPTION OPTIMIZATION

| Type | Power (μW) | | % savings in power consumption |
|---|---|---|---|
|  | Maximum output buffers size (×20) | Tailor-made output buffers size |  |
| Internal | 0.6270 | 0.5970 | 4.8 |
| Switch | 0.0892 | 0.0812 | 9.0 |
| Leak | 0.0319 | 0.0274 | 14.1 |
| *Total* | 0.7481 | 0.7056 | *5.7* |

The decimation filter core occupies 140 μm × 400 μm of chip area, whereas the digital baseband module takes up 300 μm × 200 μm.

Two set-ups are used for verifying the system. The first set-up, as depicted in Fig. 13, is meant primarily for testing the baseband functions. The second set-up, as shown in Fig. 15, is for testing the RF transmission capability of the system.

*D. Verification*

Two set-ups used in verifying the fabricated microchip are presented here.

1. Set-Up One

In the first test set-up, 16-bit constant values (minimum, typical, and maximum) are used as inputs to the digital baseband, by switching the module to the test modes. The intermediate output of the microchip transponder, after the digital baseband, before the load modulator, is channeled to a logic analyzer. Out of the many waveforms captured and analyzed (and all have been verified correct), a typical waveform is illustrated in Fig. 14. By analyzing the waveform, we can see that the header and the initial portion of the received data, which are deciphered as a series of binary values given by 00000000001_10000111_1_00011101, are correct.
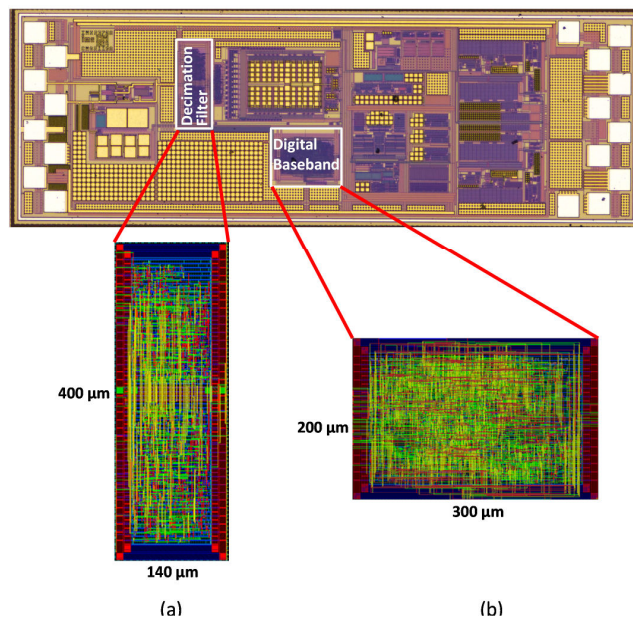


Fig. 12 Micrograph of the full chip and the layouts of the (a) decimation filter, and (b) digital baseband

2. Set-Up Two

A second test set-up is aimed at testing the RF link between the on-chip modulator and the interrogator (external RFIC reader), a representation of which is shown in Fig. 15.

In this set-up, instead of bypassing the rest of the circuits other than the digital circuits, an adapted RFID reader is used to power the system wirelessly.

One challenge is encountered during the bring-up phase of this set-up. Incorrect readings are decoded by the interrogator.

After analyzing the waveforms captured from the logic analyzer, as shown in Fig. 16, it is found that the harmonic wave of frequency $2f$, where $f$ is equal to 134.2 kHz, has been incorrectly interpreted as the fundamental wave in the transponder microchip. This problem is solved by keeping the interrogator at a farther distance (max. 10 cm) away from the transponder.

Fig. 13 Set-up one
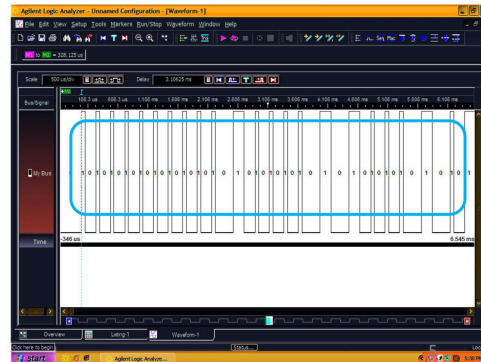


*(flipped up-side-down for convenience in analyses)*

Fig. 14 Logic analyzer's waveform display
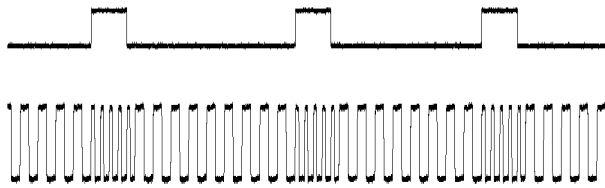


Fig. 15 Set-up two

Fig. 16 Behavior of the extracted clock (lower waveform) *vs.* the modulating signal (upper waveform)

## VI. CONCLUSION

We have implemented a digital baseband ASIC that has achieved both area- and energy-efficiency for controlling the AFEs which measure the temperature and biomedical signals, and for transmitting the measured and processed data through backscattering LSK modulation to an external adapted reader. Its low power consumption provides an environment with temperature stability for the on-chip temperature-sensitive biomedical devices to operate in. Its reduced size contributes to a smaller form-factor microchip that can be implanted under the skin without causing discomfort to the patients.

## ACKNOWLEDGMENT

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