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Algorithm Design and Performance Evaluation of Equivalent CMOS Model

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***Abstract*—**This work is a proposed model of CMOS for which the algorithm has been created and then the performance evaluation of this proposition has been done. In this context, another commonly used model called ZSTT (Zero Switching Time Transient) model is chosen to compare all the vital features and the results for the Proposed Equivalent CMOS are promising. In the end, the excerpts of the created algorithm are also included

***Keywords*—**Dual Capacitor Model, ZSTT, CMOS, SPICE Macro-Model.

I. Introduction

THE dual Capacitor Model is based on the Hysteresis loop characteristic of the ferroelectric capacitor.[1] This model approximates the two branches of the hysteresis loop by two straight lines as shown in Fig. 1.

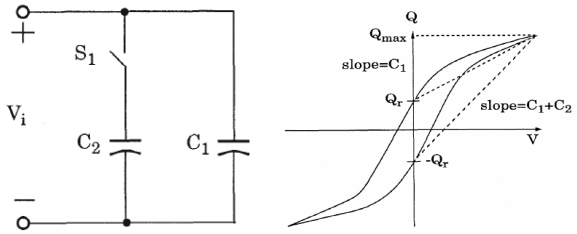

Fig. 1 Hysteresis loop characteristic of the ferroelectric capacitor

The proposed Model works on the principle of Charged being stored in the capacitor. The dual Capacitor Model is based upon the switching of the Switch S1 whereas the Proposed CMOS Model depends upon the Sweep Voltages which triggered the two pass- transistors NMOS and PMOS, which acts as switches given in Fig. 2.

In Dual capacitor Model [2] the charged stored in the Capacitors C1 and C2 which defines the Slope lines when switch S1 is open and C1 + C2 represent the higher slope when Switch S1 is closed in Fig. 1.

In Proposed CMOS model the two different Voltages V1 and V2 charges the capacitor at two different values. Let the V1 voltage is 5 volts, then the charged stored in the capacitor is Q= CV

Similarly, V2 voltage through PMOS is 2 Volts, the charged store in the capacitor is Q=CV.

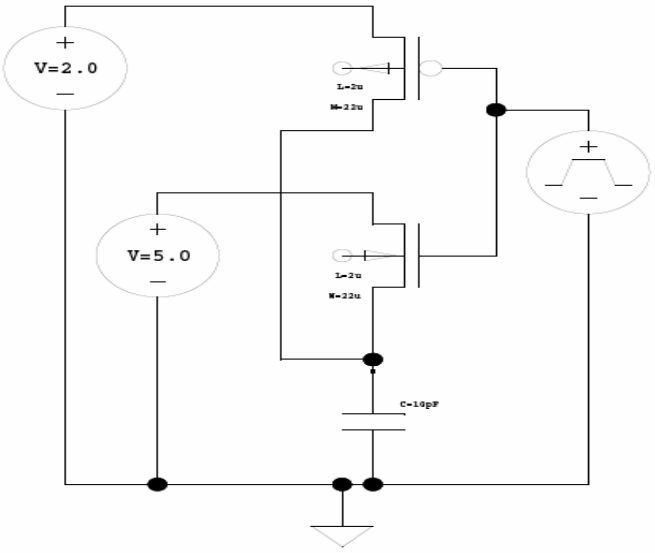

Fig. 2 Dual Capacitor Model

In dual capacitor Model, the two different charge are defines by the C1 and C2 capacitors, the slope defines the logic being stored in Ferroelectric RAM. Let the same capacitor values has been taken , the charged Qr in hystersis loop being stored is Qr=C1V and charged - Qr hystersis loop being stored is [-Qr] = (C1+C2)V.

Hence, the Proposed CMOS Model is more easier, accurate as compared with the Dual Capacitor .The proposed Model is CMOS based Model and is flexible of changing of two different voltages V1 and V2 accordingly to the change required in designing the equivalent Model of ferroelectric Capacitor. The waveform of Proposed CMOS Model is given at the Appendix D , showing the two different Voltages are being Stored in the capacitor with the Triggering of Pass-transistor with the Sweep Voltage.

The equivalent CMOS Model which is being designed using the Proposed Behavioral CMOS model is stores the two different charges in the capacitor as it is given in the hysterisis loop. The advantage of this Equivalent CMOS model is that

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the model is MOS based Model and accordingly to the application the two different charged is being stored in the capacitor.

The proposed CMOS model is Spice MacroModel (Appendix A) and only working for large scale Model of the Transistor. Hence for small size and low Power, the new Ideas and Directions should be introduced to the present CMOS model for further and future use for Spice Modeling of Ferroelectric RAM [5].

II. Zero Switching – Time Transient Model

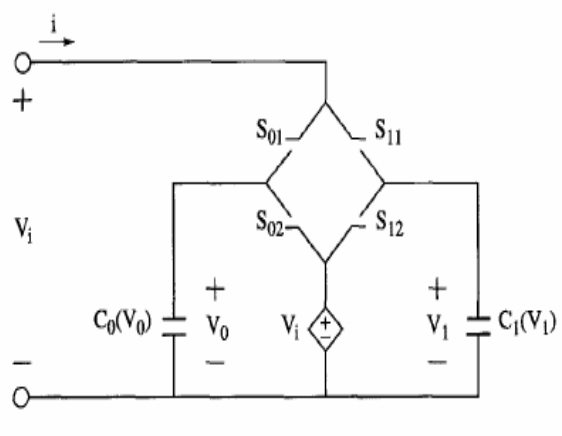

Fig. 3 Zero Model

The ZSTT model assumes the switching time of a ferroelectric capacitor to be(as from figure 3) zero. This assumption will introduce little inaccuracy if the RC time constant of the circuit under study is much larger than the switching time of the FE capacitor. It is shown that for a typical memory circuit including FE capacitors such an assumption is quite valid. Zero switching-time implies that a charge increment on the FE capacitor will take place instantaneously. Therefore, a charge increment is only a function of the applied voltage and the initial state of the capacitor, not a function of time.

$$\Delta Q = \Delta Q(V, Q_{init}) \tag{1}$$

where V and & Qinit represent the applied voltage and the initial polarization charge on the capacitor. Since there are only two initial states that are important to a memory cell (i.e digital 0 and l), the above equation (also shown in figure 4)can be broken into two parts, each corresponding to one initial state.

$$\Delta Q = \begin{cases} \Delta Q_0(V) & \text{for digital 0 state} \\ & \text{or} \\ \Delta Q_1(V) & \text{for digital 1 state} \end{cases}$$

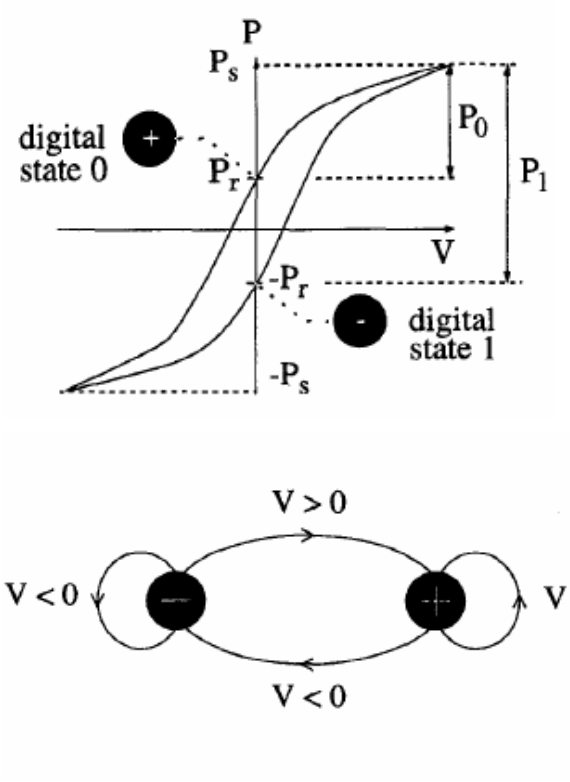

Fig. 4 State-wise Transition

III. Comparison with Zero Switching time transient (ZSST[6]) Model

The ZSST[6] Model assumes the switching Time of Ferroelectric capacitor to be Zero . Zero Switching time implies that a charge increment of FE capacitor will take place instantly, therefore a charge increment is only a function of a applied voltage and initial state of a capacitor , not a function of time as shown in eq. 1.

Where V, ΔQinit represent the applied voltage and the initial polarization charge on the capacitor. Since there are only two initial states that are important to memory cell(i.e digital 0 and digital 1) (As from Equation 1) , the above equation can be broken into two parts ,[3] each corresponding to one initial state .

$$\Delta Q = \Delta Q0 \text{ for digital 0} \tag{2}$$

$$\Delta Q = \Delta Q1 \text{ for digital1} \tag{3}$$

The proposed CMOS model behavioral Model also exhibits the same properties as there are two important states (digital 1 and digital 0) are consider(As from Equation 2 and 3). The model only takes the two different voltages which are used to charge the capacitor at different values.

$$Q0 = CV1 \tag{4}$$

$$Q1 = CV2 \quad (5)$$

V1 and V2 are two different voltages. (As from Equation 4 and 5) The charge stored in the capacitor represent the different logic stored in FE capacitor, the waveform[3] [4] is given as

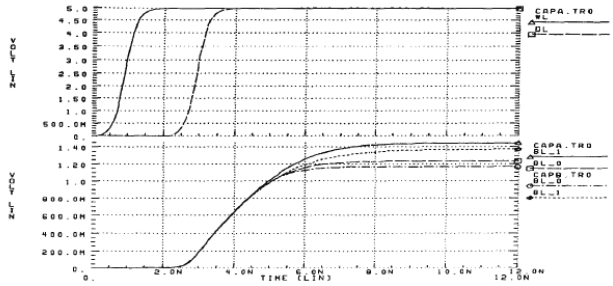

Fig. 5 Logic stored in FE capacitor

In ZSST[6] circuit representation C_0V_0 and C_1V_1 represents the two non-linear capacitors corresponding to the binary states of FE capacitor.(as from fig. 5 and 6)

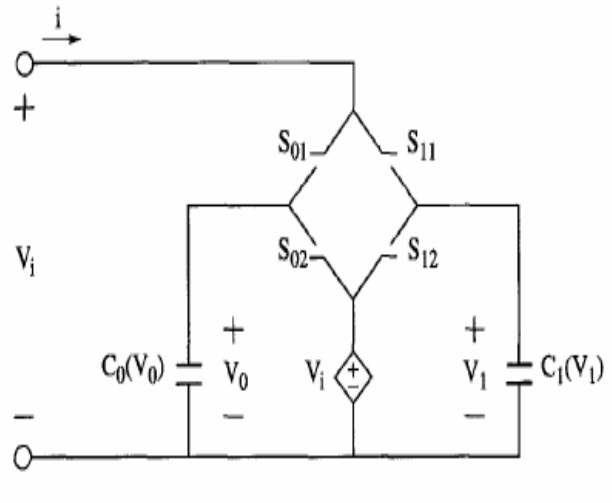

Fig. 6 Equivalent Capacitance of two capacitor are controlled by the switches

The Equivalent Capacitance of two capacitors are controlled by the switches S_{01}, S_{02}, S_{11}, S_{12} which are connected to controlled voltages V_i . The two different values of capacitors stored in two different logic states, are controlled by single voltage and controlled switches.

The proposed CMOS model having two different voltages, which are used to charged the single capacitor.

The advantage of this CMOS model is that the Single Capacitor is used for two different logics and the switching is done by two transistors NMOS and PMOS. The CMOS Model is Spice Macromodel [15-16] which can easily be implemented as Equivalent Model as in Appendix E in place of Ferroelectric Capacitor.

IV. Results and Conclusion

The Ferroelectric Random Access Memory mainly works on the principle of Hysterisis Loop , hence all the present model are based upon this hystersis loop. The Mathematical Model is just a representation of the loop in the mathematical form, it doesn't give us the Idea, how to Implement the circuit on the basis of the Mathematical Equations. The Distributed Threshold Switching Model in which dipole switches are employed for stable Binary logic. The capacitor which are used are Linear Capacitor , Non – Linear Parasitic Capacitor , NonLinear NonRemanent Capacitor , NonLinear Remanent Capacitor the combined Charactertics of Non- linear parasitic capacitor and NonLinear NonRemanent Capacitor give the two different values of distributed Voltage. In this Distributed Threshold Switching Model, the value of the capacitor is not perfectly designed so that we make Behavioral Model for Ferroelectric Capacitor.

Ferromagnetic based model, in this model ferroelectric (FE) and ferromagnetic (FM) materials are Duals in the sense that both exhibits similar hystersis loop characteristics. The B-H curve of FM core resembles the P-E Curve of an FE capacitor. This model having four critical points is chosen to quantify the B vs H hystersis loop. These Points can be translated into Saturation point (and its corresponding electri field), the remanent polarization, the corrosive field and Hence point on FE hystersis loop. These points are not modeled in this Ferromagnetic based Model. This Model doesn't give the Idea for the Implementation of Behavioral and Equivalent Model for FeRAM.

TABLE I
COMPARISON BETWEEN DIFFERENT TECHNOLOGIES

Model	Steady State	Transient	Strengths & weakness
Dual Capacitor Model	Yes	No	Approximate Macromodel
Mathematical Model	Yes	No	Complex
DTSM	Yes	No	Complex
Ferromagnetic Approximate Based model	Yes	No	Simple Macromodel
Current base Approximate Switching model	Yes	No	Accurate Macromodel RC Dependent
ZSTT Model Macromodel	Yes	No	RC Dependent
Proposed CMOS dependent Model	Yes	No	Accurate RC CMOS Macromodel

The Current based Switching Model is intended for both Transient and Steady State analysis. In this Model Current Source represents the switching current of the capacitor. It is assumes switching current is equal to the remenent Polarization of the Hystersis loop.

Hence, this Model gives transient analysis and gives the Idea (as from Table I) about the equivalent value of Current for Switching of Ferroelectric Random access memory.

The dual capacitor based model is based on the hystersis loop characteristics of Ferroelectric capacitor. This model

approximates the two branches of the hystersis loop by two straight lines. The switching of the dual capacitor model give us the idea for implementation of the behavioral Model for Ferroelectric capacitor. The two different value of charges gives the idea for the implementation in the design used as Equivalent Model FeRAM.[7-9]

Likewise Dual Capacitor model, the Zero Switching Time Transient Model (ZSST [6]) assumes the switching time of a ferroelectric capacitor to be zero. ZSST [6] implies that a charge increment of FE capacitor will take place instantly , hence charge increment is only a function of applied voltage and initial state of the capacitor. This model is transient in nature, this gives the idea if switching of ferroelectric capacitor and charging to two different values.

The proposed Behavioral Model exhibits transient and Steady state properties. The Behavioral CMOS model is based upon the switching of PMOS and NMOS transistors. The switching of these two transistors charges the capacitor with two different voltages which passes through these transistors. The two voltages V1 and V2 charges the capacitor with different values. Hence, these values of charge can be easily adjusted in the hystersis loop of Fe Capacitor[11]. The flexibility of this behavioral model is that we can change the values of two voltages V1 and V2, hence the charged stored in the capacitor will also changes. The comparison of behavioral characteristics of ZSST [6] is given in fig. 3.

The proposed Equivalent CMOS Model is based upon its Behavioral CMOS.

The bitline charges and discharges by the sweep voltage is given , the range of sweep voltage is -6 volts to +6 volts . This voltage switches the two transistors, the two voltages V1 and V2 are used to charged the capacitor upto two different values which shows the two different binary logic[12] (logic 1 and logic 0). The equivalent CMOS Model gives Flexibility to the user to charge the capacitor by changes the value of V1 and V2. This model is macro model, it only works for large size transistors, for future research the equivalent model should be of low power and having smaller transistors and also to requirement of the industry by change of time and trends.

The waveform given in Appendix D, gives the difference between the Proposed Behavioral CMOS Model and ZSST[6] Model. In Behavioral CMOS Model, the single Capacitor is used to Charge and Discharged using two Voltages V1 and V2. The output voltage, the capacitor charges from 2 volts and reaches up to 5 voltages. In ZSST[6] model, the two Capacitor C0 and C1 are charged by the voltage Vi. The capacitor from 0 volts upto 5 volts, the transient waveform shows the difference of charging and discharging of the capacitor when the Input voltage is given.

TABLE II
PROPOSED MODEL WORKING CHARACTERISTICS

ZSST[6] Model	**Proposed CMOS Model**
Input voltage range 0-5volts	Input voltage range 2-6 voltage
Logic 0 at 0 volts	Logic 0 at 2 volts
Logic 1 at 5 volts	Logic 1 at 6 volts
Dual Capacitor are used to Store the logic	Single Capacitor are used to store the logic

The waveform of ZSST [6] Model shows the speed of charging the Capacitor. The ZSST[6] Model required more time to charge up the capacitor C0 and C1 as the RC values increases with the number with capacitor(as from Table 2). Whereas in case of CMOS model, single capacitor is employed for storing the binary logic.

The logic descriptions of these Models are different as the switching is done at different Voltages. In CMOS model, the switching is done by PMOS and NMOS Transistors by providing sweep voltage at the Bitline range from -6volts and +6volts, where as switching is done by simple switching S01, S02, S10,S11.

TABLE III
PROPOSED MODEL BEHAVIOR CHARACTERISTICS

ZSST[6] Model	**Proposed CMOS Model**
Switching is done by Simple Switches	Switching is done by PMOS and NMOS transistors
Single Voltage Source is used, Vi = 5 volts	Dual voltage Sources are used V1=2volts and V2=5 volts
RC Values are higher as two Capacitors are used for storing Binary logics.	RC values are less as single capacitor is employed for storing Binary Logics.
Power consumption is higher due to reason of higher RC values	Power consumption is less due to less RC values.

The above Table III shows the difference in respect to design and power consumed by these two Models. These differences shows that CMOS Model is much faster then ZSST [6] model also give the user, flexibility to work at different voltages according to the application.

V. Netlist (algorithm) of Equivalent Model

```
* SPICE netlist written by S-Edit Win32 7.00
* Written on May 14, 2009 at 05:43:00
* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+probesdbfile="C:\Documents and Settings \CMOS\
Desktop \ eqi_model.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
C1 a Gnd 10pF
M2 a N1 N3 N8 NMOS L=2u W=22u AD=66p PD=24u
AS=66p PS=24u
M3 N1 N4 bl N7 NMOS L=2u W=22u AD=66p PD=24u
AS=66p PS=24u
M4 N11 N1 a N9 PMOS L=2u W=22u AD=66p PD=24u
AS=66p PS=24u
v5 N11 Gnd 2.0
v6 N4 Gnd 6.0
v7 N3 Gnd 5.0
v8 bl Gnd [10]pulse(-6.0 6.0 0 10n 10n 100n 200n)
.include "C:\Tanner\TSpice70\models\ml5_12.md"
.tran/op 10n 300n method=bdf
.print tran v(a) v(bl)
* End of main circuit: Module0
```

VI. Model File

```
.model nmos nmos level=5
+  Tox=2.323700E-08        Vmax=1.0E+5
+  Mu0=624.339618          Nsub=6.387808E+16
+  Vfb=-0.280000           Eghalf=1.692559E+8
+  Ld=2.00E-07             Wd=0.0
+  Xj=0.0                  Tref=27.00
+  Rsh=349.7               Cgdo=310.0E-12
+  Cgso=310.0E-12          Cgbo=340.0E-12
+  Cj=556.0E-6             Mj=435.0E-3
+  Cjsw=373.2E-12          Mjsw=344.0E-3
+  Pb=0.8                  Js=10.0E-6

Model pmos level=5
+  Tox=2.384850E-08    Vmax=1.0E+05
+  Mu0=226.135626      Nsub=1.064575E+16
+  Vfb=0.0800          Eghalf=8.738294E+07
+  Ld=-6.00E-07        Wd=0.0
+  Xj=0.0              Tref=27.00
+  Rsh=418.2           Cgdo=108.0E-12
+  Cgso=108.0E-12      Cgbo=625.0E-12
+  Cj=448.6E-6         Mj=404.0E-3
+  Cjsw=457.0E-12      Mjsw=334.0E-3
+  Pb=0.8              Js=10.0E-6
```

VII. Software Selection

Due to the expensive process of the foundry, it is advisable to first simulate the circuit before going in for the hardware. For that many software tools are available. We are using TANNER Tool for simulation of the SRAM memory cell using the 0.13µm technology and level 49. The T- SPICE Pro™ circuit simulation system. T- SPICE is a complete circuit design and analysis system that includes:

- *Schematic Editor S - EDIT:* S- EDIT is a powerful design capture and analysis package that can generate net-lists directly usable in T- SPICE simulations.
- *T - SPICE Circuit Simulator:* T- SPICE performs fast and accurate simulations of analog and mixed analog\digital circuits[12-14]and[17]. The simulator can analyze small and large, complex designs with hundreds of thousands of circuit elements.
- *Advanced Model Package:* It includes the latest and the best device models available, to help you to get the most realistic simulation results possible. This package also includes coupled line models and support for user defined device via tables for C functions.
- *W-EDIT Wave Form Viewer:* W- EDIT displays T-SPICE simulation output waveforms as they are being generated during simulation.

The design cycle for the development of the electronic circuits include an important prefabricated verification phase. Because of the expense and time pressure associated with the fabrication step, accurate verification is crucial to an efficient design process. The role of the T- SPICE is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit.

T- SPICE simulation results allow circuit designers to verify and fine- tune designs before submitting them for fabrication. T- SPICE in many ways is like the industry standard SPICE simulation program:-

- *Input language:* T-SPICE uses an extended version of SPICE's input language.
- *Analysis Mode:* T-SPICE performs the same basic analysis as does SPICE (DC, AC, transient and noise).

- *Device models:* T-SPICE incorporates all of SPICE's device models and more: resistors, capacitors, inductors, single and coupled transmission lines current sources, voltage sources, controlled sources, a full and complement of semiconductor device models for p-n diodes, BJT's, JFET's, MESFETs and MOSFETs.
- T-SPICE also incorporates several innovations and improvements not found in other SPICE and SPICE compatible simulators.
- *Speed:* The results of device model evaluations are stored in tables and reused. Because evaluation of device models can be computationally expensive, this technique can yield dramatic simulation speed increase. The memory used by T- SPICE tables is optimized by storing only those points that are actually needed. T- SPICE allows you to specify which devices are used.
- *Convergence:* T-SPICE uses advanced mathematical methods to achieve superior numerical stability. Large circuits and feedback circuits which are impossible to analyze with other SPICE products, can be simulated in T- SPICE.
- *Accuracy:* T-SPICE uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.
- *Advanced Models:* T-SPICE incorporates latest and best transmission- line and semiconductor device models to give you simulation results which are closer to real world behavior, including exclusive physically based Maher-Mead MOSFET.
- *Input language Extensions:* The T-SPICE input language is an enriched version of the standard SPICE language. It contains many enhancements including parameters, algebraic expressions, and a powerful bit and input wave specification syntax.
- *External model interface:* Users can develop custom device models using C or C++.
- *Run time waveform viewing:* The W-EDIT waveform viewers display graphical results during simulation. The T-SPICE analysis results for voltages, currents, charges and power can be written to single or multiple files.
- *Schematic entry:* T-SPICE provide schematic view draw.
- T-SPICE maintains compatibility with the traditional circuit simulation tools, while using the best available simulation technology to deliver results as quickly as possible.

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