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A Simplified Adaptive Decision Feedback Equalization Technique for $\frac{\pi}{4}$-DQPSK Signals

V. Prapulla, A. Mitra, R. Bhattacharjee and S. Nandi

Abstract— We present a simplified equalization technique for a $\frac{\pi}{4}$ differential quadrature phase shift keying ($\frac{\pi}{4}$-DQPSK) modulated signal in a multipath fading environment. The proposed equalizer is realized as a fractionally spaced adaptive decision feedback equalizer (FS-ADFE), employing exponential step-size least mean square (LMS) algorithm as the adaptation technique. The main advantage of the scheme stems from the usage of exponential step-size LMS algorithm in the equalizer, which achieves similar convergence behavior as that of a recursive least squares (RLS) algorithm with significantly reduced computational complexity. To investigate the finite-precision performance of the proposed equalizer along with the $\frac{\pi}{4}$-DQPSK modem, the entire system is evaluated on a 16-bit fixed point digital signal processor (DSP) environment. The proposed scheme is found to be attractive even for those cases where equalization is to be performed within a restricted number of training samples.

Keywords— Adaptive decision feedback equalizer, Fractionally spaced equalizer, $\frac{\pi}{4}$ DQPSK signal, Digital signal processor.

I. Introduction

IN a multipath environment within time disruptive channels, modulation bandwidth greater than the coherence bandwidth of the radio channel introduces *intersymbol interference* (ISI) resulting into high bit error rate (BER) [1]. The performance of communication links under such hostile conditions could be improved by employing an adaptive equalizer at the front end of the demodulator [2]. Adaptive decision feedback equalizer (ADFE) is one such equalizer which operates with the principle that once the value of the current symbol is determined, the ISI contribution of that symbol to future symbols can be estimated and removed. The mean square error of an ADFE is always smaller than that of an adaptive linear transversal equalizer unless the channel is ideal [3]. Employing an ADFE, therefore, is more appropriate for severely distorted wireless channels. Such an equalizer proposed for U.S. Digital Cellular (USDC) standard is a fractionally spaced decision feedback equalizer [4]. A fractionally spaced equalizer (FSE) is preferable to a symbol rate equalizer when the channel characteristics are unknown to the receiver as the usage of fractional spacing in those conditions makes the equalizer robust against sample timing jitter [5]-[6]. The optimum FSE is equivalent to the optimum linear receiver consisting of a matched filter followed respectively by a symbol rate sampler and a symbol rate equalizer.

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V. Prapulla, A. Mitra and R. Bhattacharjee are with the Department of Electronics and Communication Engineering, Indian Institute of Technology (IIT) Guwahati, India – 781039. E-Mail: (prapulla, a.mitra, ratnajit)@iitg.ernet.in.

S. Nandy is with the Department of Computer Science and Engineering, Indian Institute of Technology (IIT) Guwahati, India – 781039. E-Mail: sukumar@iitg.ernet.in.

To update the above mentioned equalizer coefficients over each iteration, some of the most commonly used algorithms are least mean square (LMS) and recursive least squares (RLS). A relatively new method, based on projection onto convex sets (POCS) [7], which is realized in a particular form of LMS recursion, has also proved its appropriateness for tailoring itself to the characteristics of the channel. However, all these techniques have relative merits and demerits over each other. While conventional LMS algorithm has slow convergence compared to RLS, the latter introduces high computational complexity in comparison with the former. The convergence speed and computational complexity of the POCS method depend mainly on newly introduced look back parameter, which, for achieving convergence speed comparable to RLS, increases the computational complexity close to RLS. Therefore, from implementation point of view, there is a need to investigate low complexity equalizer adaptation techniques with faster convergence and smaller memory requirement. In practice, apart from the low complexity and low power consumption, the most crucial parameter for such implementation schemes is the convergence accuracy within certain given number of samples, in contrary to the steady state concept of the theoretical analysis.

Apart from equalizers, a modem (modulator/demodulator) also plays a key role in digital communication system as it determines the signal mapping, baseband filtering and modulation type, which , in turn, control the bandwidth utilization, bandwidth efficiency and BER performance of that system. Although binary modulation systems are less spectrally efficient than multistate M-ary systems, but they are also less complicated and power efficient when compared to the latter. However, due to restricted spectrum availability, bandwidth efficient modulation techniques are generally given the priority in wireless communications. It is, thus, always preferred to explore the possibility of having an easily realizable modem with relatively high spectral efficiency. $\frac{\pi}{4}$-DQPSK is one such widely used modulation technique (used in IS-54 North American Digital Cellular (NADC) standard) in wireless communication. Moreover, it offers 20% more spectral efficiency than that of Gaussian minimum shift keying (GMSK) modulator [4], as well as it can also be detected non-coherently.

In this paper, we propose an efficient low complexity fractionally spaced adaptive decision feedback equalizer (FS-ADFE). The FS-ADFE under consideration employs exponential step-size LMS algorithm to yield faster convergence with low computational complexity. Such algorithm has successfully been used for smart antenna beamforming [8] applica-

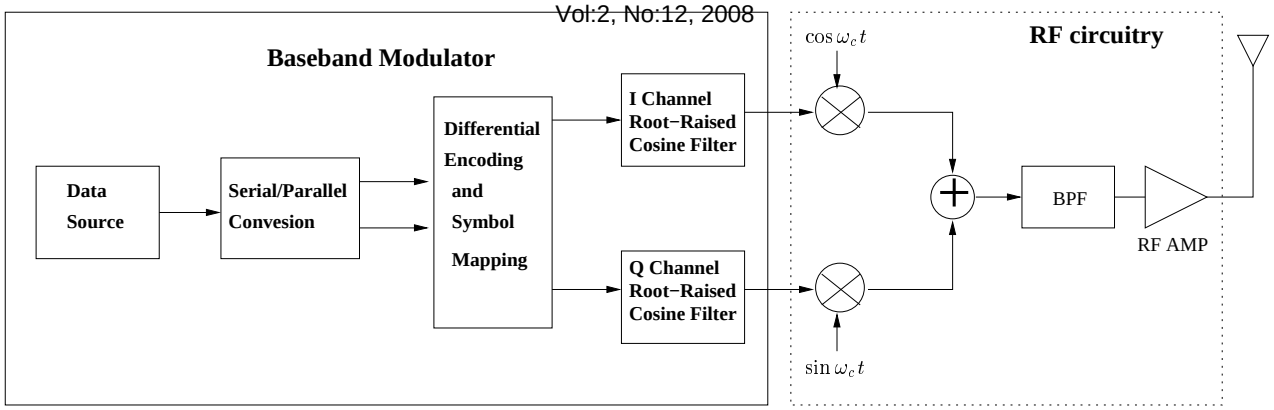

Fig. 1. Block diagram of $\frac{\pi}{4}$-DQPSK Transmitter.

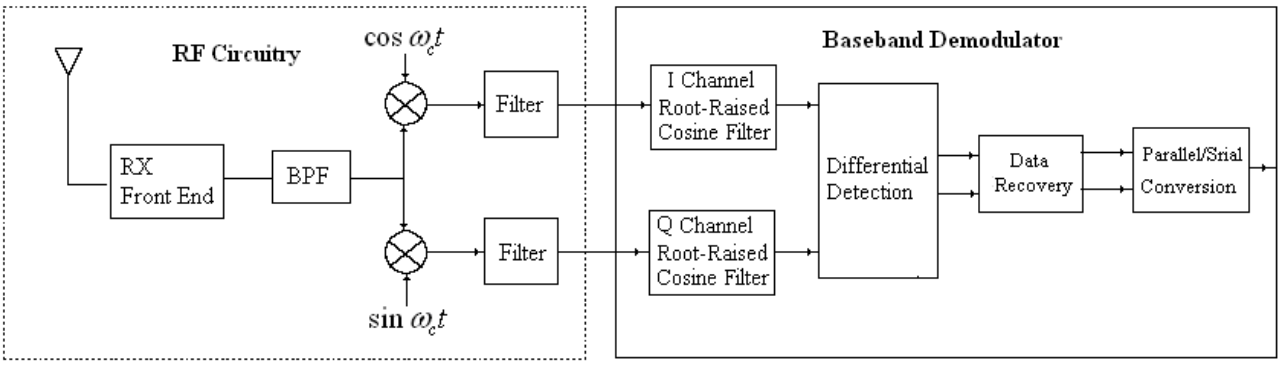

Fig. 2. Block diagram of $\frac{\pi}{4}$-DQPSK Receiver.

tions. The performance of this adaptive equalizer is evaluated with a $\frac{\pi}{4}$-DQPSK modulated signal in a multipath fading environment. The proposed FS-ADFE, along with the $\frac{\pi}{4}$-DQPSK modem, is evaluated on a 16-bit fixed point digital signal processor (DSP) environment with visual DSP (VDSP). The performance of the proposed scheme has also been evaluated and compared with LMS, RLS and POCS. Further, the computational complexity for DSP implementation has been investigated and the proposed scheme has been found to be a viable alternative as compared to the other three techniques from the view point of convergence, memory requirement and implementation complexity.

The overall organization of the paper is as follows: in Section 2, a brief overview of a $\frac{\pi}{4}$-DQPSK modem is given. Section 3 discusses about the proposed FS-ADFE scheme, emphasizing on the adaptation algorithm followed in the equalizer under consideration. In Section 4, implementational details of the entire scheme in a 16-bit fixed point VDSP environment, targeted for ADSP-2189M processor, is discussed. Section 5 highlights on the results and discussions on a few implementational points of the proposed approach and the paper is concluded in Section 6.

II. $\frac{\pi}{4}$-DQPSK Modem

Block diagram of a generic $\frac{\pi}{4}$-DQPSK transmitter is shown in Figure 1. Here, the input bit stream is partitioned by a serial-to-parallel (S/P) converter into two parallel data streams, m_{Ik} and m_{Qk}, each with a symbol rate equal to half that of the incoming bit rate. The choice of the particular phase θ_k, at the kth symbol period, within a constellation set depends on the aforementioned dibit inputs and the previous phase θ_{k-1}. The present phase θ_k can be written as $\theta_k = \theta_{k-1} + \Delta\theta$, where the phase difference $\Delta\theta$ depends on m_{Ik} and m_{Qk} as per the following mapping rule: $(11, 01, 00, 10) :\rightarrow (\pi/4, 3\pi/4, -3\pi/4, -\pi/4)$. With the help of this, the kth in-phase and quadrature pulses (I_k and Q_k) at the output of the signal mapping circuit are determined by the following set of equations:

$$I_k = \cos\theta_k = I_{k-1}\cos\Delta\theta - Q_{k-1}\sin\Delta\theta, \qquad (1)$$

$$Q_k = \sin\theta_k = I_{k-1}\sin\Delta\theta + Q_{k-1}\cos\Delta\theta. \qquad (2)$$

The $\frac{\pi}{4}$-DQPSK constellation is formed by superimposing two QPSK signal constellations offset by $\frac{\pi}{4}$ relative to each other, resulting in eight signal phases. During each symbol period, a phase angle from only one of the two QPSK constellations is transmitted and these two are used alternately to transmit every dibit. To reduce dibit errors in the receiver, Gray coding

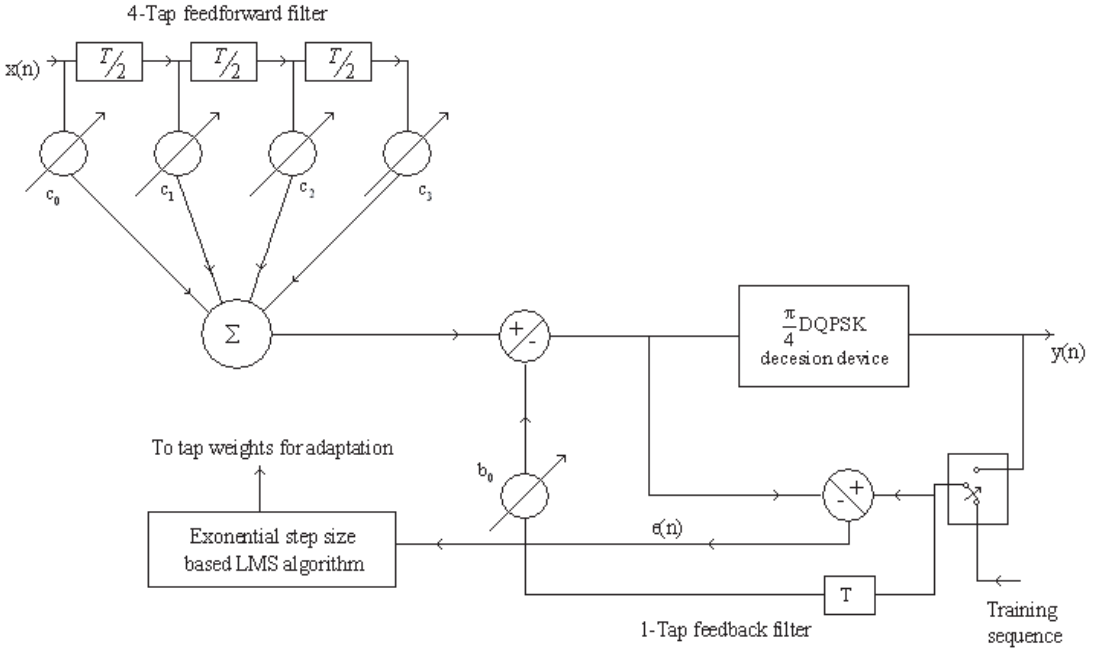

Fig. 3. The proposed fractionally spaced adaptive decision feedback equalizer.

of dibits (two dibit symbols corresponding to adjacent signal phases differ only in a single bit) is done prior to phase selection from a chosen constellation set. The final $\frac{\pi}{4}$-DQPSK waveform is given by

$$S_{\frac{\pi}{4}-DQPSK}(t) = I(t)\cos\omega_c t - Q(t)\sin\omega_c t \qquad (3)$$

where I_k and Q_k are separately modulated by two carriers which are in quadrature with one another. Note that the pulses I_k and Q_k and the peak amplitude of the waveforms $I(t)$ and $Q(t)$ can take one of the five possible values: $0, \pm 1, \pm\frac{1}{\sqrt{2}}$.

The main advantage of such a received $\frac{\pi}{4}$-DQPSK signal is that it can be demodulated either coherently or non-coherently. In a mobile environment, disturbances such as multipath fading, Doppler frequency shifts, burst noise and phase noise may severely degrade the received signal. Under such conditions, non-coherent detection is often advantageous. In literature, three types of such non-coherent detection techniques have been proposed [9], namely, baseband differential detector, IF band differential detector and FM discriminator detector. All these three receivers offer similar bit error rate performance, although there are implementation issues which are specific to each technique [10]. In this paper, baseband differential detection is considered for implementation on fixed point DSP because of its simplicity. Figure 2 shows the block diagram of a generic $\frac{\pi}{4}$-DQPSK receiver. The incoming $\frac{\pi}{4}$-DQPSK signal is quadrature demodulated in the RF part using two local oscillator signals that have the same frequency as the unmodulated carrier at the transmitter, but not necessarily the same phase. Since the phase error is removed by differential detection at baseband, phase coherence is not needed. These I and Q signals are then passed through the matched filters in the receiver. Since the baseband I and Q signals at the transmitter are filtered by square-root raised-cosine pulse shaping filters, the matched filters at the front end of the receiver are designed to give the same frequency response so that the combined receiver/transmitter response becomes raised cosine. The differential detection retrieves the cosine and sine functions of the phase difference between two successive symbol intervals. The dibit information thus transmitted is decoded at the decision circuit with the following hard decision rules.

$$a_I = 0 \quad if \quad X_k < 0; \quad a_I = 1 \quad if \quad X_k > 0 \qquad (4)$$

$$a_Q = 0 \quad if \quad Y_k < 0; \quad a_Q = 1 \quad if \quad Y_k > 0 \qquad (5)$$

III. The Proposed FS-ADFE

The basic ADFE structure comprises of two adaptive transversal filters – a feedforward one as well as a feedback one. The input to the feedforward filter is the received signal $x(n)$ and the feedback filter is fed with a known sequence as either the training sequence during the training mode or the previous decisions during the decision directed mode. The feedforward section thereby compensates for the ISI arising from multipath degradation whereas the feedback section mainly takes care to remove the ISI arising due to previous symbols. The postcursor ISI removal is accomplished by the use of this feedback filter structure [11]. Note that an equalizer can only equalize a signal over delay intervals less than or equal to the maximum delay within the filter structure. Also, the circuit complexity and processing time of the equalizer increases with the number of taps and delay elements. Keeping these points into consideration, the FS-ADFE used in this scheme is implemented by (i) a four tap feedforward filter with three delay elements spaced at $\frac{1}{2}$ symbol period to equalize one symbol time delay, and (ii) a feedback filter with one tap, delayed by one symbol period. The proposed ADFE structure is shown in Figure 3.

In order to track the time disruptive communication channel, any such adaptive equalizer uses an algorithm that updates the tap weights according to an output error signal $e(n)$ at any nth index along with certain other parameters. Proper choice of this coefficient update algorithm is very significant for equalizers and is chosen carefully based on the convergence, misadjustment, computational complexity and memory requirement of the algorithm under consideration. In the following subsection, we describe the coefficient update technique adopted in the proposed FS-ADFE, taking care of all the above factors.

A. Adaptation algorithm in the proposed FS-ADFE

The conventional LMS algorithm has been widely used in various applications of ADFE for its low computational complexity. Since LMS algorithm is a stochastic gradient procedure, an appropriate step size (μ) must be selected for desired convergence, as, a small μ could ensure small mean square error (MSE) in steady state but convergence becomes slow, whereas a large μ could provide faster convergence but results in somewhat higher MSE in steady state [12]. An alternative to such a gradient estimate is to consider error measures that do not include expectations and that may be computed directly from the data. A least squares error requires no statistical information about the input data samples $x(n)$ and the desired sequence $d(n)$. As a result, the filter coefficients that minimize the least squares error will be optimal for the given data rather than statistically optimal over a particular class of process and RLS is a well known algorithm based on the above-mentioned method of least squares. The RLS algorithm, though converges faster than its LMS counterpart, is computationally complex than the latter due to large number of operations per iteration. In the paper [7], an iterative procedure based on the normalized LMS (NLMS) has been investigated. An adaptation technique has been proposed based on the POCS method for faster convergence, in which each data vector is used more than once based on a look-back parameter. For large number of training symbols, its code and memory size requirements are also smaller compared to RLS. However, for application in practical cases where the required convergence is to be achieved in a relatively small training period interval under large Doppler spread conditions, look back parameter becomes large. As for example, in IS-54 NADC system, coefficients should converge in the training mode within 14 symbols of the training sequence. To track such a system with 40 Hz Doppler spread and varying multipath delays, a look-back parameter larger than seven is required in POCS method, which, in turn, implies all such previous data vectors must be stored in memory. Taking these points into account, a computationally efficient yet faster convergence algorithm is employed in the proposed ADFE.

In the proposed equalizer, an exponential step size based LMS algorithm [8] has been used for weight updating with faster convergence as well as lower MSE. In the most common form of a length L LMS based adaptive filter, it takes an input sequence $x(n)$ and updates the tap weight vector $\mathbf{w}(n)$ as

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu \mathbf{x}(n) e(n) \tag{6}$$

where $\mathbf{x}(n) = [x(n)x(n-1)...x(n-L+1)]^T$, $e(n) = d(n) - \mathbf{w}^T(n)\mathbf{x}(n)$ denotes the error signal with $d(n)$ and μ having the same meaning as defined earlier. In the exponential step size based LMS algorithm, the step size μ is updated with each iteration n and this time recursive $\mu(n)$ is given as

$$\mu(n) = \mu_0 \exp(b||\mathbf{x}(n)e(n)||_2) \tag{7}$$

where μ_0 and b ($b \geq 0$) are constants and $||.||_2$ denotes the Euclidean norm. For simplifying calculations, eq. (7) can be approximated as

$$\mu(n) \approx \mu_0[1 + b||\mathbf{x}(n)e(n)||_2] \tag{8}$$

as $\exp(x) \approx (1+x)$ for $x \ll 1$. Note that in order for this LMS based algorithm to converge, $\mu(n)$ must satisfy the condition

$$0 < \mu(n) < \frac{2}{tr(\mathbf{R})} \tag{9}$$

where $\mathbf{R} = E[\mathbf{x}(n)\mathbf{x}^H(n)]$, $tr(.)$ represents the trace operator, $E[.]$ denotes expectation operation and the superscript H stands for hermitian transpose. Initially, μ_0 and b are chosen as very small positive real numbers to satisfy eq. (9).

To meet the practical system requirements like that of IS-54, the proposed FS-ADFE with exponential step-size based LMS algorithm gives desired performance in terms of weight updating in a short training interval, at the same time keeping both complexity and resource requirement minimal. Such properties are also desirable for emerging software defined radio (SDR) systems where modulation, demodulation and equalization are performed using DSP/FPGA. To investigate the finite-precision performance of the proposed equalizer along with the aforesaid modem, the entire scheme is evaluated on a 16-bit fixed point DSP environment and is described next.

IV. Implementation of the Proposed Scheme

The FS-ADFE along with the $\frac{\pi}{4}$-DQPSK modem has been evaluated in a 16-bit fixed point VDSP environment in accordance with the IS-54 standard specifications, where the data rate is 48.6 $kbps$. This corresponds to a symbol rate of 24.3 $kbaud/s$, as every symbol comprises of two bits. Four samples per baud has been taken for both the modulator and the demodulator. The baseband filters at the modulator thus generate four filtered samples/baud thereby requiring a sampling frequency of 97.2 kHz. In the simulation, the timer is set to generate interrupts at the rate of 97.2 kHz. Note that the VDSP environment can be tailored with the same computational blocks as those are in 16-bit fixed point ADSP-2189M processor. This processor has the computational capacity of 75 MIPS, 32k words (24-bit) of Program Memory RAM and 48k words (16-bit) of Data Memory RAM on chip. Along with that, the DSP system also consists of AD73322 codec on the board which has two A/D conversion channels and two D/A conversion channels. These two channels, here, have been utilized separately for the baseband in-phase and quadrature signal components.

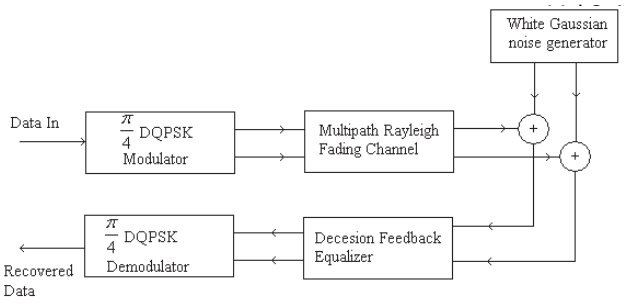

Fig. 4. Block configuration of the proposed scheme for Performance testing in VDSP environment.

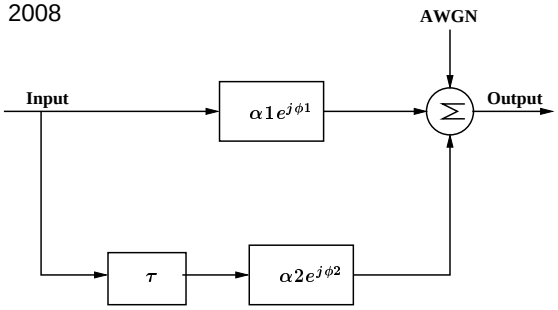

Fig. 5. Two-ray Rayleigh faded channel model corrupted by AWGN.

Figure 4 shows the block configuration of the entire scheme. The samples of the modulator output are stored in a buffer and saved into a file. These I and Q samples are passed through the multipath Rayleigh fading channel. Note that as the approach is used as a part of NADC IS-54 standard, the simulation parameters are also chosen conforming to the same standard. The IS-54 Rayleigh faded channel model is specified with a faded main ray and another independently faded delayed ray. The limit on the amount of delay is one symbol time (41.17 μs). This two-ray Rayleigh fading model is recommended by the Telecommunications Industry Association (TIA) standard committee to evaluate the tolerance of delay spread in digital cellular systems [13]. In the channel model for our purpose, as shown in Figure 5, $\alpha 1$ and $\alpha 2$ are independent and Rayleigh distributed, $\phi 1$ and $\phi 2$ are independent and uniformly distributed over [0, 2π], and τ is the time delay between the two rays. The white Gaussian noise samples, obtained from MATLAB simulation, are added to these faded samples and are passed to the FS-ADFE. The output of the equalizer is differentially detected at the demodulator and data is recovered. In the following, we first provide a brief account of implementation of the $\frac{\pi}{4}$-DQPSK modem, followed by the the proposed FS-ADFE.

A. $\frac{\pi}{4}$-DQPSK modem implementation

The block diagram of the finite precision modem implementation is shown in Figure 6. In the modulator, the symbol mapping has been performed by a look-up table technique using circular buffers, which depends on the input information bits and the previous constellation point. After the signal mapping, I and Q pulses are spectrally shaped to reduce intersymbol interference using a 24 tap square-root raised-cosine FIR filter with the roll off factor of 0.35 as per the IS-54 standard. If a digital filter is used for pulse shaping then it must operate at a sampling rate of at least twice the data rate to span the frequency response characteristic of the raised cosine pulse [15]. A polyphase interpolation filter has been used to reduce computations by a factor of four compared to the direct filtering. This necessitates the use of four interrupts per symbol period. The filter coefficients have been obtained from MATLAB simulation and stored in a program memory. The 24 filter coefficients are divided into four blocks of six coefficients in each. The appropriate set of coefficients is used by filters in the four consecutive interrupts. The same set of coefficients are used for both I and Q pulses filtering as they do not change over the complete symbol period. This, in turn, means once the new I and Q values are accessed after signal mapping in the first interrupt, these values remain unchanged for the next three interrupts and thus the required interpolation factor of four is achieved. As a result, the number of coefficients used in multiplication to calculate each output sample reduces to $24/4 = 6$. Therefore, the interpolation by using polyphase filters save three-fourth of the time required to run a normal filter. After square-root raised cosine filtering, the filtered I and Q samples are passed separately to the two D/A converters of AD73322 codec and from the left and right channels of AD73322, $\frac{\pi}{4}$-DQPSK modulated in-phase and quadrature signals are obtained respectively. As the maximum sampling rate of AD73322 codec is 64 kHz, the input data rate is limited to 32 kbps to match the codec specifications.

These two signals, processed by two-ray Rayleigh fading channel and the FS-ADFE respectively, are then fed to the left and right channels of AD73322 codec on another processor. The two ADCs on AD73322 convert analog input to digital samples and send it serially to the SPORT on an ADSP-2189M processor [16]. The received samples are filtered using square-root raised cosine filter to match the transmitter's filter, i.e., a 24 tap FIR filter similar to the modulator operating at the sampling rate of 64 kHz and the same coefficients for both I and Q samples filtering. Again, four samples per baud are chosen for the demodulator implementation. The filtered samples are then fed to the differential detection block where data are recovered according to the phase change between the two successive symbol intervals.

B. Equalizer implementation

A decision feedback equalizer can be efficiently implemented on the ADSP-2189M because this core has two arithmetic logic units (ALUs) and special instructions for computing complex numbers. For implementing FS-ADFE in our case, few constraints were set on the Rayleigh faded channel-impulse response and the number of filter taps to improve the efficiency of the DSP implementation. The constraints are (i) all the entries of the channel-impulse response should be less than one as the ADSP-2189M is a fixed point processor, and (ii) the length of the channel-impulse response and the length of the feedforward filter tap (in this case, it is four) should be constrained. Also, the channel-impulse response is assumed to

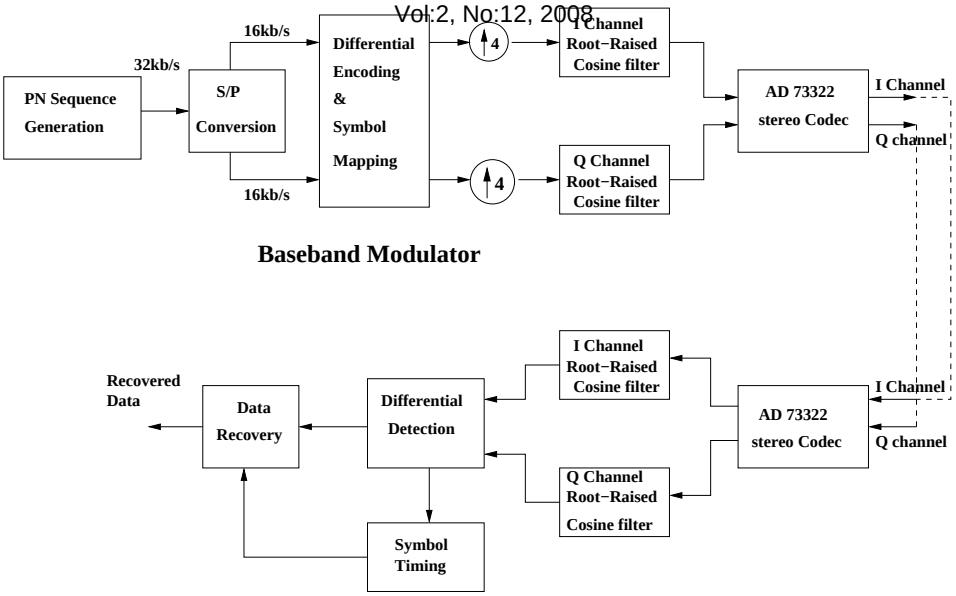

Fig. 6. Baseband unit of a 32kbps $\frac{\pi}{4}$-DQPSK modem on ADSP-2189M system.

be stored in memory as ADSP-2189M has a very large on-chip memory of 1.5 MB. The incoming data stream and the computed output are stored in two different registers and using these values, the filter tap weights are updated according to eq. (1) and (3). In the implementation, the values of μ_0 and b are kept 0.015 and 0.15 respectively which yield almost as fast convergence as comaperd to RLS.

V. Results and Discussions

The performance of the FS-ADFE under consideration employing exponential step size LMS algorithm as discussed is compared with those cases when only the adaptation algorithm is changed to LMS, RLS or POCS. In order to perform this comparison, the scheme as shown in Figure 4 is simulated in VDSP environment, separately for each of the algorithms mentioned above. Figure 7 presents this comparative performance in terms of convergence speed and mean square error in Rayleigh fading channel with different Doppler and delay spreads. In this figure, error magnitudes as a function of time between the output of the equalizer and the decision device are plotted. For the case of LMS, a step size of 0.03 is found to give a reasonable mean sense convergence within the training sequence duration. It is also observed that with this value, the steady state MSE for LMS comes highest in comparison with other algorithms. It is seen that computationally expensive RLS has fastest convergence with smaller steady state MSE in comparison with POCS. From simulations, it is also found that the exponential step size LMS algorithm, having μ_0 and b as specified earlier, achieves faster convergence with smaller MSE in steady state in comparison with conventional LMS as well as a convergence speed as fast as POCS recursion. The eye patterns corresponding to $\frac{\pi}{4}$-DQPSK modulated signal, the faded signal and the equalized signal are shown in Figure 8. The signal constellation for unfaded, faded and equalized signals are shown in Figure 9. All these figures demonstrate the effectiveness of the proposed approach.

It has also been observed that number of DSP operations required by the proposed equalizer are less compared to equalizer employing RLS algorithm. This is because of the division operations of RLS algorithm which consume more cycles. Figure 10 shows the equalizer error magnitude square, obtained from the DSP system under consideration, for one TDMA frame of data which contains three time slots. Here, calculation of $\mu(n)$ in each iteration typically requires (6N+10) cycles, which can be considered as the additional overhead compared to conventional LMS algorithm. Note that the $\frac{\pi}{4}$-DQPSK modem runs at 64 kHz, which is the maximum sampling frequency of the on board codec and the interrupts have been generated accordingly. Therefore, the complete processing of the sample must be completed in $1/64000 = 15.625 \times 10^{-6}$ seconds. As ADSP-2189M instruction rate is 75 MIPS (13 ns), the total number of instructions that can be allowed is $15.625 \times 10^{-6}/13 \times 10^{-9} = 1202$. In VDSP simulation, using a on-chip timer, the routines are checked and found that they conform to the allowed number of instruction cycles.

VI. Conclusions

A fractionally spaced ADFE employing exponential step size based LMS adaptation technique has been proposed in this paper for equalizing $\frac{\pi}{4}$-DQPSK modulated signals in multipath Rayleigh fading channel. The entire scheme is evaluated in a 16 bit fixed point VDSP environment, targeted for ADSP-2189M based system. The performance of this equalizer has also been evaluated with respect to other adaptive algorithms such as LMS, RLS and POCS. It has been found that proposed

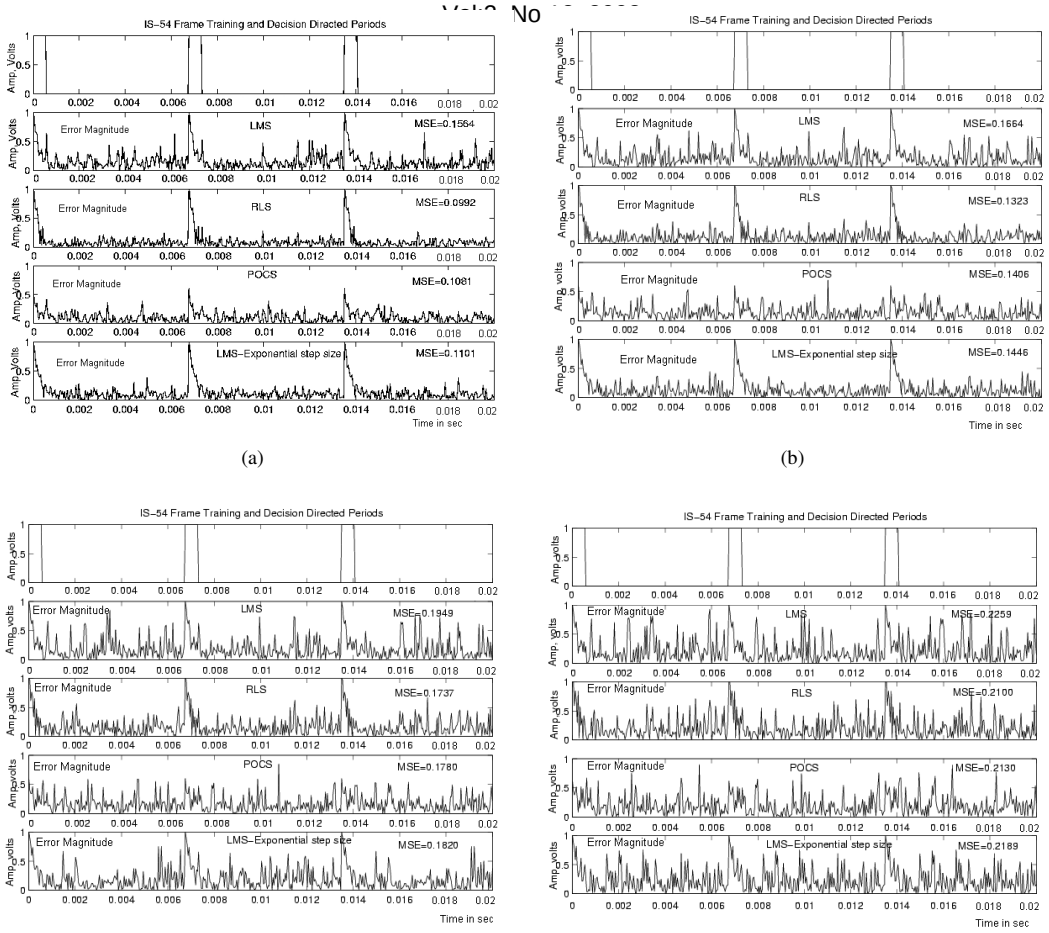

Fig. 7. Performance comparison of LMS, RLS, POCS and exponential step size based LMS algorithms in terms of convergence speed in Rayleigh faded channel for (a) Doppler spread of 5 Hz and delay spread of 1/8 symbol, (b) Doppler spread of 15 Hz and delay spread of 2/8 symbol, (c) Doppler spread of 30 Hz and delay spread of 3/8 symbol, and (d)Doppler spread of 30 Hz and delay spread of 4/8 symbol.

equalizer matches the performance of RLS in terms of convergence speed and mean square error with less computational complexity and smaller memory requirements. Further, the performance of the $\frac{\pi}{4}$-DQPSK modem has also been tested in AWGN environment and compared with the theoretical BER performance. The results show a degradation of about 2 dB when compared with the theoretical values, which is well within the acceptable limit. The entire scheme, therefore, can be an attractive option as compared to other techniques from the view point of practical systems complexity as well as convergence.

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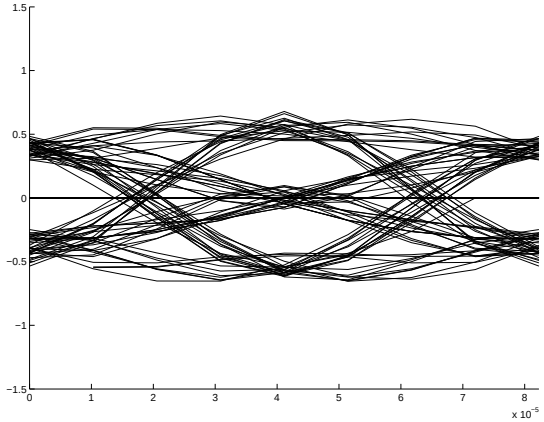
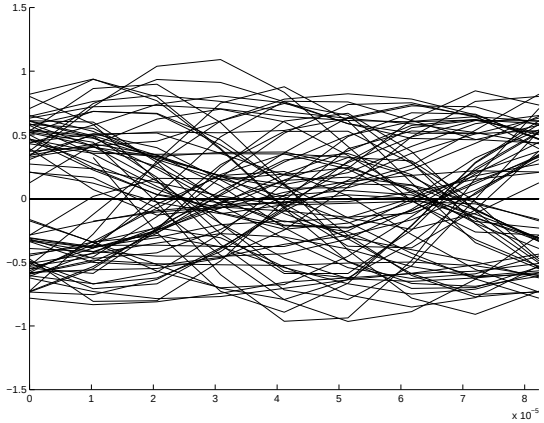


(a)



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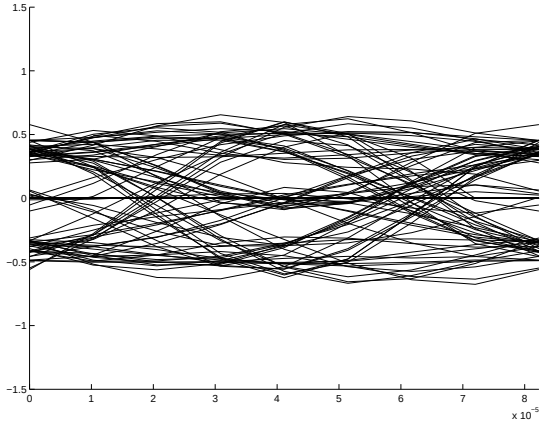
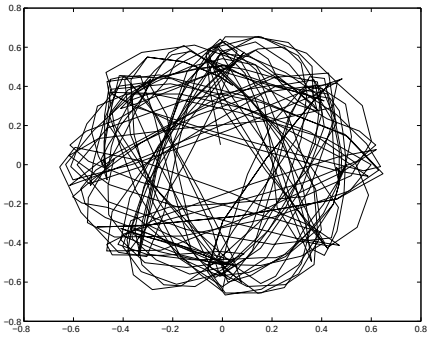
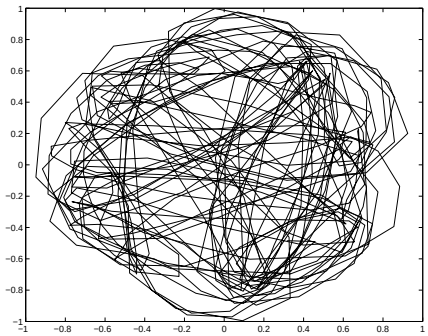


(c)

Fig. 8. Eye diagrams. (a) $\frac{\pi}{4} - DQPSK$ modulated eye diagram. (b) Faded Eye diagram. (c) Equalized Eye diagram.



(a)



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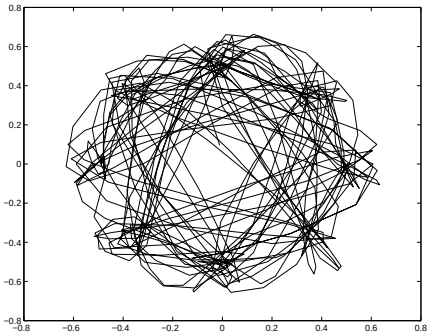

(c)

Fig. 9. Signal constellations. (a) $\frac{\pi}{4} - DQPSK$ Modulator constellation. (b) Faded constellation. (c) Equalized constellation.

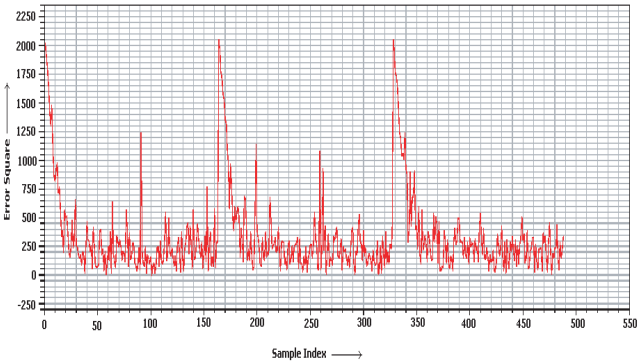

Fig. 10. Error magnitude square of the proposed FS-ADFE, in one TDMA frame for three time slots.