

# A Review of in-orbit Observations of Radiation-Induced Effects in Commercial Memories on-board Alsat-1

Y. Bentoutou, A.M. Si Mohammed

**Abstract**—This paper presents a review of an 8-year study on radiation effects in commercial memory devices operating within the main on-board computer system OBC386 of the Algerian microsatellite Alsat-1. A statistical analysis of single-event upset (SEU) and multiple-bit upset (MBU) activity in these commercial memories shows that the typical SEU rate at Alsat-1's orbit is  $4.04 \times 10^{-7}$  SEU/bit/day, where 98.6% of these SEUs cause single-bit errors, 1.22% cause double-byte errors, and the remaining SEUs result in multiple-bit and severe errors.

**Keywords**—Radiation Effects; Error Detection and Correction; Satellite Computer; Small Satellite Mission.

## I. INTRODUCTION

**E**RROR DETECTION AND CORRECTION (EDAC) devices on-board satellites aim to secure data transmitted between the central processing unit (CPU) of a satellite onboard computer and its local memory [1]-[5]. In space applications it is well known that in Low Earth Orbits (LEO), stored digital data suffers from Single Event Upsets (SEU). These upsets are induced naturally by radiation. Bit-flips caused by SEU are a well-known problem in memory chips and error detection and correction techniques have been an effective solution to this problem [1]-[5]. For the transmission of secure data between the CPU of the on board computer and its local RAM, the program memory on small satellites have generally made use of Hamming (12,8) code EDAC, or have used TMR, which is a hardware implementation that includes replicated memory circuits and voting logic to detect and correct a faulty value [1]-[3]. These error correction techniques are well-known and widely used. The Hamming (12,8) code allows the correction of a single bit per word. For computers on board a satellite, there is however a definite risk of two or more bit errors occurring within one byte of stored data; either from the impact of a particularly energetic event, or from a second SEU creating a second error [1]-[5]. As a result, later SSTL satellites made use of the TMR voting EDAC technique, which can correct any number of bit-flips in a single byte. This scheme offers excellent protection against the effects of SEUs and single-byte multiple-bit upsets (MBUs) but it cannot correct severe errors, i.e., bit-errors affecting the same logical bit position in more than one of the three physical memory locations. Another disadvantage of TMR is the large memory overhead of 200% in terms of storage [3].

In recent work, a new real-time, low-complexity codec has been described and implemented in FPGA technology for application to small satellite solid-state data recorders, such as the one operating on-board Alsat-1[1]. Another powerful EDAC architecture has been developed recently for implementation in future Algerian Earth Observation satellites, such as the Alsat-1 in order to reduce the total number of SEU in LEO [3].

This paper aims to present a follow-up of the statistical analysis of SEU and MBU activity in commercial memories onboard Alsat-1. The in-orbit observations show that the typical SEU rate at Alsat-1's orbit is  $4.04 \times 10^{-7}$  SEU/bit/day, where 98.6% of these SEUs cause single-bit errors, 1.22% cause double-byte errors, and the remaining SEUs result in multiple-bit and severe errors.

## II. SMALL SATELLITE MISSIONS

Earth observation missions using small satellites in LEO provide fast and cheap access to space [6]. To make a start-up in space technologies in Algeria, the National Center for Space Technology (CNTS) has initiated a small satellite project named Alsat-1. Alsat-1 is the first step in CNTS's plan to develop Algeria's national space infrastructure [7]. It is part of a wider international collaboration to launch the first disaster monitoring constellation of Earth observation satellites. The primary goal of the mission is to provide daily imaging worldwide for the monitoring and mitigation of natural and man-made disasters as well as dynamic Earth observation.

Alsat-1 was launched into a 686 km sun-synchronous orbit in November 2002. This microsatellite carries specially-designed Earth imaging cameras which provide 32-meter resolution imaging in 3 spectral bands (green, red, and near infrared) with an extremely wide imaging swath of 600 km on the ground that enables a revisit of the same area anywhere in the world at least every 4 days with just a single satellite. Images are stored in an 8-Gbit Solid State Data Recorder (SSDR) for high capacity onboard storage of image data, and transmission to the ground is via an 8-Mbps S-band downlink [3].

The Alsat-1 main On-Board Computer (OBC) is an Intel 80C386EX based system that was designed, built and tested at Surrey Satellite Technology Limited (SSTL), a company owned by EADS-Astrium at the University of Surrey in Guildford, UK.

The OBC plays a dual role for Alsat-1, acting as the key component of the payload computer as well as the command and control computer for the microsatellite. It has also been adopted by several other satellite projects [3].

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The OBC is a general purpose computer for space applications. It features 4 Mbytes of program memory which is protected by error detection and correction (EDAC) and 32 Kbytes of firmware storage EPROM. The EDAC is implemented using Triple Modular Redundancy (TMR) with voting logic, requiring 12 Mbytes in total. The board also supports multiple data inputs and can store a maximum of 128 Mbytes of data. This memory is normally referred to as the Ramdisk. Compared to the program memory there is no hardware protection on the Ramdisk, instead a double-error correcting modified Reed-Solomon RS (256,252) code is used [4]. The encoding and decoding process is executed entirely in software. Data are transferred in 256-byte blocks, which comprise 252 bytes of information, three RS code bytes and one byte is used to give the capability of double byte correction. The RS (256,252) code can correct any number of bit-errors affecting no more than two bytes per block. Thus, three or more bytes would have to be affected to cause a "severe" error under this scheme [4].

### III. IN-ORBIT OBSERVATIONS

Since Alsat-1 is placed in a LEO of 686 km, elevated levels of radiation caused by the lack of atmosphere increase the probability of SEUs. A SEU is a non-destructive error which usually affects logic cells in such a way that it can cause a bit in a memory device to change logic states. This phenomenon is caused by a false charge created by the transit of a single ionizing particle through a memory chip. There are various methods of error detection and correction, but the most commonly used solutions are based on Hamming and Reed-Solomon codes, and TMR.

In this paper, the period of the in-orbit observations includes the whole Alsat-1 life-time (i.e. from November 29 2002 to August 14 2010). The Ramdisk memories are based on eight Samsung SYS 84,000 parts of 4 Mbytes each in size. In Fig. 1, the yearly average of the number of SEU/day is plotted for the period from 29/11/2002 to 14/08/2010. This figure shows the increase of the upset rates with the increasing time. During this period, in 2,622 days of observation, 265,649 errors were logged in the memory devices, giving a mean error rate of  $4.04 \times 10^{-7}$  error/bit/day. In 2002 and 2010, the average SEU rate is 41 SEU/day and 117 SEU/day, respectively.

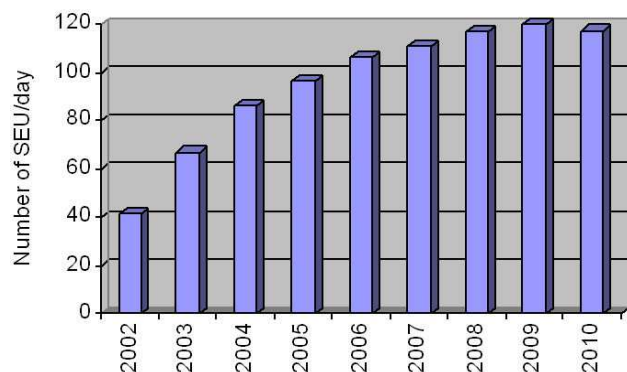


Fig. 1 Plot of the yearly average of the number of SEU/day versus time from November 2002 to August 2010

Table I summarizes the observations from the Alsat-1 main computer "OBC-386" 32 Mbytes Ramdisk. From these observations, the correct average SEU rate is 108.62 SEU/day in 8 memories of 4 Mbytes each. The mean SEU rate at Alsat-1's orbit is  $4.04 \times 10^{-7}$  SEU/bit/day, where 98.6% of these SEUs cause single-bit errors, 1.22% cause double-byte errors, and the remaining SEU result in multiple-bit and severe errors. Most of the Single-Byte Multiple-bit Upsets (SMU) are double-bit upsets. Double-byte errors are events which affect two bytes. Severe errors are due to single-event multiple-bit upsets affecting bits spread across more than two bytes. The severe (uncorrectable) error-rate of these memory devices is  $3.7 \times 10^{-10}$  severe error/bit/day when using the double-error correcting modified Reed-Solomon RS (256, 252) code.

TABLE I  
SEU OBSERVATIONS FOR ALSAT-1

| System monitored           | OBC 386 RAMDISK Memory                          |
|----------------------------|---|
| EDAC code                  | R-S (256, 252)                                  |
| Memory size                | 32 M-bytes                                      |
| Hybrid                     | SYS84000RKXLI-70 (4 M × 8-bit)                  |
| Device                     | Samsung SEC KM684000BLT-5L<br>512K × 8-BIT SRAM |
| Observation period         | 2622 days November 29 2002 – August 14 2010     |
| Bits monitored             | 268435456                                       |
| Total number of errors     | 265649  |
| No. of Single-bit errors   | 261905 (98.59%)                                 |
| No. of double-byte errors  | 3249 (1.223%)                                   |
| No. of severe errors       | 247 (0.093%)                                    |
| No. of Multiple-bit errors | 233 (0.087%)                                    |
| No. of Hardware errors     | 15 (0.005%)                                     |

Figs. 2, 3, 4 and 5 show the yearly average of the number of single-bit, double-byte, severe, and multiple-bit errors per day, respectively. From these figures it's clear that the majority of SEU cause single-bit upsets. Most of the severe errors occurred when Alsat-1 was located over the geo-magnetic poles where galactic cosmic rays are most able to penetrate to low altitudes.

The most significant events being those of 2009 which caused an average of 120 upsets per day in the Alsat-1 memory devices. These events caused a maximum number of single-bit, double-byte, and multiple bit errors during this year. However, a maximum number of severe errors has been registered in December 2002.

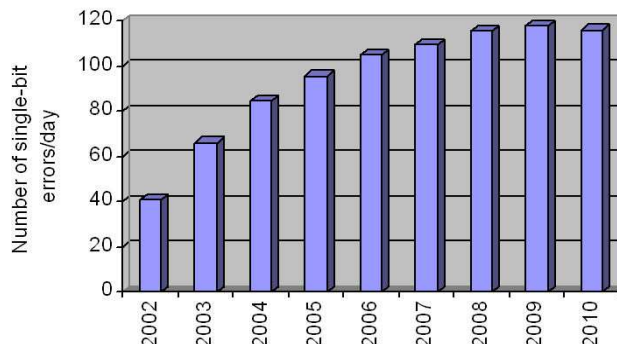


Fig. 2 Plot of the yearly average of the number of single-bit errors per day versus time from November 2002 to August 2010

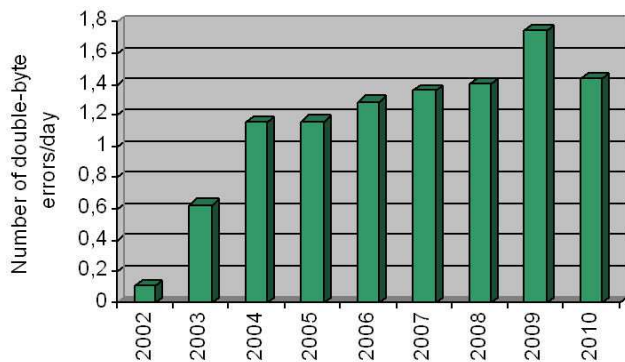


Fig. 3 Plot of the yearly average of the number of double byte errors per day versus time from November 2002 to August 2010

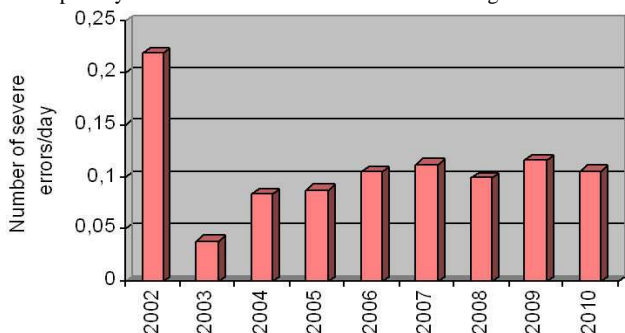


Fig. 4 Plot of the yearly average of the number of severe errors per day versus time from November 2002 to August 2010

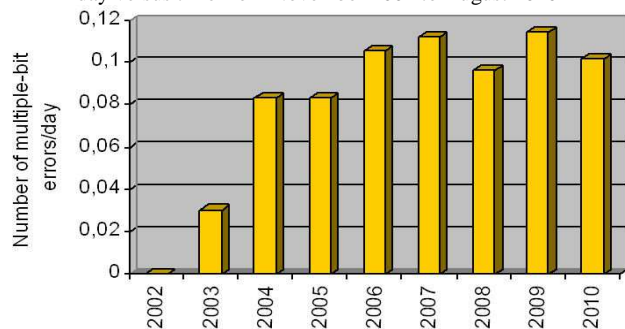


Fig. 5 Plot of the yearly average of the number of multiple-bit errors per day versus time from November 2002 to August 2010

It is clear that from these observations, severe errors defeated TMR-EDAC used to protect the program memories of the Alsat-1 OBC-386. It is recommended that the hybrid EDAC circuit be used to protect the memory and to correct all the errors encountered during the Alsat-1 life time [8].

#### IV. CONCLUSION

This paper has presented a review of an 8-year study on radiation effects in commercial memory devices operating within the main on-board computer system OBC386 of the Algerian microsatellite Alsat-1. In-orbit observations of single and multiple event upsets are presented for the period between November 2002 and August 2010. In this period of time the mean SEU rate at Alsat-1's orbit is  $4.04 \times 10^{-7}$  SEU/bit/day, where 98.6% of these SEU cause single-bit errors, 1.22% cause double-byte errors, and the remaining SEU result in multiple-

bit and severe errors. These will defeat the standard TMR used to protect these memories. It is recommended that the hybrid EDAC circuit be used to protect the memory [8].

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