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A Novel Low Power Very Low Voltage High Performance Current Mirror

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***Abstract*—**In this paper a novel high output impedance, low input impedance, wide bandwidth, very simple current mirror with input and output voltage requirements less than that of a simple current mirror is presented. These features are achieved with very simple structure avoiding extra large node impedances to ensure high bandwidth operation.

The circuit's principle of operation is discussed and compared to simple and low voltage cascode (LVC) current mirrors. Such outstanding features of this current mirror as high output impedance ~384K, low input impedance~6.4, wide bandwidth~178MHz, low input voltage ~ 362mV, low output voltage ~ 38mV and low current transfer error ~4% (all at 50μA) makes it an outstanding choice for high performance applications. Simulation results in BSIM 0.35μm CMOS technology with HSPICE are given in comparison with simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror.

***Keywords*—** Analog circuits, Current mirror, high frequency, Low power, Low voltage.

I. Introduction

Current mirror is one of the most essential building blocks in analog integrated circuits which its performance affects qualitive performance of the system. The major draw backs of conventional current mirrors due to technology scaling trend in VLSI design tend to be: voltage supply reduction requirement, input and output impedances degradation, and high frequency malfunctioning. Considering that in many applications, the performance of the traditional current mirrors are inadequate; In the past two decade, a series of high performance current mirrors has been reported [1]-[13]. Low power current mirrors using low supply voltages are attractive for all designers. Meanwhile, traditional current mirrors/sources, such as simple, cascode, and regulated current mirrors/sources [1], suffer from a trade-off between the output resistance and the compliance voltage (the minimum voltage required for the current mirror/source to operate). Some topologies such as the high swing cascode [2] and the active regulated cascode [3] have improved R_{out} with a relatively low compliance voltage of $2V_{DSsat}$. This, however, may still be too large to be tolerated in low voltage circuits. In [4]-[5] are presented current sources with high output resistance and compliance voltage of one V_{DSsat}. The circuit in [4] works based on sensing the voltage across the current source. Its draw backs are high frequency degradation and instability problems. The circuit in [5] uses positive feedback to increase its output impedance reduce its output compliance voltage. These circuits however are used as current sources and are not suitable as current mirrors. Although the circuits proposed in [6]-[8] eliminate some of the above mentioned draw backs, however they suffer from heavy structures and large chip area consumption. In order to further relaxing voltage requirements some techniques such as body driven topologies are introduced in literatures [9]-[11]. These circuits suffer from lower bandwidth, expensive technology and higher input impedance due to g_{mb} being lower than g_m. Another method for increase the linearity and decrease input voltage swing of current mirrors is to use self biasing structures, which offer reduction in voltage and power supply because of adaptive biasing [13], but they suffer from complexity, larger area. Self biasing improves the performance of current mirrors when the supply voltage is decreased.

In this work a high performance current mirror is presented in which favorably most of aforementioned characteristics are improved.

In section II the proposed current mirror is explained. Section III includes the results achieved from simulations. And finally Section IV concludes this paper.

II. Proposed High Performance Current Mirror

A. Principle of Operation

The proposed current mirror, which its schematic is shown in Fig. 1, is composed of M1 and M2 as mirror transistors, M3 and Mp1 as feedback transistors, M4 as shift transistor, and bias current of Ib. aspect ratio of M4 and I_b are adjusted to set V_{ds1} equal to V_{ds2} prohibiting the channel effect and attaining a high precision result. By using FVF structure [12] at input node low input voltage is achieved and at the same time containing a positive feedback loop of M1, M2, M3, M4, and Mp1 in the other side causes the input impedance to be extremely low and output impedance to be extremely high. In other words, transistors M2, M4, M3, and Mp1 create output positive feedback. Transistors M2, M4, M3, and M1 create input positive feedback. The above mentioned positive

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feedback in accompany with adaptively biased amplifier M3 in input node preserves low input voltage requirement and low input resistance capability.

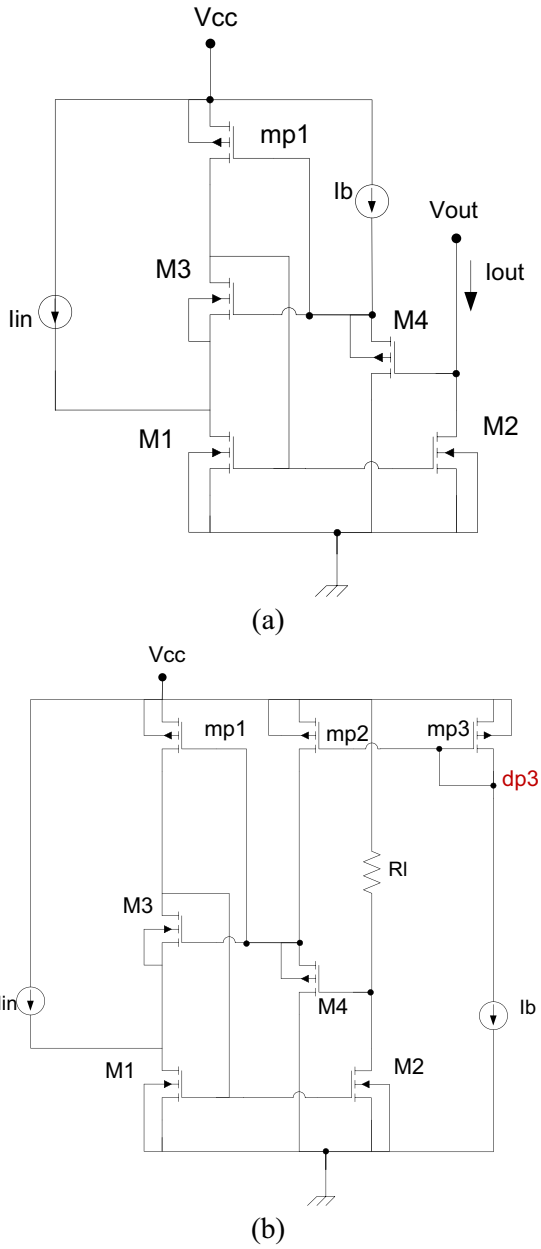

Fig .1 A schematic of the low-voltage current mirror (a) without (b) with bias transistors.

Since the loop gain can be controlled by aspect ratios of the transistors hence we can either have negative or positive impedance. This new configuration is capable to operate at output voltages smaller than that of simple current mirror by means of pos itive feedback in its output. Using Mp1 in the feedback loop helps circuit to keep its accuracy in extra low output voltages. When V_{out} approaches lower voltages, then current flowing through Mp1 is increased and this will increase the gate voltages of M1 and M2 and so this will increase the output current.

Biasing the gate of M3 and M4 with a voltage source provides two disadvantages. First, it needs an extra circuit to build this bias voltage. Second, setting the gate voltage of M3 and M4 at a fixed voltage causes output positive feedback to be removed. It also changes input positive feedback to the negative one limit us to achieve negative impedances so, input impedance will be higher and output impedance will be lower than those of the proposed scheme.

B. Circuit Analysis

The proposed current mirror is shown in Fig. 1. When the output voltage is increased the channel length modulation effect tends to increase the output current, but meanwhile transistors M3 and Mp1 reduce mirror transistors' gate voltage, reducing the M1 and M2 currents. By adjustment of the operating point and aspect ratio of transistors one can achieve very high output impedances even greater than low voltage cascade current mirror while output compliance no more than that of the simple current mirror is consumed. There is no restriction for transistors M3, M4 and Mp1 to work in saturation region, in fact they can work in saturation, triode, and even off regions. This is an interesting result; firstly because the voltages of circuit are not limited by addition of these transistors, secondly power consumption is not increased very much. For low voltage operation at input node, FVF structure is adopted [12]. This structure makes the circuit to operate at input voltages as low as possible for V_{Dsat}. It also reduces the input impedance and increases the output impedance.

1) Output impedance analysis

Considering small signal equivalent circuit we have:

$$v_{out} = r_{o2}(I_{out} - g_{m2}v_{d3}) \quad (1)$$

$$v_{d3} = -g_{m3}(r_{op1} \| \mu_3 r_{o1})(v_{out} - v_{d1}) \quad (2)$$

Where:

$$v_{d1} = -\frac{g_{m1}}{g_{m3}} v_{d3} \quad (3)$$

Substituting (3) into (2) we get:

$$v_{d3} = -g_{m3}(r_{op1} \| \mu_3 r_{o1})(v_{out} + \frac{g_{m1}}{g_{m3}} v_{d3}) \quad (4)$$

$$v_{d3} = \frac{-g_{m3}(r_{op1} \| \mu_3 r_{o1})}{1 + g_{m1}(r_{op1} \| \mu_3 r_{o1})} v_{out} \quad (5)$$

$$v_{d3} = -g_{m3}(r_{op1} \| \mu_3 r_{o1})(v_{out} + \frac{g_{m1}}{g_{m3}} v_{d3}) \quad (6)$$

$$v_{d3} = \frac{-g_{m3}(r_{op1} \| \mu_3 r_{o1})}{1 + g_{m1}(r_{op1} \| \mu_3 r_{o1})} v_{out} \quad (7)$$

Substituting (7) into (1) gives:

$$v_{out} = r_{o2}\left(I_{out} + \frac{g_{m2}g_{m3}(r_{op1}\|\mu_3 r_{o1})}{1+g_{m1}(r_{op1}\|\mu_3 r_{o1})}v_{out}\right) \quad (8)$$

$$v_{out} = \left[\frac{r_{o2}}{1-\frac{g_{m2}g_{m3}r_{o2}(r_{op1}\|\mu_3 r_{o1})}{1+g_{m1}(r_{op1}\|\mu_3 r_{o1})}}\right] I_{out} \quad (9)$$

$$R_{out} = \left[\frac{r_{o2}}{1-\frac{g_{m2}g_{m3}r_{o2}(r_{op1}\|\mu_3 r_{o1})}{1+g_{m1}(r_{op1}\|\mu_3 r_{o1})}}\right] \quad (10)$$

2) Input impedance analysis

$$I_{in} = -g_{m3}(v_{g3} - v_{in}) + g_{m1}v_{d3} \quad (11)$$

Where:

$$v_{d3} = -g_{m3}(r_{op1}||\mu_3 r_{o1})(v_{g3} - v_{in}) \quad (12)$$

$$v_{d3} = \frac{-v_{g3}}{g_{m2}(R_L\|r_{02})} \quad (13)$$

$$v_{g3} = \frac{g_{m3}(r_{op1}||\mu_3 r_{o1})v_{in}}{g_{m3}(r_{op1}||\mu_3 r_{o1}) - \frac{1}{g_{m2}(R_L\|r_{02})}} \quad (14)$$

By choosing g_{m1} equal to g_{m2} we have

$$I_{in} = g_{m3}v_{in} - \frac{(g_{m3}+\frac{1}{(R_L\|r_{02})})g_{m3}(r_{op1}||\mu_3 r_{o1})v_{in}}{g_{m3}(r_{op1}||\mu_3 r_{o1}) - \frac{1}{g_{m2}(R_L\|r_{02})}} \quad (15)$$

$$R_{in} = g_{m3} - \frac{(g_{m3}+\frac{1}{(R_L\|r_{02})})g_{m3}(r_{op1}||\mu_3 r_{o1})}{g_{m3}(r_{op1}||\mu_3 r_{o1}) - \frac{1}{g_{m2}(R_L\|r_{02})}} \quad (16)$$

III. Simulation Results

Hspice simulation of the proposed current mirror is carried out in a BSIM 0.35µm CMOS process. To investigate the performance improvement (especially, input and output impedance, input and output voltage swing, power and band width) of the proposed current mirror compared to simple and LVC current mirrors, their simulation results are compared. For a fair judgment the W/L of all investigated circuits is selected the same.

The comparative simulation results are given in Fig. 2 for simple, LVC and proposed circuits. In this figure I_{out} is shown in terms of V_{out} sweep. It can be seen that the proposed circuits offer higher output impedances and benefit from lower voltage operation capability. Also it can be seen that low voltage cascode exhibits more offset error and does not operate at low voltages. However, low voltage cascode provides higher output impedance compared to proposed current mirror. The proposed current mirror's well functionality as a low voltage and high resistance block especially at low current levels is comprehensively understood from the Fig.2.

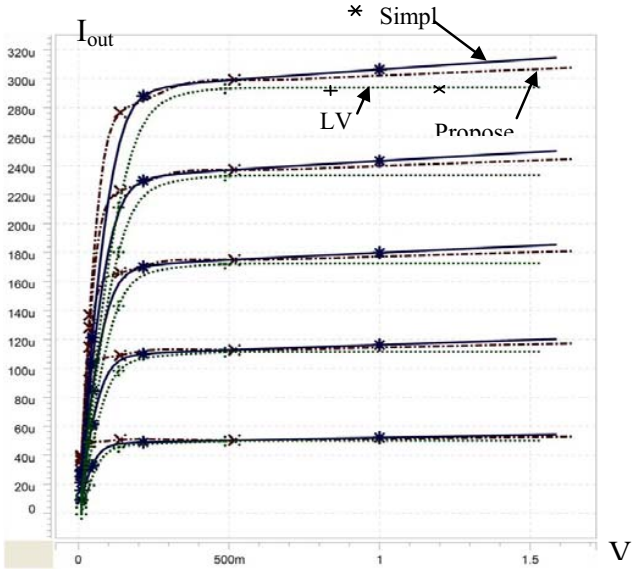

Fig. 2 comparative simulation results for simple, LVC and proposed circuits

Fig. 3 shows the output current dynamic range for simple, LVC and proposed circuits.

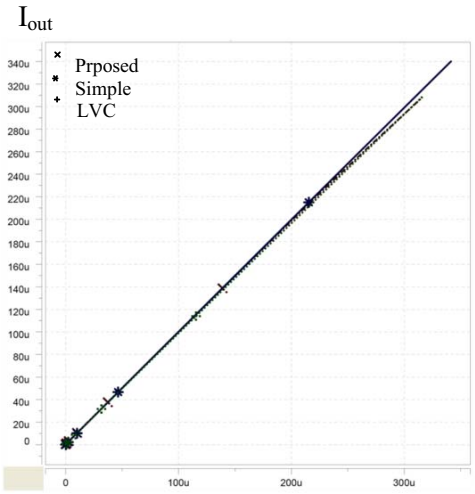

Fig. 3: output current dynamic range

Fig. 4 compares the input resistance of simple, LVC, and proposed current mirrors.

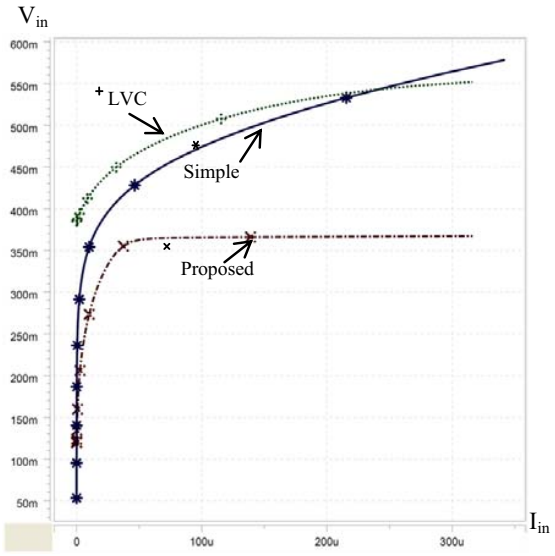

Fig. 4 The input resistance of simple, LVC, and proposed current mirrors.

Fig. 5 shows the band width of simple, LVC, and proposed current mirror. It is seen that the proposed current mirrors have the high band width of the simple current mirror.

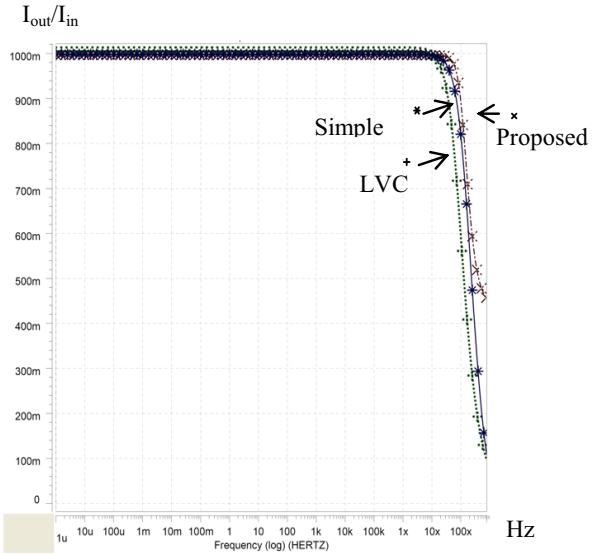

Fig. 5: Comparing band width of simple, LVC, and proposed current mirror

Comparative results of proposed current mirrors with some other works are presented at Table 1.

IV. Conclusion

In this work a high performance current mirror is presented with such favorable characteristics as: high output impedance~384K, low input impedance~6.4, wide bandwidth~178MHz, low input voltage ~ 362mV, low output voltage ~ 38mV and low current transfer error ~4% (all at 50μA). Its simulation results in BSIM 0.35μm CMOS technology with Hspice are given in comparison with those of simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror.

The proposed current mirror (CM) shows output impedance greater than traditional cascode current mirrors, while maintaining the output voltage requirement and high bandwidth of the simple current mirror. This circuit's bandwidth, input and output voltage requirements are comparable to those of the simple current mirror. The circuit can show a minimum output voltage even lower than that of the simple current mirror. The proposed current mirror is an outstanding choice for high frequency low power low voltage applications

TABLE I
COMPARISON RESULTS

Ref	Simple	LVC	[9]	[11]	Proposed circuit
I_{IN} (μA)	50	50	12	30	50
Offset (μA)	3	4	8.8	18	2
Vin(mV)	432	469	NA	300	362
Rin(Ω)	360	145	0.02	NA	6.4
Vout(mV)	232	376	1.4	200	38
Rout(MΩ)	0.27	19.23	360	NA	0.384
P(μW)	20	50	2300	NA	23
BW(MHz)	145	76	0.083	2	178
Supply (V)	1.5	1.5	1	1.5	1.5
Tech.	BSIM 0.35μm	BSIM 0.35μm	90nm	TSMC 0.25μm	BSIM 0.35μm

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