

A Novel Digital Calibration Technique for Gain and Offset Mismatch in $T\Sigma\Delta$ ADCs

Ali Beydoun, Van-Tam Nguyen and Patrick Loumeau
TELECOM ParisTech - LTCI-CNRS-UMR 5141

Abstract—Time interleaved sigma-delta ($T\Sigma\Delta$) architecture is a potential candidate for high bandwidth analog to digital converters (ADC) which remains a bottleneck for software and cognitive radio receivers. However, the performance of the $T\Sigma\Delta$ architecture is limited by the unavoidable gain and offset mismatches resulting from the manufacturing process. This paper presents a novel digital calibration method to compensate the gain and offset mismatch effect. The proposed method takes advantage of the reconstruction digital signal processing on each channel and requires only few logic components for implementation. The run time calibration is estimated to 10 and 15 clock cycles for offset cancellation and gain mismatch calibration respectively.

Keywords—sigma-delta, calibration, gain and offset mismatches, analog-to-digital conversion, time-interleaving.

I. INTRODUCTION

The trend in wireless communication where terminals give their users ubiquitous access to a multitude of services drives the development of software defined radio and cognitive radio. These concepts were proposed by Mitola in [1][2]. They consist in moving the digital processing as close as possible to the receiver antenna in order to ensure a software and smart management of the radio spectrum. This solution requires a wide-band and high-resolution Analog to Digital Converter (ADC) which remains the main bottleneck.

Many ADC topologies based on sigma-delta modulators and parallelism to widen the conversion bandwidth were proposed. The Time Interleaved Sigma-Delta ($T\Sigma\Delta$) converter (Fig. 1) [3], [4], [5], [6] provides high performance and has the lowest hardware complexity compared to Parallel Sigma-Delta ($\Pi\Sigma\Delta$) [7] and Frequency Band Decomposition (FBD) [8] architectures. For example, a 4 channel $T\Sigma\Delta$ converter using innovative sigma-delta modulator [9] with a suitable interpolation factor can provide a theoretical Signal to Noise plus Distortion Ratio (SNDR) of 102 dB. However, $T\Sigma\Delta$ converter is very sensitive to channel mismatch which drastically reduces the SNDR. In fact, analog imperfections in $\Sigma\Delta$ modulators are the main cause of this mismatch. Many factors can contribute to these analog imperfections : thermal noise associated with the switch resistances, parasitic capacitances, charge injection from MOS switches, offsets in operational amplifiers, amplifier finite gain, comparator gain and offset, mismatches among the passive elements, etc. These imperfections can be classified in two types :

- imperfections due to manufacturing process (eg: mismatches among the passive elements) which vary slowly in time,
- imperfections due to the frequency behavior of some analog components (eg: amplifier finite gain, comparator

gain) which depend on the bandwidth of the input signal.

Advanced mathematical models were developed to model the impact of all these imperfections on $T\Sigma\Delta$ ADC performance [10], [11], [12]. In practice, the frequency imperfection effects can be limited at the design stage of the $T\Sigma\Delta$ ADC taking into account the bandwidth of the input signal. For this reason, this paper deals only with imperfections due to manufacturing process whose effect can be illustrated using the simplest behavioral model presented in [3], [13]. In this model, the output of the k^{th} $\Sigma\Delta$ modulator will be amplified by $g_k = (1 + \varepsilon g_k)$ and added to an offset o_k (Fig. 1). In the analysis developed in this paper, the gain error εg_k and the offset error o_k are assumed to be time invariant, independent and identically distributed random variables, having a Gaussian probability density function with zero mean and variance σ_g^2 and σ_o^2 respectively.

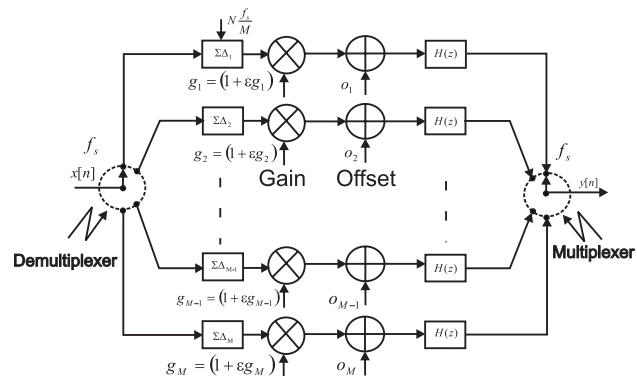


Fig. 1. $T\Sigma\Delta$ ADC architecture with gain g and offset o at the output of each modulator modelling the analog imperfections.

After a brief introduction of the $T\Sigma\Delta$ ADC with an overview of the calibration methods in the state of the art, section III presents the effect of offset mismatch and the proposed correction method. Section IV sheds light on the effect of the gain mismatch and the relevant calibration method. The implementation of the calibration algorithm is detailed in section V. Finally, section VI presents a conclusion about the performance of the proposed calibration method.

II. REVIEW OF THE $T\Sigma\Delta$ A/D CONVERTER

The block diagram of $T\Sigma\Delta$ ADC is presented in Fig. 1. An equivalent mathematical model based on multirate signal processing shown in Fig. 2 is used to evaluate its performance [3]. The $T\Sigma\Delta$ ADC is composed of M parallel low-pass

$\Sigma\Delta$ modulators. The input signal $x[n]$ is distributed among the M modulators through an analog multiplexer. Then, the signal rate, on each channel, is increased by a factor N using interpolation by zeros. Afterward, the output of each modulator is filtered by the digital filter $H(z)$ to suppress the out of band quantization noise. Finally, the signal is decimated by a factor N to reduce the data rate before being demultiplexed by a digital demultiplexer to reconstruct the output signal $y[n]$.

The theoretical Signal to Noise Ratio (SNR) of a $T\Sigma\Delta$ ADC depends on three parameters of the modulators : its order (P), the number of quantizer levels and the interpolation factor (N). The conversion bandwidth depends on the number of channels (M). The number of taps in digital filters (L) determines the hardware complexity needed to reach the expected SNDR.

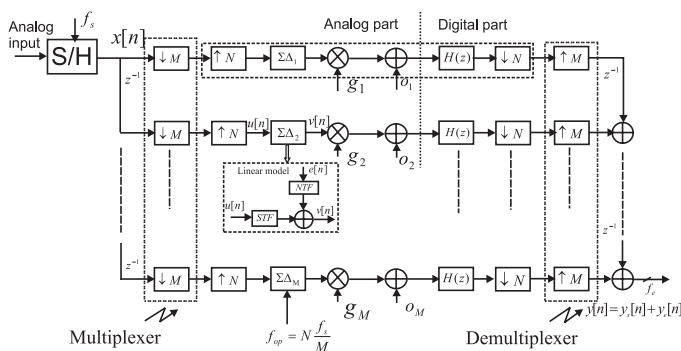


Fig. 2. Mathematical model of the $T\Sigma\Delta$ ADC architecture with M channels using multirate building blocks.

It has been shown in [14] that the digital filter ensuring high attenuation of the out of band quantization noise with the lowest hardware complexity is a Comb-filter whose order is the first even number higher than $P + 1$.

The major problem of the $T\Sigma\Delta$ converter is the mismatch among the $\Sigma\Delta$ modulators which then creates harmonic distortion in the digital output. Channel offset mismatch causes additive tones at integer multiples of the channel sampling rate $\frac{f_s}{M}$ and channel gain mismatch results in images of the useful signal spectrum appearing at intervals of $\frac{f_s}{M}$ [13]. Several solutions have been proposed in the literature to correct these errors. They can be classified into three approaches :

1) The first approach aims to compensate the gain and the offset of each channel. First, it consists in estimating the gain and the offset of the modulator in each channel. Then, the output of the modulator is multiplied by the inverse of the estimated gain and subtracted from the estimated offset. Several methods have been proposed for gain and offset estimations.

- The first method uses a digital sigma-delta modulator after the analog modulator to estimate and compensate gain and offset [15]. This method increases the area and the power consumption considerably even if it allows an online calibration.
- The second method proposed in [16] offers an online digital estimation and compensation of the

offset. In this method, the input of the modulator is multiplied by a pseudo-random sequence $\{\pm 1\}$ to whiten its spectrum. Then, the offset in each channel is estimated, using the linear least squares algorithm, and subtracted from the modulator's output before being multiplied again by a delayed version of the same pseudo-random sequence to reconstruct the useful signal. The multiplication of the input signal by the sequence $\{\pm 1\}$ increases the implementation constraints of the first stage of the $\Sigma\Delta$ modulator and the noise floor which will significantly degrade the expected resolution especially with a low order $\Sigma\Delta$ modulator. Moreover, a perfect reconstruction of the useful signal is not sure if the Signal Transfer Function (STF) of the modulator is not a pure delay.

- The third method aims to estimate and correct the gain error at the output of the modulator [5]. It uses an appropriate reference signal at the input with the Least Mean Square algorithm (LMS) [17] known for its implementation simplicity. However, this method requires knowledge of the ideal output of the $T\Sigma\Delta$ ADC to the reference signal, which is impossible because of the chaotic behavior of the $\Sigma\Delta$ modulator.

2) As spurious tones are introduced by gain and offset mismatches between $\Sigma\Delta$ modulators, the second approach aims to equalize gain and offset of all modulators. The first method based on this approach [18] uses an extra $\Sigma\Delta$ modulator as a reference modulator. Each modulator of the $T\Sigma\Delta$ ADC architecture is connected successively in parallel with the reference modulator in order to estimate, in the digital domain, the appropriate gain and offset to be introduced to ensure the same gain and offset as the reference modulator. Once the calibration cycle is finished, another modulator is placed on the calibration phase. Despite this method ensuring online calibration, the equalization of the offset is strongly affected by the modulator's gain. Moreover this method considerably increases the silicon die area by adding an extra modulator and appropriate digital processing for gain and offset estimations.

To eliminate the need for an extra modulator, another method was proposed in [19], using a 1-bit Digital to Analog Converter (DAC) and a pseudo-random generator, to achieve a complete gain matching between modulators. This calibration method has two drawbacks : first the output of the DAC must be fed back to the input of the modulator which increases the implementation constraints; second the offsets are not equalized.

3) The presence of spurious tones is due to the periodic selection of the channels by the multiplexer at the output to reconstruct the useful signal. The third approach uses randomization of the channel selection to spread out the spurious tones energy over the whole bandwidth. A randomization technique was proposed in [21] using an extra channel. Whereas this approach ensures online calibration, it increases the die area and the noise floor

leading to a decrease of the SNDR.

In order to overcome the drawbacks of the calibration methods mentioned above, this paper presents an innovative digital calibration method based on a mix of the first two approaches [22]. This new method [20] consists in :

- Estimating the offset value on each channel and then subtracting it from the useful signal. This approach is chosen because even if all the offsets resulting from manufacturing process are equal, the offset value will be added to the useful signal at the output of the $TIS\Delta$ ADC and it will be difficult to distinguish it from the offset value in the useful signal leading to a significant decrease of the SNDR.
- Equalizing the gain of $\Sigma\Delta$ modulators to the gain of one of them used as a reference modulator. This suppresses spurious tones without any additional modulator.

The major benefits of our method lie in the following factors:

- No additional modulator is needed,
- No reference signal generator is needed,
- Only an accumulator on each channel in addition to the existing digital resources in the $TIS\Delta$ architecture is required,
- High accuracy for offset and gain estimation with very short convergence time is achieved.

To illustrate the influence of these errors and show the efficiency of the proposed correction method, a basic example is considered throughout this paper without any loss of generality. In this example, a 4 channel $TIS\Delta$ ADC is used with an interpolation factor of 80. A fourth order $\Sigma\Delta$ modulator is employed and the digital filter is a 6th order Comb-filter [14]. The input signal is a sinusoidal signal with a normalized amplitude of 0.6 located at the normalized frequency 0.02. The Power Spectral Density (PSD) at the output is presented in Fig. 3. The SNDR without any channel mismatch is estimated to 102 dB.

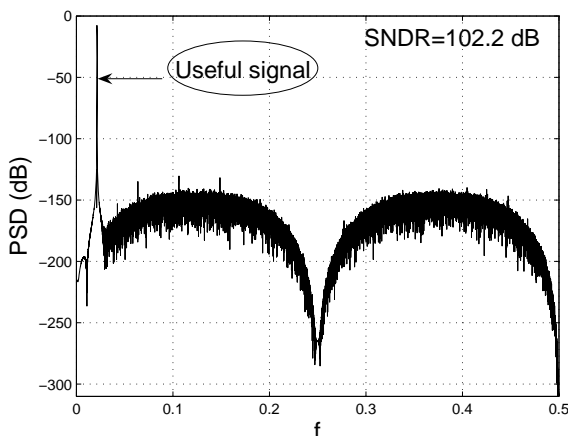


Fig. 3. PSD of the output signal with 4 channels $TIS\Delta$ ADC architecture.

III. OFFSET MISMATCH AND DIGITAL OFFSET CANCELLATION

Due to the time multiplexer at the output of the $TIS\Delta$ ADC, the presence of the offset o_i on each channel adds a periodic signal to the useful signal of period M (Fig. 4) whose Fourier transform is given by :

$$O(e^{jw}) = \sum_{l=-\infty}^{l=+\infty} 2\pi O_l \delta\left(w - \frac{2\pi}{M}\right) \quad (1)$$

where $\delta(\cdot)$ is the Dirac function and O_l is the l^{th} coefficient of the discrete Fourier series of the output:

$$O_l = \frac{1}{M} \sum_{k=0}^{M-1} o_k \left(e^{-\frac{j2\pi}{M}}\right)^{lk} \quad (2)$$

Consequently, this periodic signal causes additive tones at integer multiples of the channel sampling rate $\frac{f_s}{M}$ on the spectrum at the output of the $TIS\Delta$ ADC leading to a degradation of the SNDR. Moreover, even if all offsets are equal, spurious tone at zero frequency is still present which leads to a reduction of the SNDR. It is therefore essential to remove the offset on each channel.

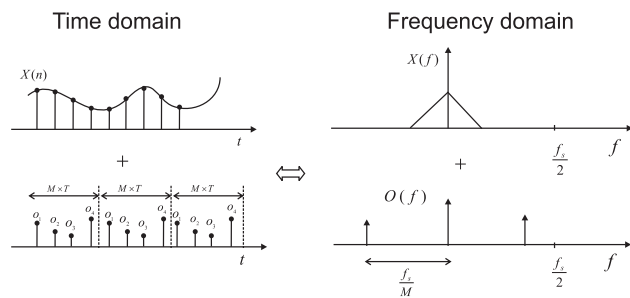


Fig. 4. Offset mismatch effect in time and frequency domain.

Fig. 5 shows the PSD at the output while considering an offset mismatch with standard deviation $\sigma_o = 2 \times 10^{-6}$. The SNDR drops to 72 dB. To determine the order of the offset values which maintains the expected SNDR, Fig. 6 presents the impact of the standard deviation σ_o on the SNDR. It can be noticed that very small offset values ($\sigma_o = 5 \times 10^{-7}$) severely degrade the SNDR explaining the high sensitivity of the $TIS\Delta$ ADC to offset mismatch.

Compensation of the offset requires first the estimation of its value and then the subtraction of the estimated value from the output signal of each modulator. Regarding the estimation phase, it is essential to know the required accuracy for the estimated value. For this purpose, Fig. 7 shows the SNDR at the output while subtracting the offset o value with a relative error $\varepsilon : (o \times (1 + \varepsilon))$.

It can be noticed that the SNDR evolves linearly with respect to the precision before reaching saturation until the spurious tone amplitude decreases to reach the quantization noise level. According to this result, there is a linear relationship between the required accuracy for the estimated value and the expected SNDR. It is given by :

$$estimation_precision = 10^{-k} = 10^{-\left(\frac{SNDR+35}{20}\right)} \quad (3)$$

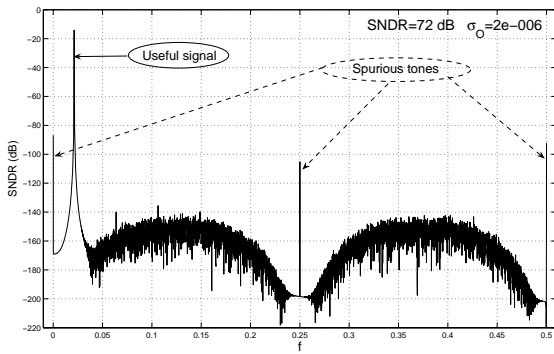


Fig. 5. PSD at the output with offset mismatch.

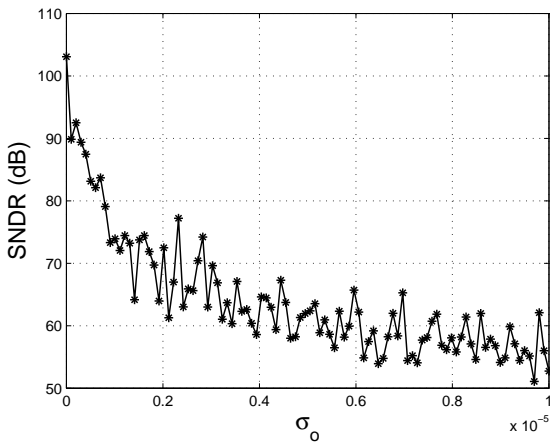


Fig. 6. SNDR at the output compared to the standard deviation σ_o .

As a result, a high theoretical SNDR (high interpolation rate) requires more accuracy for the estimation of the offset values. For the example considered in this paper, the required accuracy to achieve the expected SNDR is 10^{-7} .

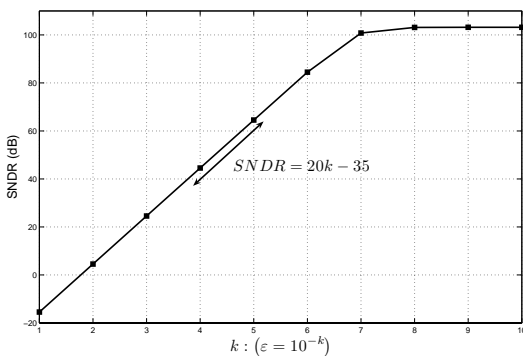


Fig. 7. SNDR compared to the accuracy for the estimated value of the offset.

Intuitively, the estimation of the offset value could be performed by calculating the average of the output signal of

the modulator when its input is connected to the ground. In fact, relying on the linear model of the quantizer inside the modulator, the modulator output, taking into account gain and offset errors, is given by :

$$Y(z) = (STF(z)X(z) + NTF(z)E(z)) \times g + o \quad (4)$$

where:

$X(z)$: the z transform of the input signal,

$STF(z)$: the Signal Transfer Function,

$E(z)$: the z transform of the quantization noise,

$NTF(z)$: the Noise Transfer Function.

When the input of the modulator is connected to the ground, the output signal will be :

$$y[n] = (Z^{-1} \{NTF(z)\} * e[n]) \times g + o \quad (5)$$

The output signal is then composed of the offset value plus the quantization noise shaped by the modulator and multiplied by the gain g . In this case, the estimation of the offset value could be performed using the classical linear least squares algorithm given by :

$$\hat{o} = \frac{1}{N_s} \sum_{i=0}^{N_s-1} y[i] \quad (6)$$

where N_s is the number of samples. The variance of the estimated value is given by:

$$\sigma_{\hat{o}}^2 = \frac{\sigma_y^2}{N_s} \quad (7)$$

The variance of the output signal σ_y^2 is very high due to noise shaping. Therefore, a large number of samples N_s is required to decrease $\sigma_{\hat{o}}^2$ and consequently achieve the desired accuracy of 10^{-7} . It was verified by simulation that with 2^{18} samples the maximal achievable accuracy is 5×10^{-6} . Hence, this method requires huge computing resources and a high run time estimation.

To improve the accuracy for the estimated value of the offset, it is necessary to reduce the noise power at the output of the $\Sigma\Delta$ modulator. For this purpose, the Comb-filter in each channel, dedicated to the reconstruction of the digital signal at the output, is used. Indeed, the Comb-filter has a very small bandwidth and a high out of band attenuation for a high interpolation factor ($N = 80$) (Fig. 9). Therefore, a good estimation of the offset value is obtained at the output of the Comb-filter, due to its very small bandwidth, when the input of the modulator is connected to the ground (Fig. 8).

To illustrate the efficiency of the Comb-filter, Fig. 10 presents the estimation error defined as the difference between the true offset value and the estimated one at the output of the Comb-filter. It can be noticed that the desired accuracy 10^{-7} for the estimated value is reached after 10 clock cycles ($(M \times N)/f_s$). To further improve the accuracy, it is possible to use the linear least squares algorithm (equation 6) at the output of the Comb-filter.

In order to validate this method, Monte-Carlo simulations with 500 shots have been performed with two normalized standard deviations 0.002 and 0.2 respectively. Fig. 11 shows the maximum estimation error for all channels at each shot. According to these results, the estimation of the offset with the

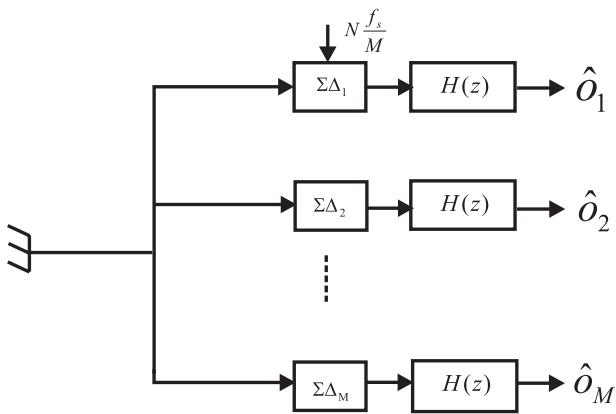


Fig. 8. Block diagram of the offset estimation method.

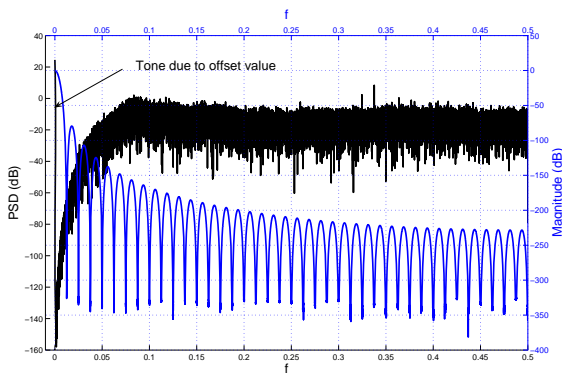


Fig. 9. PSD at the output of the $\Sigma\Delta$ modulator and frequency response of the Comb-filter.

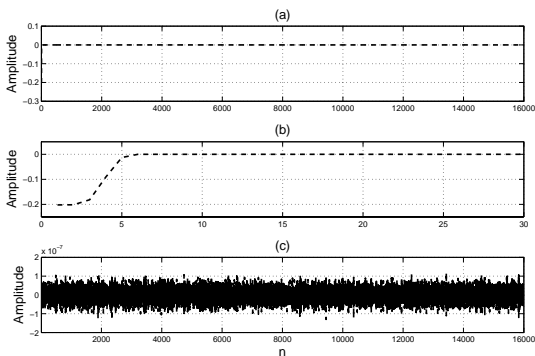


Fig. 10. Estimation error a), zoom in the interval time $0 \leq n \leq 30$ b), zoom from the 10th sample c).

Comb-filter is good enough to achieve the desired accuracy. It can be also noticed that the estimation error does not depend on the value of offset, but rather on the frequency response of the Comb-filter.

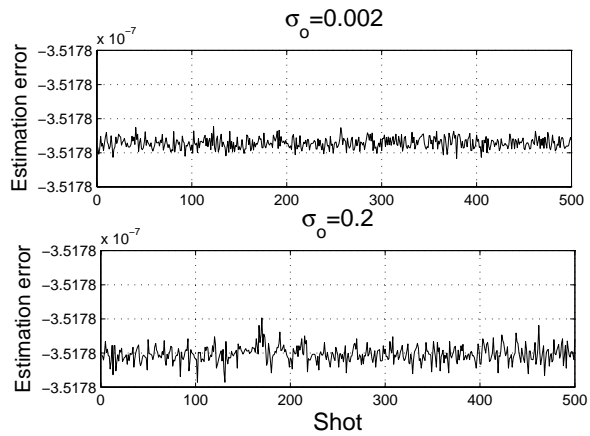


Fig. 11. The maximum of the estimation error at each shot of the Monte-Carlo simulation.

Fig. 12 shows the PSD of the output signal before and after the correction of the offset on each channel. The compensation of the offset decreases the amplitude of spurious tones to the level of quantization noise. As a consequence, the SNDR is improved by approximately 60 dB compared to the case without correction, up to 2 dB of difference with the ideal SNDR value.

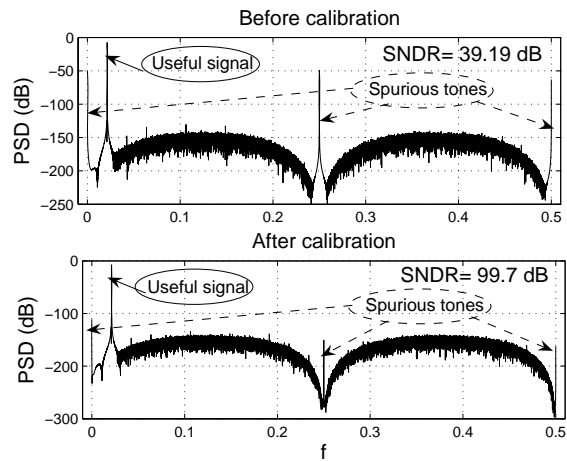


Fig. 12. The PSD at the output before and after the calibration of the offset mismatch.

IV. GAIN MISMATCH AND DIGITAL CALIBRATION

The multiplication of the output signal of each channel by a gain g_i is equivalent, due to the digital multiplexer at the output, to multiplying the useful signal at the output of the $T\Sigma\Delta$ ADC by a periodic signal of period M formed by the different gains g_i (Fig. 13). This multiplication results in

a convolution between the spectrum of the useful signal and the spectrum of the periodic signal. The latter spectrum is composed of tones located at frequencies $k \frac{f_s}{M}$ (k an integer) whose magnitude is given by the discrete Fourier series of the periodic signal. This convolution produces images of the spectrum of the useful signal weighted by the tone magnitudes.

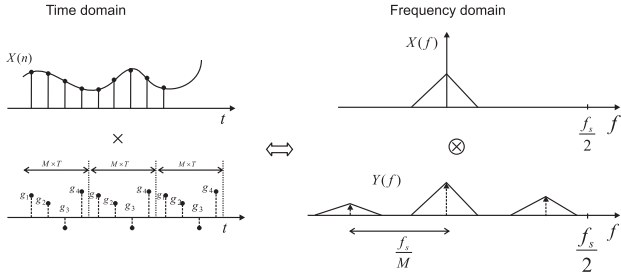


Fig. 13. Gain mismatch effect on the $TMS\Delta$ ADC architecture in time and frequency domain.

The gain mismatch effect could be supported by theoretical calculation using the mathematical model of the $TMS\Delta$ ADC presented in Fig. 2. With this mathematical model, the output of the $TMS\Delta$ ADC while just taking into account gain mismatch is [13]:

$$Y(z) = z^{-(M-1)}X(z) + z^{-(M-1)}G_0X(z) + z^{-(M-1)}L(z) \quad (8)$$

where

$$L(z) = \sum_{l=1}^{M-1} X(zW_M^{-l})G_l; \quad W_M = e^{-\frac{j2\pi}{M}} \quad (9)$$

and

$$G_l = \frac{1}{M} \sum_{k=0}^{M-1} g_k W_M^{lk} \quad (10)$$

The first term in equation (8) is a delayed version of the useful signal. The second term is the spectrum image resulting from the convolution of the useful signal spectrum with the tones of the periodic signal located at zero frequency whose magnitude is equal to G_0 which is the mean value of all channel gains g_k . This error does not harm the expected performance as it adds a constant bias to the output. The third term represents spectrum images resulting from the convolution of the useful signal spectrum with the other tones of the periodic signal with magnitude G_l . It was shown in [13] that the mean and variance of the spectrum image magnitudes are :

$$\mu_r = \frac{\sigma_g}{2} \sqrt{\frac{\pi}{M}} \quad \text{and} \quad \sigma_r^2 = \left(1 - \frac{\pi}{4}\right) \frac{\sigma_g^2}{M} \quad (11)$$

Note that the number of aliasing components increases with the number of channel M , but both the mean and the variance of the image magnitudes decrease according to equation (11) in such a way that the total energy provided by the gain mismatch remains constant.

Fig. 14 shows the PSD at the output of the $TMS\Delta$ ADC with 1% channel gain mismatch. It can be noticed that the SNDR is decreased by 60 dB. It is therefore mandatory to calibrate gain mismatch to maintain the expected performance.

It is interesting to note that the impact of gain and offset mismatches on the overall performance depend on the theoretical performance. Indeed, the higher the SNDR is, ie. the lower the quantization noise level is, the higher the $TMS\Delta$ ADC sensitivity to channel mismatch. In other words, when the noise level is very low, the slightest channel mismatch will cause spurious tones above the quantization level and seriously degrade the SNDR. In other cases, the spurious tones level will be below the quantization noise level and they do not affect the SNDR considerably.

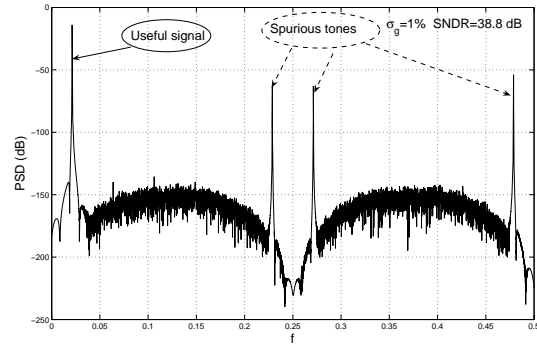


Fig. 14. PSD at the output of the $TMS\Delta$ with 1% of gain mismatches.

Fig. 15 presents the SNDR with respect to the standard deviation σ_g . It can be shown that the gain mismatch among channels must be less than 10^{-5} to avoid a high drop in of the SNDR. Therefore, the $TMS\Delta$ ADC is very sensitive to gain

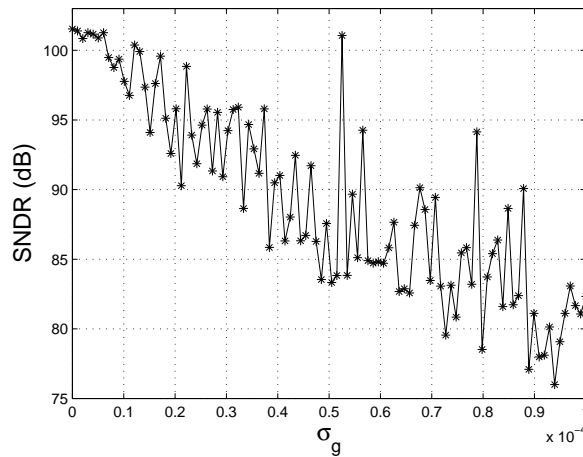


Fig. 15. SNDR at the output of the $TMS\Delta$ ADC with respect to the standard deviation σ_g .

mismatch and a calibration method is necessary.

The gain calibration method proposed in this paper supposes that the correction of the offset on each channel was already performed and then aims to equalize the gain on all channels to the gain of one of them considered as the reference channel. The block diagram of this method is depicted in Fig. 16 where the first channel is considered as the reference channel.

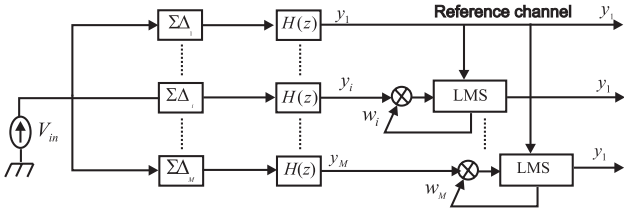


Fig. 16. Block diagram of the gain equalization method.

The different steps of this method are :

- The input signal is a constant signal applied to all modulators simultaneously. The magnitude of this signal V_{in} is fixed, without any loss of generality, to $\frac{V_R}{2}$ where V_R is the reference voltage. Any other values in the input dynamic range of the $\Sigma\Delta$ modulator can be used.
- The output signal of the i^{th} modulator is composed of the constant input signal V_{in} multiplied by the gain g_i and the quantization noise shaped by the modulator. The Comb-filter $H(z)$ extracts the useful signal value $V_{in} \times g_i$ on each channel with the same accuracy for offset estimation (section III).
- The Least Mean Square (LMS) algorithm calculates the weight value w_i to equalize the gain of the i^{th} channel to that of the reference channel (channel 1 in Fig. 16) :

$$g_i \times w_i = g_1 |_{i=2..M} \quad (12)$$

The LMS algorithm and its varieties (SD-LMS Sign-Data LMS, SE-LMS Sign-Error LMS, SS-LMS Sign data Sign Error LMS) have been chosen for their implementation simplicity compared to other estimation algorithms. The estimation of w_i using these algorithms is given by :
LMS :

$$\hat{w}_i[n+1] = \hat{w}_i[n] + \mu (y_1[n] - y_i[n]) \times y_i[n] \quad (13)$$

SD-LMS:

$$\hat{w}_i[n+1] = \hat{w}_i[n] + \mu (y_1[n] - y_i[n]) \times \text{sgn}[y_i[n]] \quad (14)$$

SE-LMS:

$$\hat{w}_i[n+1] = \hat{w}_i[n] + \mu \text{sgn}[(y_1[n] - y_i[n])] \times y_i[n] \quad (15)$$

SS-LMS:

$$\hat{w}_i[n+1] = \hat{w}_i[n] + \mu \text{sgn}[(y_1[n] - y_i[n])] \times \text{sgn}[y_i[n]] \quad (16)$$

where μ is the step of the algorithm.

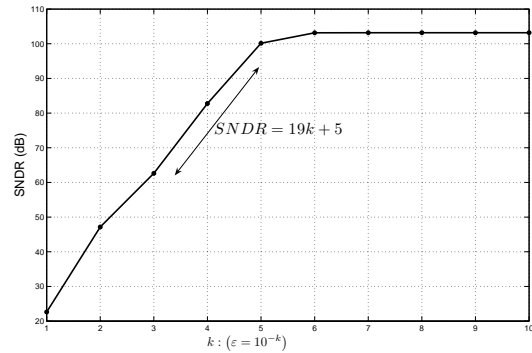
These four types of LMS algorithms are compared in terms of convergence time and accuracy for the estimated values. In the following, only simulation results with the SD-LMS algorithm will be detailed. The performance of these algorithms will be summarized in Table I at the end of this paper.

To evaluate the performance of this method, simulations have been performed using the basic example described in section II where the following gains [1.0113, 1.0146, 1.0029, 0.9884] are introduced on all channels.

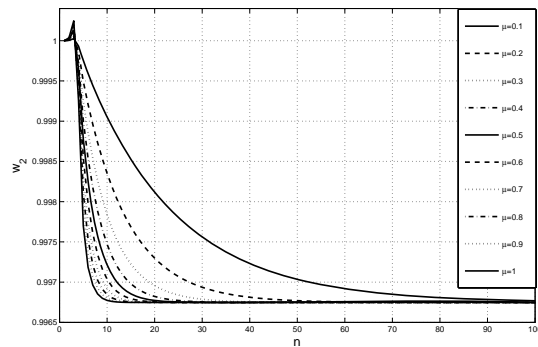
Before evaluating the performance of the LMS algorithm, it is important to know the required accuracy for the weight values w_i to ensure a good calibration of the gain mismatch. Fig. 17 presents the SNDR after the gain calibration with respect to the relative error ε introduced on the theoretical value of the weights $w_i : (w_i \times (1 + \varepsilon))$. It can be noticed that, with the same reasoning as for the offset estimation values, there is a linear relationship between the required accuracy for the weight values and the SNDR. It is given by :

$$\text{Weight_precision} = 10^{-k} = 10^{-\left(\frac{\text{SNDR}-5}{19}\right)} \quad (17)$$

It can be noticed that an accuracy of 10^{-6} for the estimated weights is required to regain the expected SNDR (102 dB).


 Fig. 17. SNDR at the output of the $T\Sigma\Delta$ ADC with respect to the relative error ε on the weight values.

The step of the LMS algorithm μ controls the convergence time and the accuracy for the estimated weights. Fig. 18 shows the estimated weight w_2 at each iteration n using the SD-LMS algorithm for different values of μ and Fig. 19 shows the maximum estimation error once the convergence is achieved with respect to μ . It can be noticed that the value $\mu = 1$ ensures the shortest convergence time with the best accuracy (5×10^{-7} compared to the desired accuracy 10^{-6}). Moreover, this value simplifies the implementation of this algorithm by removing the multiplication operation.


 Fig. 18. Estimation of the weight w_2 with the SD-LMS algorithm for different values of μ .

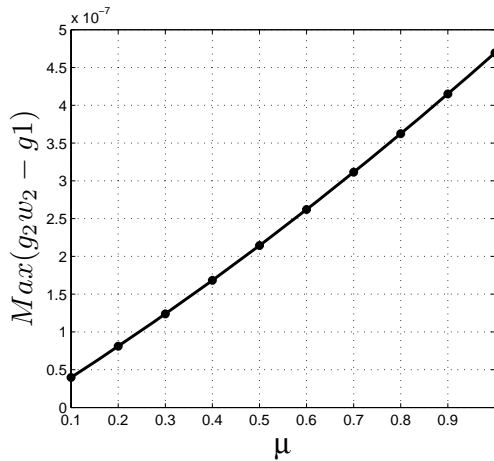


Fig. 19. Maximum estimation error of the weight w_2 with respect to μ .

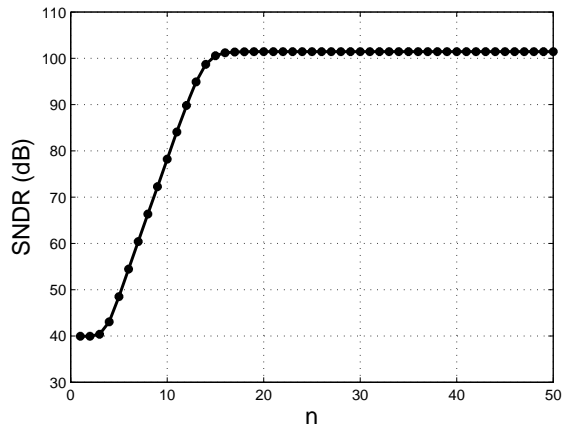


Fig. 21. SNDR at the output after each iteration of the estimation algorithm SD-LMS.

Fig. 20 shows the estimated weights with the SD-LMS algorithm with the step $\mu = 1$. In these conditions, the convergence of the algorithm to the desired weight values is reached after 10 clock cycles. To prove how accuracy is achieved, Fig. 21 shows the SNDR at each iteration of the algorithm. Therefore, the convergence of the algorithm to the desired weight with the required accuracy is reached after 15 clock cycles.

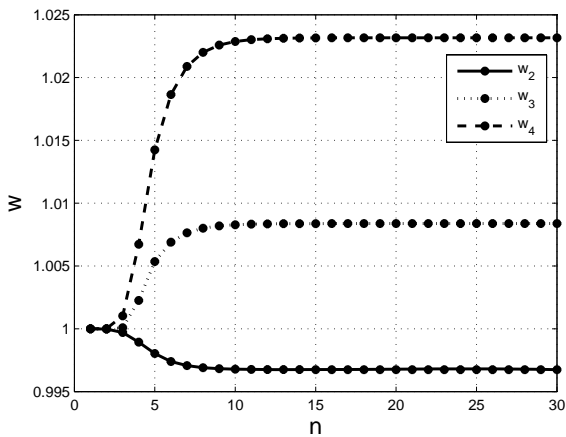


Fig. 20. The estimation of the weights using SD-LMS algorithm with $\mu = 1$.

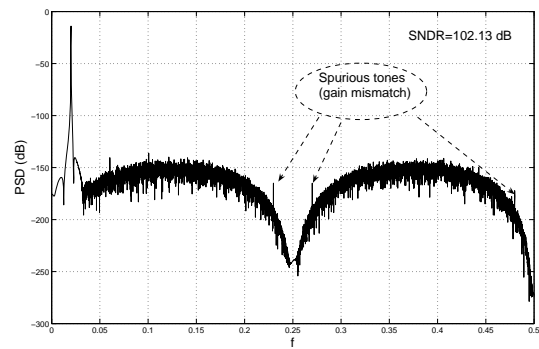


Fig. 22. PSD at the output after applying the calibration algorithm for gain mismatches.

Fig. 22 shows the PSD at the output after applying the calibration algorithm for 15 clock cycles. As a result, there is a decrease of the amplitude of spurious tones to the level of quantization noise thus regaining the expected SNDR of 102 dB.

In order to consider a real example, gain and offset are considered simultaneously in the basic example with values given by the following vectors :

$$O = [-0.202, 0.717, 0.765, 0.1832] \times 10^{-4}$$

and

$$g = [1.0113, 1.0146, 1.0029, 0.9884]$$

. The offset cancellation is applied first and then the gain equalization algorithm is applied taking into account the residual offset mismatch remaining after the offset cancellation. Fig. 23 shows the PSD at the output before and after calibration. It can be noticed that the gain equalization algorithm regains the expected performance even in the presence of weak offset mismatch. The total run time calibration is 25 clock cycles.

V. IMPLEMENTATION OF THE LMS ALGORITHM

The implementation of the calibration algorithm requires a Comb-filter on each channel plus an accumulator to run the LMS algorithm. The Comb-filter exists already in the $TFS\Delta$ ADC for the reconstruction of the useful signal at the digital output. It was designed and synthesized in a 1.2 V 65 nm CMOS process to work with the maximum clock rate of 208 MHz [14]. The total die area of the four Comb-filters was estimated to 0.048 mm².

As for the implementation of the LMS algorithm, it needs to determine the optimal accumulator length Nbw in which

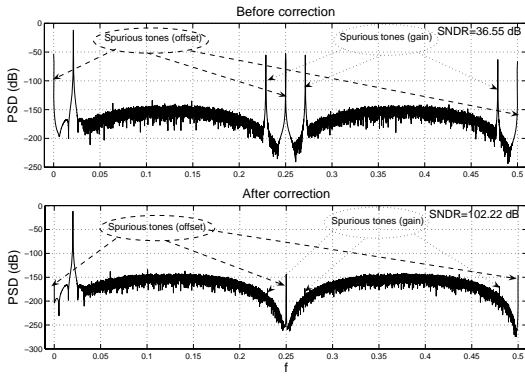


Fig. 23. PSD at the $TIS\Delta$ output before and after correction in the presence of gain and offset mismatch simultaneously.

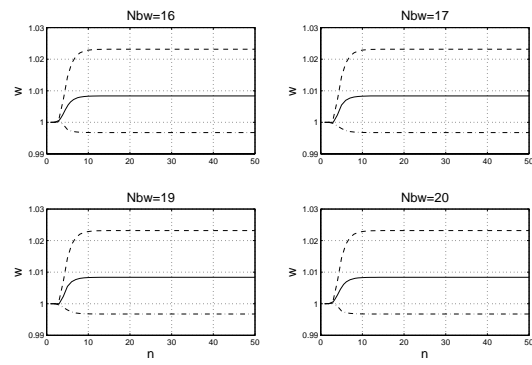


Fig. 24. Estimation of the weights w with the quantized SD-LMS algorithm for different values of Nbw .

the weight values will be quantized. For this purpose and in order to find the optimal value of Nbw to optimize die area and material resources, a quantized version of the LMS algorithm was considered. The quantized version is given by :

$$\hat{w}_{qi}[n+1] = \langle \hat{w}_{qi}[n] + \mu (\langle y_1[n] \rangle_{Nbr} - \langle y_i[n] \rangle_{Nbr}) \times \langle y_i[n] \rangle_{Nbr} \rangle_{Nbi} \quad (18)$$

where the operator $\langle A \rangle_{Nb}$ represents the quantization of the value A in Nb bits and is given by :

$$A_q = \frac{[A \times 2^{Nb}]}{2^{Nb}} \quad (19)$$

The register length of the output of the Comb-filter Nbr was fixed to 25 bits after optimizing the Comb-filter architecture with the interpolation factor $N = 80$ [14], [23].

To illustrate the effect of the accumulator length, Fig. 24 shows the weights estimation with the SD-LMS algorithm with different values of Nbw . It can be noticed that the quantization of the weights w does not affect the convergence time of the algorithm. However, it affects the accuracy of the algorithm. Fig. 25 presents the PSD at the output after applying the gain equalization algorithm with different word-length Nbw . It can be noticed that the higher the number of bits Nbw is, the smaller the magnitude of the spurious tones and the better the obtained SNDR. According to these simulation results, a quantization of the weight values on 19 bits is enough to ensure good performance.

Table I summarizes the optimal parameters and the computing resources for the four types of the LMS algorithm. The SE-LMS and SS-LMS present the easiest implementation

TABLE I
OPTIMAL PARAMETERS AND COMPUTING RESSOURCES FOR ALL TYPES OF THE LMS ALGORITHM.

Algorithm	μ	Multiplications	Additions	Convergence time	Nbw
LMS	1	1	2	$C_t = 35 \frac{N}{f_{op}}$	20
SD-LMS	1	0	2	$C_t = 15 \frac{N}{f_{op}}$	19
SE-LMS	$\frac{1}{2^{16}}$	1(shift)	2	$C_t = 780 \frac{N}{f_{op}}$	17
SS-LMS	$\frac{1}{2^{16}}$	0	2	$C_t = 1550 \frac{N}{f_{op}}$	17

and the least hardware complexity. However, they present the largest convergence time. The SD-LMS is the best compromise

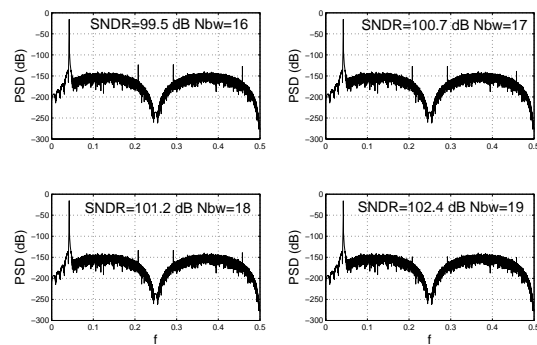


Fig. 25. PSD at the $TIS\Delta$ output after gain calibration for different values of Nbw .

with a very short convergence time without any multiplication which decreases the implementation complexity.

To perform the implementation of the LMS algorithm, it remains to define the criterion when the algorithm will stop running. Theoretically, the LMS algorithm must stop when the difference between the estimated value of the weight $\hat{w}_i[n+1]$ and the theoretical value w_i^{th} falls below the required accuracy $Weight_precision$ (equation 17). However, in practice the theoretical value w_i^{th} is unknown. To resolve this problem, the criterion proposed here consist stopping the LMS algorithm when the difference between two successive estimation values ($\hat{w}[n+1] - \hat{w}[n]$) is less than the desired accuracy. This criterion is equivalent to filter the estimated value $\hat{w}_i[n+1]$ by a filter with a transfer function of $(1 - z^{-1})$. Therefore, the first output of the filter must be dropped due to the filter delay. Fig. 26 shows the convergence time N^{th} and N^{diff} of the SD-LMS algorithm obtained with the theoretical and the proposed criterions respectively from a Monte-Carlo simulation with 300 shots while considering 1% of gain mismatch.

Note that the mean convergence time is about 15 clock cycles and it is the same with the two criterions. In practice, the evolution of the estimated values $\hat{w}_i[n+1]$ may be not monotonic before reaching the theoretical value but it may have some stationarity zones that can stop the execution of

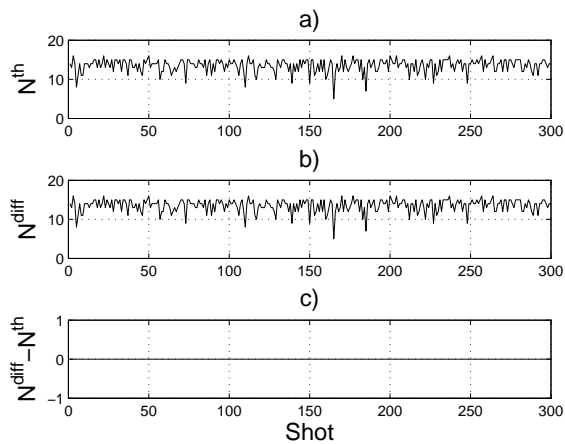


Fig. 26. Convergence time : a) with the theoretical criterion, b) with the criterion of the difference ($\hat{w}[n+1] - \hat{w}[n]$). c) the difference between the two convergence times.

the LMS algorithm before reaching the convergence to the theoretical value.

To avoid this problem, a high order transfer function filter ($1 - z^{-Lf}$) can be used where Lf is the filter order. Fig. 27 shows the convergence time with a 3rd order filter ($Lf = 3$). It can be noticed that the convergence time N^{diff} is always higher than the theoretical one N^{th} with a maximum difference of Lf clock cycles. In this case, a stationary zone with Lf clock cycles can be avoided.

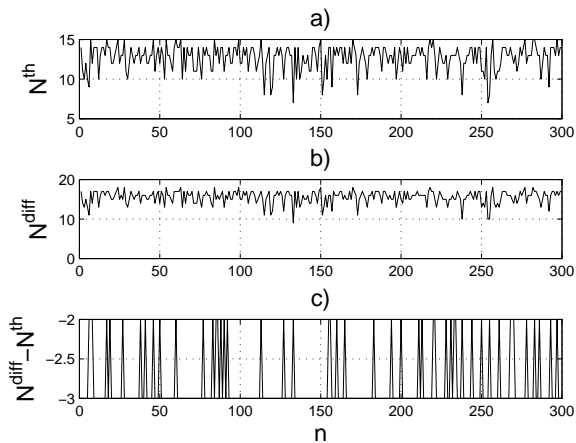


Fig. 27. Convergence time : a) with the theoretical criterion, b) with the criterion of the difference ($\hat{w}[n+1] - \hat{w}[n]$). c) the difference between the two convergence times.

VI. CONCLUSION

This paper has proposed a new digital calibration method for static gain and offset mismatches. This method uses Comb-filter on each channel without any additional material resources except for an accumulator in each channel for the implementation of the LMS algorithm. The proposed method

has a very short run time calibration estimated of 10 and 15 clock cycles for offset and gain calibration respectively. With this short run time, the calibration method could be often applied especially when the receiver is in the standby phase to update the correction coefficients to the time variation of analog imperfections. This method could be used also for other parallel ADC architectures such as the Parallel Sigma Delta ($\Pi\Sigma\Delta$) using Hadamard modulation. It may also be adapted to conventional TI ADC.

The proposed calibration method facilitates the adaptation of time interleaved architecture to achieve high performances ADC. However, there are a lot of challenges and difficulties to implement this architecture such as the implementation of the interpolation function, the dynamic channel mismatch which is much more difficult and more expensive to calibrate and the clock skew which needs to be reduced even when a full rate sample/hold circuit is used at the front-end of the ADC.

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REFERENCES

- [1] J. Mitola, "The software radio architecture," *Communications Magazine, IEEE*, vol. 33, pp. 26–38, 1995.
- [2] J. Mitola III and Jr Maguire, "Cognitive radio: making software radios more personal," *IEEE personal communications*, vol. 6, pp. 13–18, 1999.
- [3] A. Eshraghi and T. Fiez, "A time-interleaved parallel $\Delta\Sigma$ A/D converter," *IEEE Trans. Circuit and Sys.II*, vol. 50, pp. 118–129, March 2003.
- [4] A. Eshraghi, "High-Speed Parallel Delta-Sigma Analog-To-Digital Converters," *Phd thesis, Washinton State University*, May 1999.
- [5] V.T. Nguyen, P. Loumeau, and J.F. Naviner, "An interleaved delta-sigma analog to digital converter with digital correction," *IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. 4, 2002.
- [6] V.T. Nguyen, P. Loumeau, and J.F. Naviner, "Analysis of time-interleaved delta-sigma analog to digital converter," *IEEE Vehicular Technology Conference*, vol. 4, pp. 1594–1597, 2002.
- [7] I. Galton and H.T. Jensen, "Delta-sigma modulator based A/D conversion without oversampling," *IEEE Trans. Circuit and Sys.II*, vol. 42, no. 12, pp. 773–784, December 1995.
- [8] P. Benabes, A. Beydoun and J. Oksman, "Extended frequency-band-decomposition sigma-delta A/D converter," *Analog Integrated Circuits and Signal Processing, Springer*, Jan 2009.
- [9] V.T. Nguyen, P. Loumeau, J.F. Naviner and P. Benabes, "Convertisseur sigma delta," *Patent, Number Fr 08-53213*, may 2008.
- [10] C. Vogel and G. Kubin, "Modeling of time-interleaved ADCs with nonlinear hybrid filter banks," *AEUE-International Journal of Electronics and Communications, Elsevier*, vol. 59, no. 5, pp. 288–296, 2005.
- [11] C. Vogel, "The impact of combined channel mismatch effects in time-interleaved ADCs," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 1, pp. 415–427, 2005.
- [12] C. Vogel and H. Koepl, "Behavioral modeling of time-interleaved ADCs using MATLAB," *Proc. Austrochip*, pp. 45–48, 2003.
- [13] A. Petraglia and SK. Mitra, "Analysis of mismatch effects among A/D converters in a time-interleaved waveform digitizer," *Instrumentation and Measurement, IEEE Transactions on*, vol. 40, no. 5, pp. 831–835, 1991.
- [14] A. Beydoun, V. T. Nguyen, L. Naviner and P. Loumeau, "65 nm digital processing for $TIHP\Sigma\Delta$ A/D converters in multistandard applications," *IEEE, ISCAS, International Symposium on Circuits and Systems, Taipei, Taiwan*, May 24-27, 2009.
- [15] RD. Batten, A. Eshraghi and TS. Fiez, "Calibration of Parallel $\Sigma\Delta$ ADCs," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 6, pp. 390–399, 2002.
- [16] J.E. Eklund and F. Gustafsson, "Digital offset compensation of time-interleaved ADC using randomchopper sampling," *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 3, 2000.

- [17] A. Shoval, D.A. Johns and W.M. Snelgrove, "Comparison of DC offset effects in four LMS adaptive algorithms," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, pp. 176–185, 1995.
- [18] V. Ferragina, A. Fornasari, U. Gatti, P. Malcovati, and F. Maloberti, "Gain and offset mismatch calibration in time-interleaved multipath A/D sigma-delta modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 12, pp. 2365–2373, 2004.
- [19] D. Fu, K.C. Dyer, S.H. Lewis and P.J. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1904–1911, 1998.
- [20] A. Beydoun, V.T. Nguyen and P. Loumeau, "A Novel Digital Calibration Technique for Gain and Offset Mismatch in Parallel $T\Sigma\Delta$ ADCs," *IEEE, ICASSP*, 2010.
- [21] A. Eshraghi and T. Fiez, "A comparative analysis of parallel delta-sigma ADC architectures," *IEEE Trans. Circuit and Sys.I*, vol. 51, pp. 450–458, March 2004.
- [22] A. Beydoun, V.T. Nguyen and P. Loumeau, "Correction des défauts analogiques dans des convertisseurs analogiques/numeriques paralleles, notamment pour des applications multistandards, radio logicielle et/ou radio-cognitive," *Patent, Number Fr 09-55351*, July 2009.
- [23] A. Beydoun, C. Jabbour, H. Fakhoury, V.T. Nguyen, L. Naviner, and P. Loumeau, "A 65 nm CMOS Versatile ADC using Time Interleaving and $\Sigma\Delta$ modulation for Multi-mode Receiver," *IEEE, NEWCAS-TAISA, Toulouse, France, 28 June-1 July, 2009*.



Patrick Loumeau received the engineer degree in 1982 from the Institut National des Telecommunications in Paris, France. He received the authorization to manage research diploma in 2000. He joined the Ecole Nationale Supérieure des Telecommunications of Paris in 1982. He is Professor in the Analog and Mixed IC Design group, Communications and Electronics Department. He is in charge of research on analog and mixed IC for telecommunications. He has realized a number of research and development project with industry, national research center and universities. He has co-authored more than 50 technical publications in international congress and revues. He is a member of IEEE Solid State Circuits Society, and Circuits and Systems Society.



applications and spectrum sensing algorithms.

Ali Beydoun was born in Beirut, Lebanon, in 1980. He received a B.S. in Electronics from the University of Lebanon in 2002, an Engineering Degree in Telecommunications from the ENSIETA school, Brest, France, in 2004 and a Ph.D in Electronics from Paris XI university in 2007. From 2007 to 2009, he was a research assistant at the Institut Telecom - ParisTech. Since October 2009, he is assistant professor at the Lebanese university. His research focuses on the development of advanced RF architecture for software and cognitive radio



Van Tam Nguyen received the Diplôme d'Ingénieur from Ecole Supérieure d'Electricité (Supelec - www.supelec.fr) and a M.Sc. degree in automatic and signal processing from University Paris Sud (www.u-psud.fr) in 2000, and a Ph.D. degree in Communications and Electronic from Ecole Nationale Supérieure des Telecommunications (Telecom ParisTech- www.telecom-paristech.fr) in 2004. From 2000 to 2005 he was research engineer at Schlumberger and Telecom ParisTech working mainly on European Project SPRING (Scientific Multidisciplinary Network for metering - IST-1999-12342). In 2005 he joined Telecom ParisTech as an Associate Professor. His main research interests are in the areas of cognitive radio network, software defined radio, sensor network, wireless communication system and network. In particular, his research focuses on reconfigurable radio interface, flexible radio frequency front-end, digital/analog/radio frequency partitioning, mixed signal interference cancellation, sensing algorithm for cognitive radio, algorithms for MIMO spectrum sensing, cooperation sensing with reduced delay in relaying decisions, digital oriented architecture for SoC sensor and routing algorithms in wireless sensor network for power saving.