

# A Novel 14 nm Extended Body FinFET for Reduced Corner Effect, Self-Heating Effect, and Increased Drain Current

Cheng-Hsien Chang, Jyi-Tsong Lin, Po-Hsieh Lin, Hung-Pei Hsu, Chan-Hsiang Chang, Ming-Tsung Shih, Shih-Chuan Tseng, and Min-Yan Lin

**Abstract**—In this paper, we have proposed a novel FinFET with extended body under the poly gate, which is called EB-FinFET, and its characteristic is demonstrated by using three-dimensional (3-D) numerical simulation. We have analyzed and compared it with conventional FinFET. The extended body height dependence on the drain induced barrier lowering (DIBL) and subthreshold swing (S.S) have been also investigated. According to the 3-D numerical simulation, the proposed structure has a firm structure, an acceptable short channel effect (SCE), a reduced series resistance, an increased on state drain current ( $I_{on}$ ) and a large normalized  $I_{DS}$ . Furthermore, the structure can also improve corner effect and reduce self-heating effect due to the extended body. Our results show that the EB-FinFET is excellent for nanoscale device.

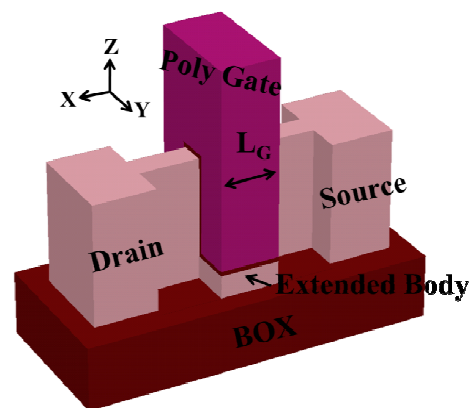
**Keywords**—SOI, FinFET, tri-gate, self-heating effect.

## I. INTRODUCTION

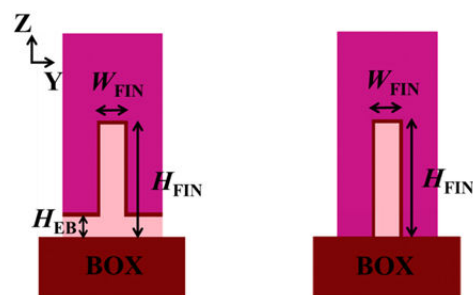
IN recent years, pursuit of scalability, leading to non-ideal effects such as quantum effect and short channel effect (SCE) severely degrades the performance of CMOS devices. When a traditional MOSFET is continuously scaled down, it will face many challenges. At this time, the silicon on insulator (SOI) fin-shaped field-effect transistor (FinFET) and multi-gate FET (MuFET) have absorbed a lot of attraction because their fabrication are fully compatible with standard CMOS process [1], [2]. SOI FinFET and MuFET possess multiple channels so they have a better controllability, higher SCE immunity, and higher current drive. However, although SOI FinFET and MuFET have aforementioned advantages, they also bring some other disadvantages, such as corner effect in relation to the multiple-gate structure, which resulting in current gather in the corner crowdedly, and even produce much heat leading to self-heating. Moreover, because we utilize SOI technology, SiO<sub>2</sub> dissipates heat harder compared than bulk Si does [3]-[8].

In this letter, we propose a novel extended-body FinFET to reduce corner, self-heating and increase drain current. Our structure is alike that conventional FinFET is elevated and has an additional body under its fin so that we call it an extended-

body FinFET (EB-FinFET). Owing to the extended body, EB-FinFET has a hardness structure, compared with the conventional FinFET. Fig. 1 (a) illustrates the schematic of the EB-FinFET. Fig. 1 (b) shows the cross section of conventional FinFET and EB-FinFET, in which we label the extended body height as  $H_{EB}$ .



(a)



(b)

Fig. 1 (a) Three-dimensional view of the EB-FinFET (b) The cross section of the EB-FinFET and the conventional FinFET

## II. DEVICE PROCESS AND SIMULATION METHOD

The key process flow of the new-designed EB-FinFET is illustrated in Fig. 2, and the device parameters are listed in the Table I. Our proposed device was carried out on the SOI

The authors are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan, R.O.C. (phone: (+886) 7-5252000, ext: 4122, fax: (+886) 7-5254199, e-mail: jtlin@ee.nsysu.edu.tw).

wafer. Firstly, we utilize first mask to etch the fin shape by electron beam (EB) lithography, but the bottom of the fin remains on Si rather than on silicon dioxide, which was not etched completely as shown in Fig. 2 (b). And then, extended body region was etched through the second mask as shown in Fig. 2 (c). The gate length was 14nm, so was the extended body length. Before the gate patterning, we used the  $\text{NH}_3$  annealing process to remove the surface defects caused by the RIE process. Then, the gate oxide layer with its effective oxide thickness (EOT) of 1nm was deposited. Next, the poly gate was deposited, and the third mask was used for the gate patterning and redefined the active region as shown in Fig. 2 (d). The source/drain doping process was performed by ion implantation and activated by rapid thermal annealing (RTA), and the source/drain concentration was  $1 \times 10^{20} \text{cm}^{-3}$ . Finally, the BEOL (back end of line) fabrication process included the metal interconnect process and plug formation was carried out.

TABLE I  
THE PARAMETERS USED FOR THE FINFET AND THE EB-FINFET

Device Parameters	FinFET	EB-FinFET
Fin length	42 nm	42 nm
Fin Width	6 nm	6 nm
Fin Height	27 nm	27 nm
Gate length ( $L_g$ )	14 nm	14 nm
Extended Body Height ( $H_{EB}$ )	Not defined	5~10 nm
BuriedOxideThickness	14 nm	14 nm
Barrier	0.575	0.575
Body Doping Concentration	$10^{15} \text{cm}^{-3}$	$10^{15} \text{cm}^{-3}$
S/DDoping Concentration	$10^{20} \text{cm}^{-3}$	$10^{20} \text{cm}^{-3}$

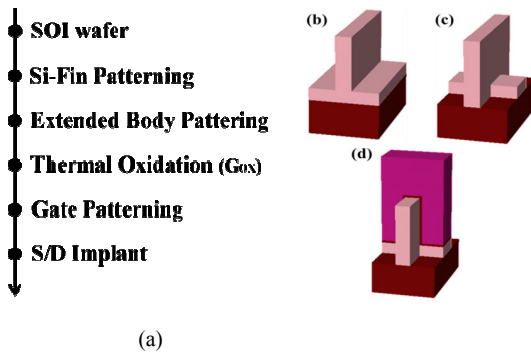


Fig. 2 (a) Device fabrication process flow (b) Fin shape was formed after the first mask (c) Extended body patterning was achieved (d) The poly gate was deposited and patterned

Our proposed EB-FinFET device has been evaluated by ISE-TCAD three dimension (3-D) simulator [10], and compared with the conventional FinFET. We used the Shockley-Read-Hall recombination included doping, temperature, tunneling dependence, and Auger Avalanche to simulate carrier's recombination and generation. Besides, the mobility model including the High Field Saturation and transverse field dependence are specified. Also, the Effective Intrinsic Density (oldSlotboom) was used to describe the intrinsic carrier concentration. Finally, due to scaling of the device, Hydrodynamic model is used in all simulations.

### III. RESULTS AND DISCUSSION

Fig. 3 illustrates the normalized  $I_{DS}-V_{GS}$  characteristics of conventional FinFET and EB-FinFET with  $V_{DS}=0.05\text{V}$  and  $V_{DS}=1\text{V}$ . It is observed that our structure can maintain conventional characteristics. In fact, the leakage current and on state drain current ( $I_{ON}$ ) are reduced and increased, respectively. There will be a more detailed explanation, latter. Fig. 4 shows the normalized  $I_{DS}-V_{DS}$  characteristics of conventional FinFET and EB-FinFET with  $V_{GS}=1\text{V}$ . It is clear that both of them suffer from self-heating effect, but the  $I_{DS}$  of EB-FinFET exhibits higher current. Because the extended body helps to dissipate heat, the mobility of electron increases, which resulting in that  $I_{DS}$  of EB-FinFET rises up.

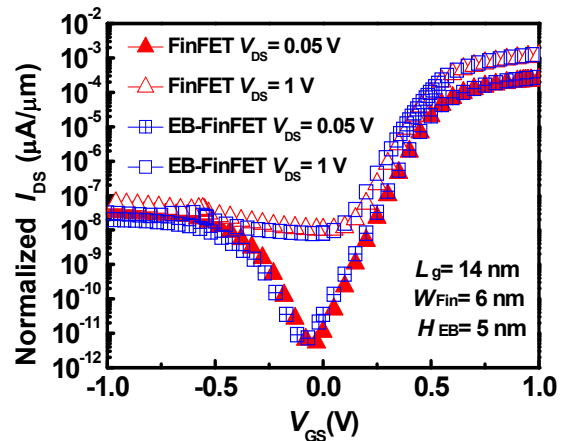


Fig. 3  $I_D-V_{GS}$  characteristics of FinFET, and EB-FinFET with 14nm gate length and 5nm extended body height

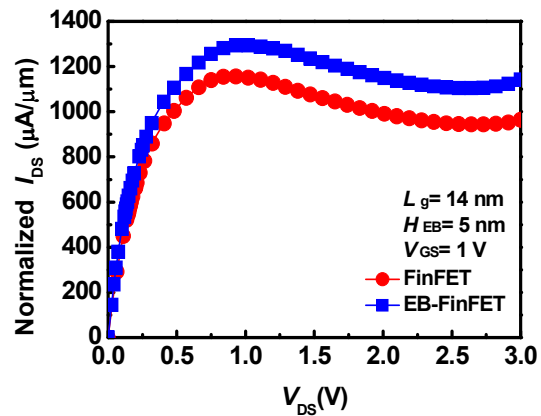


Fig. 4  $I_D-V_{DS}$  characteristics of FinFET, EB-FinFET with 14nm gate Length and 5nm extended body height

Fig. 5 shows the on state drain current ( $I_{ON}$ ) versus different extended body height from 5nm to 10nm. It can be seen that the higher extended body height is, the higher on state drain current ( $I_{ON}$ ) is. The on state drain current ( $I_{ON}$ ) drops when the extended body height is at a 10nm thickness because the volume of additional body increases too much, which resulting in raising the probability of leakage current. The drain induced

barrier lowering (DIBL) and subthreshold swing (S.S) are plotted in Figs. 6 and 7, respectively. It is observed that DIBL and S.S characteristics of EB-FinFET increase as the extended body height increases. The phenomenon still can be seen at a 9nm thick  $H_{EB}$ , but the curve declines at a 10 nm thick  $H_{EB}$ . According to our previous research [9], we consider that the drain electric field is partially dispersed due to extended body region, so the DIBL and S.S characteristics drop slightly. Although the DIBL and S.S characteristics of EB-FinFET are not better than conventional, they have an acceptable SCE.

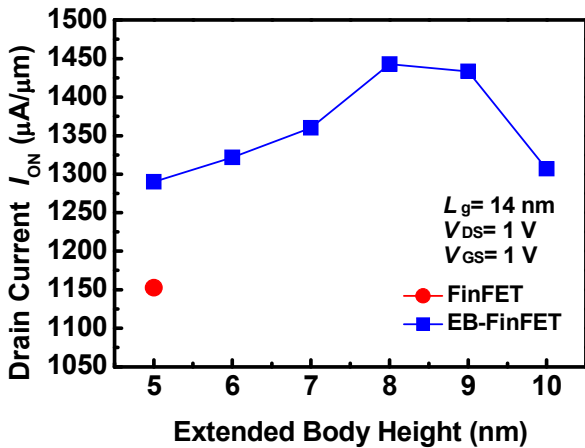


Fig. 5 Drain current ( $I_{ON}$ ) characteristic of the EB-FinFET with extended body height from 5nm to 10nm

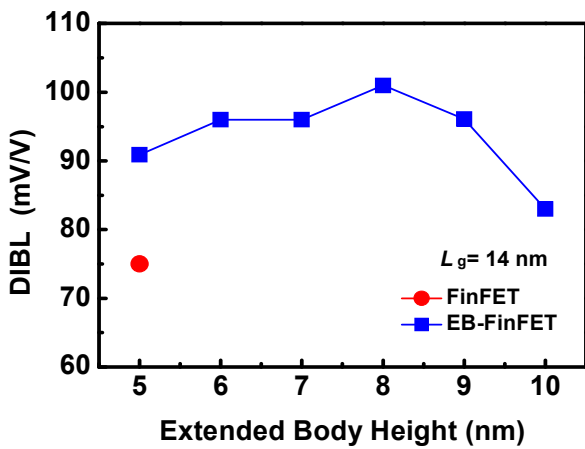


Fig. 6 DIBL characteristic of FinFET, EB-FinFET with 14nm gate length versus extended body height from 5nm to 10nm

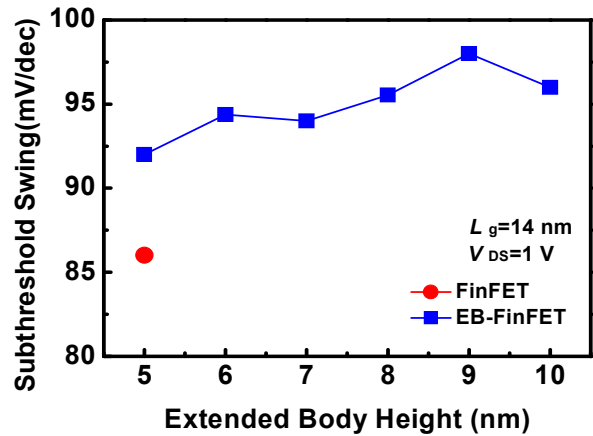


Fig. 7 Subthreshold swing characteristic of FinFET, EB-FinFET with 14nm gate length versus extended body height from 5nm to 10nm

Fig. 8 shows that series resistance ( $R_{tot}$ ) versus  $V_{GS}$ . We clearly see the  $R_{tot}$  of the EB-FinFET is lower than that of conventional FinFET because of the extended body. This is one of the reasons for the increase of the drain current. Lattice Temperature distribution of the FinFET and EB-FinFET are plotted in Fig. 9. It can be seen that the conventional FinFET has a higher lattice temperature than EB-FinFET has. Due to the extended body, it helps to dissipate heat. Fig. 10 clearly shows lattice temperature along X axis. The maximum temperature of EB-FinFET is 543K, whereas FinFET is 582K. From the figure, the temperature of our structure surely reduces, so it can prove why the drain current increases.

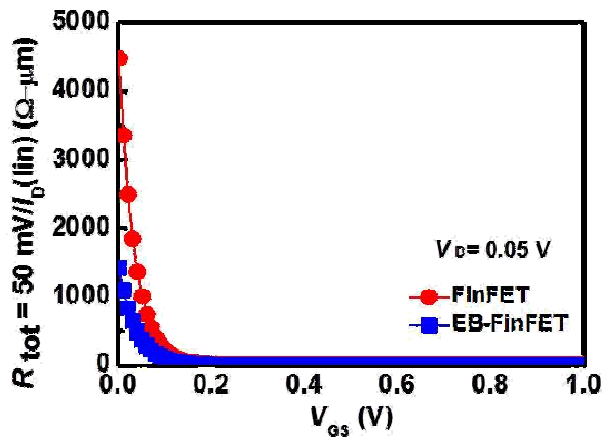


Fig. 8 The series resistance ( $R_{tot}$ ) curve of FinFET, EB-FinFET at  $V_D=0.05V$

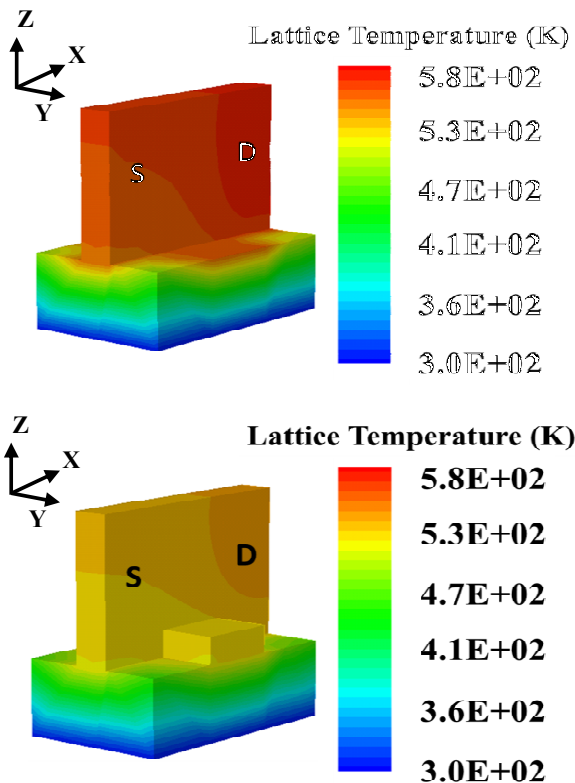


Fig. 9 (a) The lattice temperature distribution of FinFET (b) The lattice temperature distribution of EB-FinFET

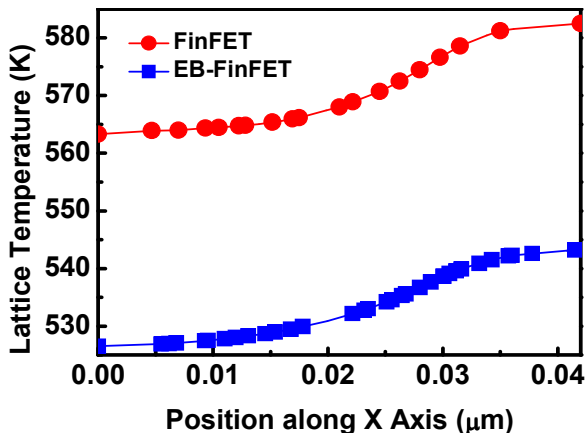


Fig. 10 Lattice Temperature along X axis for the FinFET, EB-FinFET

#### IV. CONCLUSION

In this work, we have proposed a new extended body FinFET, which is called EB-FinFET and also, analyzed the influence of the different extended body height. EB-FinFET has a hardness structure, an acceptable drain induced barrier lowering (DIBL) and subthreshold swing (S.S), a reduced series resistance, and an increased drain current drive. Furthermore, the extended body region can help to dissipate

heat and reduce the self-heating effect of the device. Therefore, we consider that the EB-FinFET can be a promising device in the future for nano CMOS and 1/T DRAM applications.

#### ACKNOWLEDGMENT

The authors would like to thank the National Center for High-performance Computing (NCHC) for computer time and facilities.

#### REFERENCES

- [1] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320-2325, Dec. 2000.
- [2] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, Member, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub-50 nm P-Channel FinFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880-886, May 2001.
- [3] A. A. Orouji, and M. Mehrad, "A New Rounded Edge Fin Field Effect Transistor for Improving Self-Heating Effects," *Japanese Journal of Applied Physics*, vol. 50, pp. 124303-1-6, 2011.
- [4] M. Mehrad and A. A. Orouji, "Partially Cylindrical Fin Field-Effect Transistor: A Novel Device for Nanoscale Applications," *IEEE Trans. Electron Devices and Materials Reliability*, vol. 10, no. 2, pp. 271-275, June 2010.
- [5] L. Mathew, M. Sadd, S. Kalpat, M. Zavala, T. Stephens, R. Mora, S. Bagchi, C. Parker, J. Vasek, D. Sing, R. Shimer, L. Prabhu, G.O. Workman, G. Ablen, Z. Shi, J. Saenz, B. Min, D. Burnett, B.-Y. Nguyen, J. Mogab, M.M. Chowdhury, W. Zhang, J.G. Fossum, "Inverted T channel FET (ITFET)—Fabrication and characteristics of vertical-horizontal, thin body, multi-gate, multi-orientation devices, ITFET SRAM bit-cell operation. A novel technology for 45nm and beyond CMOS," in *IEDM Tech. Dig.*, pp. 713-716, 2005.
- [6] X. Xu, R. Wang, R. Huang, J. Zhuge, G. Chen, X. Zhang, and Y. Wang, "High-Performance BOI FinFETs Based on Bulk-Silicon Substrate," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3246-3250, Nov. 2008.
- [7] M. Shrivastava, M. S. Baghini, D. K. Sharma, and V. R. Rao, "A Novel Bottom Spacer FinFET Structure for Improved Short-Channel, Power-Delay, and Thermal Performance," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1287-1293, June 2010.
- [8] X. Sun, V. Moroz, N. Damrongplisit, C. Shin, and T.-J. King Liu, "Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3294-3299, Oct. 2011.
- [9] Y.-C. Eng, J.-T. Lin, C.-H. Kuo, P.-H. Lin, Y.-H. Fan, and H.-H. Chen, "Numerical Study of a Highly Scaled Bulk MOSFET With Block Oxide and Source/Drain-Tied Structure," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1381-1387, 2011.
- [10] User's manual, ISE TCAD, 2004.