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A New Approach to Design Low Power Continues-Time Sigma-Delta Modulators

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***Abstract*—**This paper presents the design of a low power second-order continuous-time sigma-delta modulator for low power applications. The loop filter of this modulator has been implemented based on the nonlinear transconductance-capacitor (Gm-C) by employing current-mode technique. The nonlinear transconductance uses floating gate MOS (FG-MOS) transistors that operate in weak inversion region. The proposed modulator features low power consumption (<80uW), low supply voltage (1V) and 62dB dynamic range. Simulation results by HSPICE confirm that it is very suitable for low power biomedical instrumentation designs.

***Keywords*—**Sigma-delta, modulator, Current-mode, Nonlinear Transconductance, FG-MOS.

I. Introduction

THE motivation for using system-on-chip technique in sensing, recording and processing of physical signals, ranging from micromachined silicon sensor readouts to biological signals has increased the interest of researchers in the applications of low frequency analog-to-digital circuits in the front-end of these systems. Since many of these systems are designed to be portable, having low power consumption and low supply voltage is crucial. Continuous-time (CT) current-mode circuits that operate in subthreshold region open a possibility to design converter architectures that are suitable for these systems [1], [2].

In this work, a new approach based on the current mode technique for designing of a continuous-time sigma-delta modulator which is an analog part of the oversampeling *A/D* converter, is presented [3]. The technique provides low power consumption, low voltage power supply, mixed analog-digital design and low circuit complexity. In addition, like other CT modulators, it has some advantages over their discrete-time (DT) modulator counterparts; for example the existence of an implicit anti-aliasing filter associated with the CT modulator [4], [5] and the possibility of significantly lowering the gain-bandwidth product of the active elements in the loop filter, compared to that of the traditional DT modulator counterpart, that implies lower power consumption [6]. The proposed modulator uses the nonlinear transconductance of the FG-MOS transistor based on its I-V characteristic in thesubthreshold region.

The paper organized as follows. In section 2 the analytical model of the proposed sigma-delta modulator is presented. In section 3 the circuits of, loop filter, one bit quantizer, and D/A, as the basic building blocks of the modulator, are discussed. In section 4 simulation results of a second-order modulator to demonstrate the validity of the proposed method is presented.

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II. Analytical Model

A. DT-to-CT Conversion

Most works in sigma-delta modulator with a great deal of software tools focused on DT modulator, so to design a CT modulator it is advantageous to start first with a DT loop filter and then proceed with a DT to CT conversion to produce the equivalent CT modulator [4], [7]. A general linearized model of a DT sigma-delta modulator is shown in Fig. 1. Typically, the quantization error *e(n)* caused by the one bit quantizer inside the modulator is assumed to be an additive noise. The operation of the modulator can be expressed as:

$$Y(z) = STF(z)\cdot X(z) + NTF(z)\cdot E(z) \tag{1}$$

$$NTF(z) = \frac{1}{1+H(z)} \tag{2}$$

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{3}$$

in which $X(z)$, $Y(z)$ and $E(z)$ are the z-transforms of input, output and additive noise respectively; $NTF(z)$ is noise transfer function, $STF(z)$ is signal transfer function and $H(z)$ is the DT loop filter transfer function.

The most used and the simplest noise-shaping function to create a notch shaped $NTF(z)$ function for a k^{th} order sigma-delta modulator is:

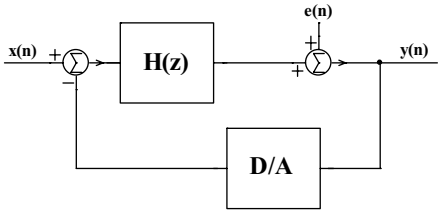


Fig. 1 Linearized model of a DT sigma-delta modulator

$$NTF(z) = \left(1 - z^{-1}\right)^{k}. \tag{4}$$

For a second-order modulator (k=2), substituting (4) in (2) results the following DT loop filter transformation:

$$H(z)=\frac{2z-1}{(z-1)^2}. \tag{5}$$

Rewriting (5) based on its partial fraction terms results:

$$H(z)=\frac{2}{z-1}+\frac{1}{(z-1)^2}. \tag{6}$$

Fig. 2 shows the block diagram of a general CT sigma-delta modulator, which consists of a loop filter H(s), non-return to zero (NRZ) D/A and a quantizer. In this modulator the analog input signal is modulated to a digital word sequence with a frequency spectrum that approximates the analog input spectrum in a narrow frequency range, while the quantization noise is shaped away from this frequency range.

By clocking the quantizer that consists of a one bit A/D and a D-latch, the transfer function of the loop from the output of the quantizer back to its input, is exactly equivalent to the z-domain transfer function $H(z)$. The sample values of the continuous-time waveform at the input of the quantizer define the discrete-time impulse response of the continuous-time loop [4]. Now the objective is to apply the DT to CT conversion for a given non-return to zero (NRZ) D/A feedback, CT loop filter $H(s)$ and DT loop filter $H(z)$, so that applying impulse-invariant transformation in time domain results[4], [7]:

$$Z^{-1}\{H(z)\}=\pounds^{-1}\left\{\frac{1-exp(-sT)}{s}\cdot H(s)\right\}_{t=nT} \tag{7}$$

in which T is period of sampling, Z^{-1} is inverse z-transform operator, $\pounds^{-1}$ is inverse laplace-transform operator and $H(s)$ is the CT equivalent of the DT loop filter transfer function $H(z)$.

Applying above transformation for each term of partial fraction terms of (6) results [7]:

$$\frac{2}{z-1} \quad \rightarrow \quad \frac{2}{sT} \tag{8–1}$$

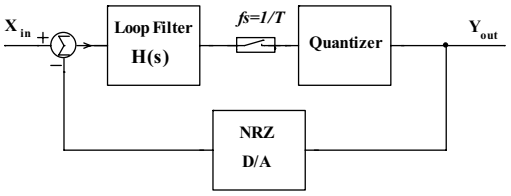


Fig. 2 Block diagram of a CT sigma-delta modulator

$$\frac{1}{(z-1)^2} \quad \rightarrow \quad \frac{1-0.5sT}{(sT)^2} \tag{8–2}$$

Thus the equivalent s-domain transfer function $H(s)$ is expressed as:

$$H(s)=\frac{2}{sT}+\frac{1-0.5sT}{(sT)^2} \quad \rightarrow \quad H(s)=\frac{1+1.5sT}{(sT)^2} \tag{9}$$

B. Nonlinear Transconductance-Capacitor Approach

For implementation of the loop filter in Fig. 2, many proposals that use linear transconductance-capacitance (gm-C) structure and work in the voltage-mode have been reported [4], [7]. Fig. 3 shows a single ended diagram of a gm-C voltage-mode second-order filter based on (9).

The current-mode technique employed in this work offers some important advantages over the voltage-mode technique; for example the circuits designed based on current-mode can operate at lower voltages and consume lower powers [1], [2]. The state-space equations of transfer function (9) in current-mode are:

$$\begin{cases} T\dot{I}_1 = I_{in} \\ T\dot{I}_{out} = 1.5I_{in} + I_1 \end{cases} \tag{10}$$

where I_1 is internal state space variable and I_{in} and I_{out} are the input and output signals.

To exploit a new synthesis method for current-mode log-domain systems, by employing the I-V relationship of FG-MOS transistor in the weak inversion region explained in next section, the following logarithmic mapping is applied to the current variables [3], [8], [9]:

$$I = I_b\, exp\left(\frac{V-V_{ref}}{2nU_T}\right) \tag{11}$$

where U_T is the thermal potential, n is the subthreshold slope, V_{ref} is a constant voltage, I_b is a constant current, and V is the voltage variable which is the logarithmic mapping of current variable I.

It can be shown that, substituting (11) into (10) results [9]:

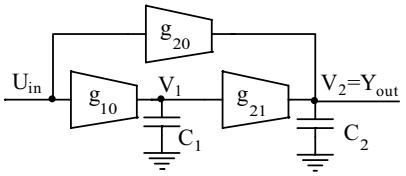


Fig. 3 Single ended diagram of a gm-C second-order filter [4]

$$\begin{cases} \dot{V}_1 = \dfrac{2nU_T}{T}\exp\left(\dfrac{V_{in}-V_1}{2nU_T}\right) \\ \dot{V}_{out} = \dfrac{3nU_T}{T}\exp\left(\dfrac{V_{in}-V_{out}}{2nU_T}\right)+\dfrac{2nU_T}{T}\exp\left(\dfrac{V_1-V_{out}}{2nU_T}\right) \end{cases} \quad (12)$$

in which, the voltage state variables V_1, V_{in} and V_{out} are nonlinearly mapping of the current state variables I_1, I_{in} and I_{out}, respectively.

In order to implement dynamic term of voltage state variable V_1 ,$\dot{V}_1$, capacitors C_1 is employed. In a similar way, to implement dynamic term of the output voltage V_{out} ,$\dot{V}_{out}$, capacitor C_2 is used. In such case, multiplication both sides of first equation of (12) by capacitor C_1 and second equation by capacitor C_2, and then using capacitor equation $I_c = C\dfrac{dV_c}{dt}$, this set of equations can be expressed as:

$$\begin{cases} I_{c,1} = I_{bT}\, exp\left(\dfrac{V_{in}-V_1}{2nU_T}\right) \\ I_{c,2} = I_{bT}\, exp\left(\dfrac{V_{in}-V_{out}}{2nU_T}\right)+I_{bT}\, exp\left(\dfrac{V_1-V_{out}}{2nU_T}\right) \end{cases} \quad (13)$$

in which, $I_{c,1}$ and $I_{c,out}$ are current capacitors of capacitors C_1 and C_2, respectively.

Also, the bias current I_{bT} is defined as follows:

$$I_{bT} = \frac{2U_T C}{T} \quad (14)$$

For circuit implementation of the loop filter in current-mode, the nonlinear transconductance $G_m(V_i, V_j)$ is defined as following [8]:

$$G_m(V_i, V_j) = I_{bij}\, exp\left(\frac{V_i - V_j}{2nU_T}\right) \quad (15)$$

By this definition the output current of the nonlinear transconductance as obtained as:

$$I_{ij} = G_m(V_i, V_j) \quad (16)$$

and using (16) into (13), it can be rewritten as follows:

$$\begin{cases} I_{c,1} = G_{10}(V_{in}, V_1) \\ I_{c,out} = G_{20}(V_{in}, V_{out}) + G_{21}(V_1, V_{out}) \\ I_{in} = G_{00}(V_{in}, V_{ref}) \\ I_{out} = G_{22}(V_{out}, V_{ref}) \end{cases} \quad (17)$$

Equation (17) demonstrate that the current-mode nonlinear transconductance-capacitor (*Gm-C*) realization of the loop filter can be obtained, using its equivalent voltage-mode linear transconductance-capacitor (*gm-C*) realization, just by replacing the linear transconductance g_{ij} having input node *i* and output node *j* $(i, j \in \{1, in, out\})$ in the g_m-*C* realization by nonlinear transconductance $G_m(V_i, V_j)$. The resulting proposed synthesis has some advantages, such as: regularity and generality, because it keeps the conventional transconductance-capacitor (g_m-*C*) invariant; simplicity, because complexity is regardless of the system size. Also, as it extracted by simple substitution, it preserves the LTI topology. In addition, it allows to readily relation between compressed variables and their counterparts in an externally equivalent linear implementation [3]. Fig. 4 shows the single ended diagram of the second-order filter based on nonlinear transconductance G_m.

In the next section first the implementation of the nonlinear transconductance G_{ij} is presented, then for designing a fully-differential second order sigma-delta modulator the proposed nonlinear transconductance-capacitor structure (G_m-*C*) is employed.

III. Circuit Design

Fig. 5 shows a fully differential structure for a second-order sigma-delta modulator that consists of a fully-balanced current-mode loop filter, a quantizer and two NRZ DACs [10]. Implementation of these subcircuits and also the nonlinear transconductance G_{ij} are discussed in this section.

A. Nonlinear Transconductance

A good choice for circuit design of loop filter is using FG-MOS transistors that operate in weak inversion. A FG-MOS transistor with *N* input voltages consists of a floating gate electrode extended over the channel and *N* input gates located over the floating gate. In other words, the FG-MOS transistor is a MOS transistor with an isolated gate that capacitively coupled to the inputs[1].

Fig. 6 shows the symbol diagram and equivalent circuit of the transistor with 2 input voltages.

The drain current of a N-type FG-MOS transistor in weak inversion region is given by [11]:

$$I_d = I_s\, exp(\frac{V_{FG}}{nU_T}) \quad (18)$$

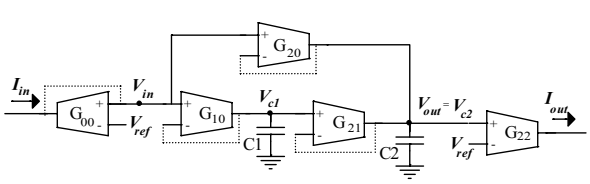


Fig. 4 Single ended diagram of the second-order filter based on nonlinear transconductance G_m

where U_T stands for the thermal potential, I_s is a device dependent coefficient, *n* represents the subthreshold slope and V_{FG} is voltage of floating gate electrode

Applying charge conservation law, the voltage at the floating gate with two equal input capacitances, which is used in this work, is obtained by:

$$V_{FG} = w_1 V_1 + w_2 V_2 + \frac{C_{gd}}{C_t} V_{gd} + \frac{C_{gs}}{C_t} V_{gs} + \frac{C_{gb}}{C_t} V_{gb} + \frac{Q_{fg}}{C_t} \qquad (19)$$

V_i is the *i*-th input gate voltage $\left(i \in \{1,2\}\right)$, C_t is the sum of capacitors that are connected to the floating-gate, C_{gd}, C_{gs}, C_{gb} are the parasitic capacitors between the floating gate and the drain, source and bulk, respectively, Q_{fg} is residual charge trapped at the floating gate during fabrication process (This latter charge can be made negligible by using the technique described in [12]) and w_i is input capacitance ratio of *i*-th input gate, and is defined as:

$$w_i = \frac{C_i}{C_t} \qquad (20)$$

in which C_i is the input capacitance between the floating gate and the *i*-th input gate. From (20) it is evident that the input capacitance ratios of FG-MOS transistor with two equal input capacitances are 1/2 $\left(w_i = 1/2\right)$. If the sum of input capacitances is much larger than parasitic capacitances, i.e.,

$$C_1 + C_2 >> C_{gd}, C_{gs}, C_{gb} \qquad (21)$$

then using (19), the voltage at floating gate with two equal input capacitances can be approximated by:

$$V_{FG} \cong \frac{1}{2} V_1 + \frac{1}{2} V_2 \qquad (22)$$

Substituting (22) into (18), the drain current of a N-type FG-MOS transistor, with two equal input capacitances, is as follows:

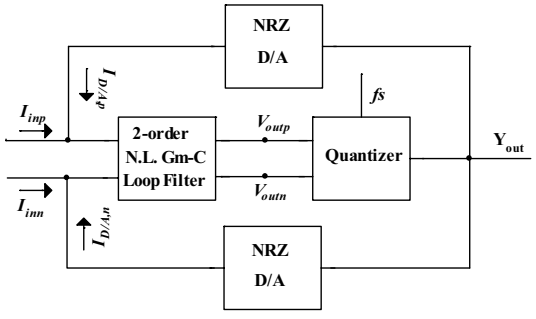


Fig. 5 A fully-differential current-mode second-order sigma-delta modulator

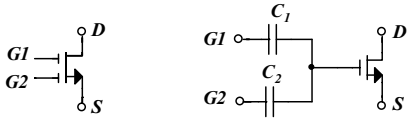


Fig. 6 Symbol diagram (left) and equavalent circuit (right) of a N-type FG-MOS transistor

$$I_d = I_s \exp\left(\frac{V_1 + V_2}{2nU_T}\right) \qquad (23)$$

Fig. 7 shows the FG-MOS implementation of the nonlinear transconductance $G_m\left(V_i, V_j\right)$. Using (23), the drain currents of transistors M1 and M2 in this Figure are obtained as:

$$I_{ij} = I_s \exp\left(\frac{V_i + V_{cm}}{2nU_T}\right) \qquad (24)$$

$$I_{bij} = I_s \exp\left(\frac{V_j + V_{cm}}{2nU_T}\right) \qquad (25)$$

and dividing (24) by (25) results:

$$I_{ij} = I_{bij} \exp\left(\frac{V_i - V_j}{2nU_T}\right) \qquad (26)$$

Comparing (26) with (15) shows that, the circuit of Fig. 7 can be used for the nonlinear transconductance G_m defined in the preceding section. As Fig. 7 shows, the proposed nonlinear transconductor circuit is designed just by using of two FG-MOS transistors, so, the number of components in the proposed circuit is much less than transconductances that reported before [4]-[7]. Also the source of transistors is connected to the substrate, so the body effect is eliminated. In addition, the transistors are operating in weak inversion; therefore this circuit can work in low-power, low-voltage and wide dynamic range. This Figure reveals that, the minimum supply voltage of the circuit is one V_{gs} plus one V_{ds} and since extra biasing current and voltage are not needed, the static power consumption is low.

Fig. 8 shows the complete circuit diagram of the proposed second-order loop filter. As the Figure shows the circuit consists of two single ended second-order loop filters (p-half filter and n-half filter) and two common mode feedback (CMFB) circuits.

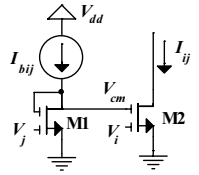


Fig. 7 Circuit diagram of the proposed transconductance Loop Filter Circuit

In p-half of the Figure (upper side), transistors M1, M2, current mirror transistors M9, M10, and current source $I_{b10,p}(=I_{bT})$ form transconductance G_{10}. Transistors M3-M6, current mirror transistors M11, M12 and current sources $I_{b20,p}(=1.5I_{bT})$, $I_{b21,p}(=I_{bT})$ are used for nonlinear transconductances G_{20} and G_{21}. For implementation of G_{00}, transistor M7 and current sources $I_{b00,p}(=I_b)$ are employed. Transistor M8 and current source $I_{b22,p}(=I_b)$ form nonlinear transconductance G_{22}. In n-half of the Figure (lower side), the rules of transistors M13-M24 are similar to those of M1-M12 in p-half of the Figure. Instead of comparing the output currents of the two n-half and p-half circuits, the related capacitance voltages of these two outputs are used as the inputs of the comparator, which has the advantage of eliminating the two nonlinear transconductanes G_{22} of the two half circuits.

As the Fig. 8 shows besides two single ended diagrams of the second-order filter, two common mode feedback (CMFB) circuits are also used for the circuit of fully-balanced loop filter. Without these CMFBs the capacitors of the filter can not be discharged. The CMFB circuit and the technique used to solve above problem adopted from [13].

Each capacitor of each half circuit is discharged by using of the counterpart state variable in the other half circuit. The extra branches do not affect the overall differential transfer function of the filter described in (10) with output current $I_{out}(=I_{outp}-I_{outn})$ and input current $I_{in}(=I_{inp}-I_{inn})$. Using the state-space equations (10) for two n-half and p-half filters and then subtraction of the extra terms caused by discharge ($\frac{I_{1p}\cdot I_{1n}}{I_{b2}}$ and $\frac{I_{2p}\cdot I_{2n}}{I_{b2}}$), it results:

$$\begin{cases} T\dot{I}_{1p} = I_{inp} - \dfrac{I_{1p}\cdot I_{1n}}{I_{b2}} \\ T\dot{I}_{outp} = 1.5I_{inp} + I_{1p} - \dfrac{I_{2p}\cdot I_{2n}}{I_{b2}} \end{cases} \quad \text{for n-half filter}$$

,

$$\begin{cases} T\dot{I}_{1n} = I_{inn} - \dfrac{I_{1p}\cdot I_{1n}}{I_{b2}} \\ T\dot{I}_{outn} = 1.5I_{inn} + I_{1n} - \dfrac{I_{2p}\cdot I_{2n}}{I_{b2}} \end{cases} \quad \text{for p-half filter} \qquad (27)$$

in which subscripts p and n refer to the p-half and n-half filters. Transistors M25, M26 form the extra branch of the CMFB circuit for the first state variable and transistors M27-M28 form the extra branch of the CMFB circuit for the second state-variable.

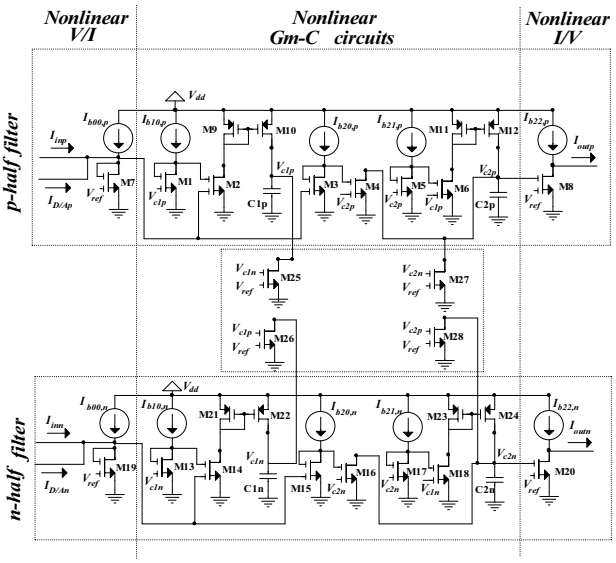


Fig. 8 Complete circuit diagram of the proposed loop filter

B. The Quantizer and D/A Converter

Fig. 9 shows the circuits of the one bit quantizer and the one bit D/A converter. As shown in Fig. 9a the quantizer is a one bit comparator, followed by a D-latch. The input stage of the comparator consists of a differential input transistor pair loaded by a cross coupled PMOS transistors. The comparator is reset during the reset phase by connection of the output nodes to the V_{dd}. The inputs of the comparator, V_p and V_n, are the capacitance voltages that are controlled by the output currents of the n-circuit and p-circuit.

Fig. 9b shows the one bit D/A converter that consists of a current source I_{ref} and two switches q and $\bar{q}$. The output of the quantizer controls the switches and the current I_{ref} is directed through the switches [14]. When switch q is turned on, the reference current I_{ref} flows in the $I_{D/Ap}$ branch and when switch q is turned off, the current flows in the $I_{D/An}$ branch.

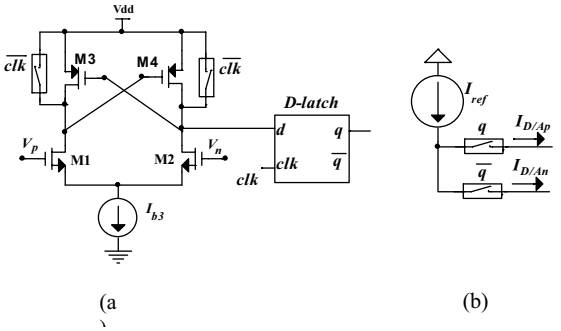


Fig. 9 a) one bit quantizer b) one bit D/A converter

IV. Simulation Results

The proposed modulator was simulated by HSPICE with TSMC 0.18um CMOS process parameters. The circuit of modulator was simulated using HSPICE with TSMC 0.35um CMOS process. $V_{dd} = 1V$, $C_{1p} = C_{1n} = C_{2p} = C_{2n} = 50pF$, $I_b = I_{bT} = 100nA$, $I_{b2} = 200nA$ and $V_{ref} = 0.75V$ were employed. The aspect ratios of the NMOS and PMOS transistors for loop filter and D/A were 20um/2um and 40um/2um, respectively. For the quantizer, the aspect ratios of the NMOS and PMOS transistors were 0.4um/0.4um and 1.6um/0.4um, respectively. For all FG-MOS transistors, the value of the input capacitance ratio was assumed ½, the aspect ratios of them were 20um/2um and also the model of reference [15] is used. The output data of the modulator was collected by HSPICE; then by MATLAB, FFT with hanning window for 2^{13} points was used to evaluate power spectral density (PSD) and signal to noise ratio (SNR). Fig. 10 shows the modulator output power spectrum for the sinusoidal input signal with frequency of 122Hz and magnitude 70.7nA (-3dBFS). The clock frequency was set to 0.1MHz.

The SNR (including distortion) vs. input is shown in Fig. 11. Here also, the input is 122Hz sinusoidal and the clock frequency was set to 0.1MHz. The oversampling ratio (OSR), defined as [16]:

$$OSR = \frac{f_s}{2BW} \tag{28}$$

was 64. As the figure shows the maximum SNR is 62dB, therefore the bit resolution, defined as [16]:

$$Bit\ \ resolution = \frac{SNR(dB) - 1.76}{6.02} \tag{29}$$

is 10 bit for the proposed modulator.

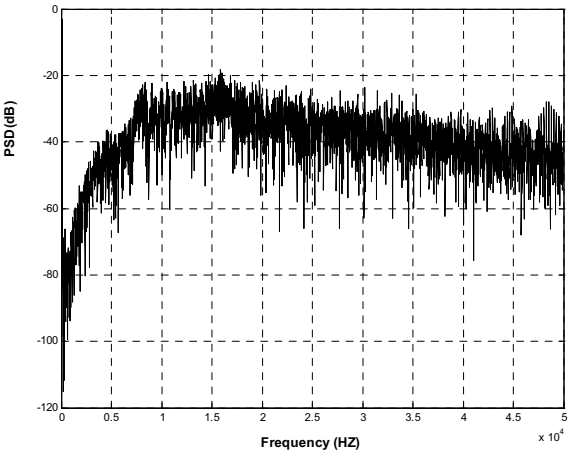
Simulation results showed the power consumption of less than 80uW for the maximum accepted input current (100nA).

The characteristics of the proposed second-order continuous-time sigma-delta modulator are summarized in Table I.

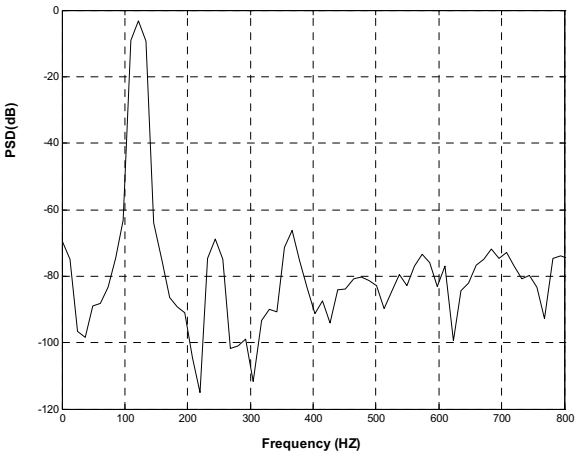
To provide more insight into the technique proposed here, a comparison was made with formerly reported low voltage/low power sigma delta modulators in Table II.

V. Conclusion

A low power/voltage fully differential second-order sigma delta modulator circuit that employs FG-MOS transistors for nonlinear transconductance is presented. The circuit work in current-mode and with low circuit complexity. Simulation results of a sigma delta converter, constructed based on the proposed nonlinear transconductance, show that the technique is promising and can be used in biomedical applications.



(a)



(b)

Fig. 10 Power spectrum of the second-order modulator
a) out of bandwidth b) in bandwidth

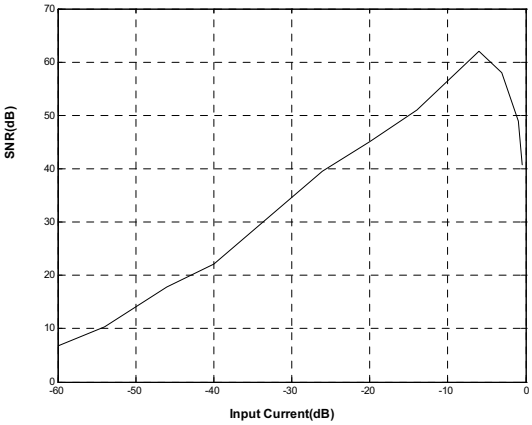


Fig. 11 Signal-to-Noise vs. input amplitude

TABLE I
CIRCUIT CHARACTERISTICS

Supply Voltage	1 V
Power Consumption	< 80 uW
Technology	0.35u CMOS
Max. Signal-to-Noise Ratio	62 dB
Sampling Frequency	100 kHZ
Order of Modulator	2nd
Bit resolution	10bit
Oversampling Ratio	64
Number of Sampling	8192

TABLE II
COMPARISON WITH FORMER SIGMA-DELTA MODULATORS

Parameter	Ref. [17]	Ref. [18]	Ref. [19]	This Work
Year	2007	2006	2005	-
Technology	0.18u	0.18u	0.18u	0.35u
Supply Voltage	1.8V	0.8V	1.8V	1V
Power Consumption	38mW	180uW	400uW	<80uW
Band Width	50kHz	5kHz	4kHz	1kHz
SNR	85.76dB	60dB	67.8dB	62dB

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