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A Low Power High Frequency CMOS RF Four Quadrant Analog Mixer

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Abstract**—**This paper describes a CMOS four-quadrant multiplier intended for use in the front-end receiver by utilizing the square-law characteristic of the MOS transistor in the saturation region. The circuit is based on 0.35 um CMOS technology simulated using HSPICE software. The mixer has a third-order inter the power consumption is 271uW from a single 1.2V power supply. One of the features of the proposed design is using two MOS transistors limitation to reduce the supply voltage, which leads to reduce the power consumption. This technique provides a GHz bandwidth response and low power consumption.

Keyword**—**RF-Mixer, Multiplier, cut-off frequency, power consumption

I. Introduction

AS wireless products such as cellular phones, global system for mobile communications (GSM), global positioning satellite (GPS), wire-less local area network (WLAN) have become a part of people's life, the need for higher performance at low costs and low power consumption of these products becomes more and more important.

On the other hand, an important block in the receiver of these systems is the mixer. The operation of a mixer can be based on an analog multiplier circuit.

In this paper a new CMOS four-quadrant analog multiplier is proposed. In section 2 the design of our proposed circuit is presented. The simulation results of this multiplier are given and compared to those of some similar circuits designed in [1-3].

II. The Proposed Multiplier

Usually, the variable trans-conductance technique which operates on Gilbert's trans-linear circuit is widely used to design multiplier circuits in bipolar and CMOS technologies [4-6]. The other approaches in CMOS technology are based on square-law characteristics of MOS transistors biased in the saturation region [7-8] or based on the current voltage characteristics of CMOS transistors biased in the non-saturation region [9-10].

Our proposed multiplier is based on the square-law characteristics of MOS transistors biased in the saturation region. The operation of four PMOS transistors to describe this law is shown in Fig. 1. Voltage V_a consists of two components DC and AC whereas voltage V_a^- has the same DC component but negative AC. This condition is valid for voltages V_b and V_b^-. The drain current of each transistor can be expressed as

$$I_{D1} = \frac{K}{2}\left(V_{DD} - V_a - V_T\right)^2 \quad (1)$$

$$I_{D2} = \frac{K}{2}\left(V_{DD} - V_a^- - V_T\right)^2 \quad (2)$$

$$I_{D3} = \frac{K}{2}\left(V_{DD} - V_b - V_T\right)^2 \quad (3)$$

$$I_{D4} = \frac{K}{2}\left(V_{DD} - V_b^- - V_T\right)^2 \quad (4)$$

where K can be taken as process technology constant, V_{DD} is the power supply, and V_T is the threshold voltage for each transistor. By some definitions as follows

$$V_a = V_1^+ + V_2^- \quad (5)$$

$$V_b = V_1^- + V_2^+ \quad (6)$$

$$V_1^+ = V_{DC1} + V_1 \quad (7)$$

$$V_1^- = V_{DC1} - V_1 \quad (8)$$

$$V_2^+ = V_{DC2} + V_2 \quad (9)$$

$$V_2^- = V_{DC2} - V_2 \quad (10)$$

then we have

$$I_1 = I_{D1} + I_{D2} = \left\{\frac{K}{2}\left\{2\left(V_{DD} - V_{DC2} - V_{DC1} - V_T\right)^2 + 2V_1^2 + 2V_2^2 + 4V_1V_2\right\}\right. \quad (11)$$

and

$$I_2 = I_{D3} + I_{D4} = \left\{\frac{K}{2}\left\{2\left(V_{DD} + V_{DC2} - V_{DC1} - V_T\right)^2 + 2V_1^2 + 2V_2^2 - 4V_1V_2\right\}\right. \quad (12)$$

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Thus one can obtain the following useful equation

$$I_1 - I_2 = 4KV_1V_2 \tag{13}$$

Fig. 1 Four MOS transistors used to describe the square-law characteristics

The proposed four-quadrant multiplier is shown in Fig. 2. The design of this multiplier is based on the circuit shown in Fig.1 and consists of 14 MOS transistors operating in the saturation region except for M5 and M6. These two transistors work as two linear resistors whose resistance can be described as [11]

$$R = \frac{1}{K\left(V_{GS} - V_T\right)} \tag{14}$$

Then using (13) the differential output of the multiplier is

$$V_O = 4RKV_1V_2 \tag{15}$$

III. Simulation Results

The performance of the proposed analog multiplier circuit is simulated using HSPICE and parameters based on 0.35 μm CMOS technology [12]. The supply voltage V_{DD} is +1.2 V while the aspect ratios for all transistors are given in Table I.

In order to analysis of the multiplier as an amplitude modulator, we set V_1 and V_2 as 300 MHz and 3 GHz sinusoidal input signals with peak amplitude of 100mV, respectively. Fig. 3 shows the transient response of the modulator. Fig. 4 shows the DC transfer characteristics of the proposed analog multiplier without any load while the input voltage range is ±100 mV.

This multiplier has also a GHz-bandwidth response with a cut-off frequency of 4.14 GHz as shown in Fig.5. This high frequency response can be due to small aspect ratios for the circuit's transistors.

The calculated power consumed in the proposed multiplier is 192 μW. In fact, using fewer transistors in comparison with some other similar circuits [1] can lead to smaller required supply voltage and hence smaller power consumption. The simulated results for the proposed multiplier are summarized and compared to those for some similar circuits in Table II.

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TABLE I
ASPECT RATIO, W/L

Transistor	Aspect ratio ($^{\mu m}/_{\mu m}$)
M1-M4	7/0.35
M5-M6	10/0.35
M7-M14	10/0.35

TABLE II
THE SIMULATED PARAMETERS FOR DIFFERENT ANALOG MULTIPLIERS

Parameter	Proposed Multiplier	[1]	[2]	[3]
Supply voltage	1.2V	1.5V	1.5V	2.5V
Number of MOS transistors	14	16	8	16
Power dissipation	192μW	1.18 mW	6.7μW	---
Cut-off frequency	4.14GHZ	900MHz	268KHz	197MHz
Technology	0.35μm	0.5μm	0.35μm	0.5μm

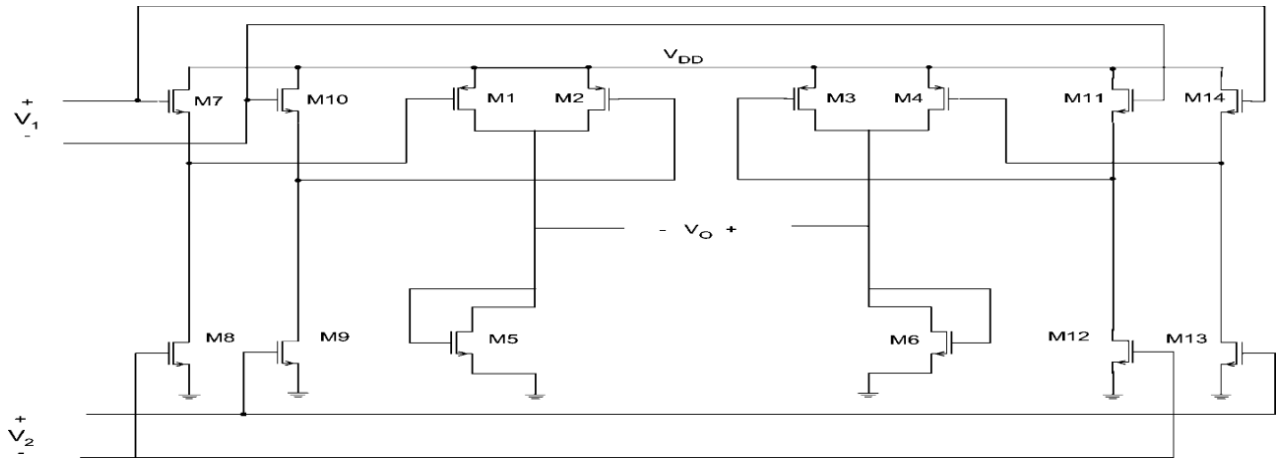

Fig. 2 The proposed multiplier

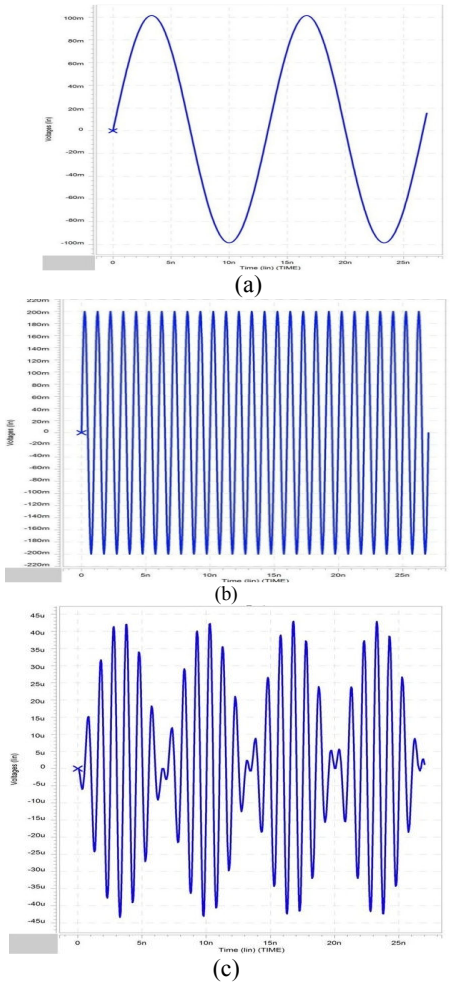

Fig. 3 The transient analysis of the multiplier as an amplitude modulator: a) input signal V_1, b) input signal V_2, c) output signal V_o

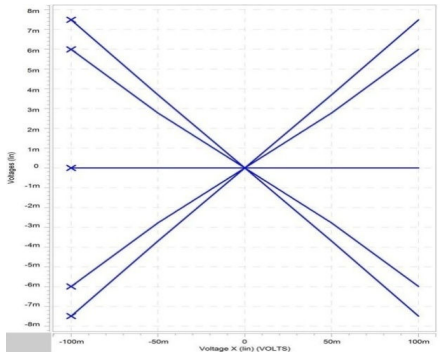

Fig. 4 DC transfer characteristics of the multiplier

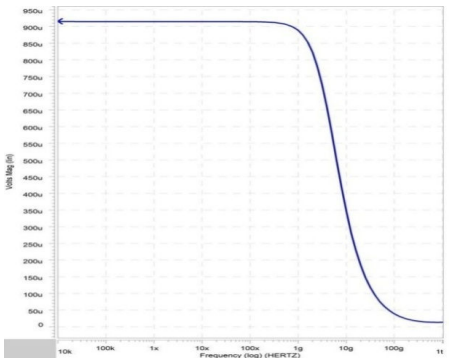

Fig. 5 The frequency response of the multiplier