International Journal of Engineering, Mathematical and Physical Sciences
ISSN: 2517-9934
Vol:4, No:11, 2010

A Clock Skew Minimization Technique Considering Temperature Gradient

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***Abstract*—**The trend of growing density on chips has increases not only the temperature in chips but also the gradient of the temperature depending on locations. In this paper, we propose the balanced skew tree generation technique for minimizing the clock skew that is affected by the temperature gradients on chips. We calculate the interconnect delay using Elmore delay equation, and find out the optimal balanced clock tree by modifying the clock trees generated through the Deferred Merge Embedding(DME) algorithm. The experimental results show that the distance variance of clock insertion points with and without considering the temperature gradient can be lowered below 54% and we confirm that the skew is remarkably decreased after applying the proposed technique.

***Keywords*—** clock, clock-skew, temperature, thermal.

I. Introduction

Due to aggressive technology scaling, density of chips increases drastically and a chip can have more functions. However, the growing current density in chips has brought the increased chip temperature. According to a research [2], power density in microprocessors doubles every three year. The temperature of high-performance VLSI affects deeply on its performance. Figure 1 illustrates the temperature of chips depending on CMOS technology generations from 350nm to 90nm. This graph means scaling trend incurs the exponential temperature increase of chips [5].

An intuitive way of decreasing temperature of chips decreases the overall power consumption, for which many low-power techniques have been studied. However, most of low-power techniques generally change the overall power consumption and cause uneven current densities depending on locations. It means that although these techniques may reduce the overall chip temperature, but the gradients of temperature would increase even higher. Reference [3] has shown that high-performance VLSI system might have the temperature gradient higher than 50℃. Temperature gradients may incur timing problem in the form of clock skew since they result in different delays in the clock sub-trees.

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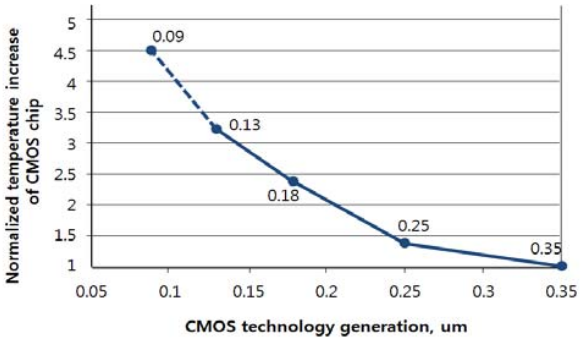

Fig. 1. Normalized chip junction temperature according to CMOS technology

Reference [1] has proposed the design of clock-distribution based on temperature gradients by improving DME algorithm under the traditional uniform temperature distribution assumption. In this paper, we propose a new balanced skew tree generation technique to minimize clock skew that is brought by temperature gradients caused from unbalanced increase of temperature.

The remainder of this paper is organized as follows. Section 2 introduces the relevant research dealing with temperature of chips. In Section 3, we propose the technique to make the balanced skew tree on clock routing. Experimental results are shown in Section 4 and Section 5 concludes this paper.

II. Background

As temperature in chips increases, resistance of the wire will increase, too. We can find a temperature-resistance function based on the temperature of wire, $T(x)$.

$$r_0(x) = r_0(1+\beta \cdot T(x)) \tag{1}$$

where r_0 is wire resistance per unit length and β represents temperature coefficient of resistance. The capacitance is assumed to be invariant with respect to the temperature. Using (1) and Elmore delay, we can write delay time of the wire under non-uniform chip temperature distribution as follow [4].

$$D = D_0 + (c_0 L + C_L) r_0 \beta \int_0^L T(x)dx - c_0 r_0 \beta \int_0^L xT(x)dx \tag{2}$$

$$D_0 = R_d(C_L + c_0 L) + (c_0 r_0 \cdot (L^2/2) + r_0 L C_L) \tag{3}$$

where D_0 is the Elmore delay at 0℃. In (2), the wire is assumed to have uniform thickness and length L and is driven by output resistance R_d. C_L is a load capacitance and c_0 and r_0 are the unit length capacitance and resistance, respectively, and β is the temperature coefficient of resistance and $T(x)$ is wire thermal profile.

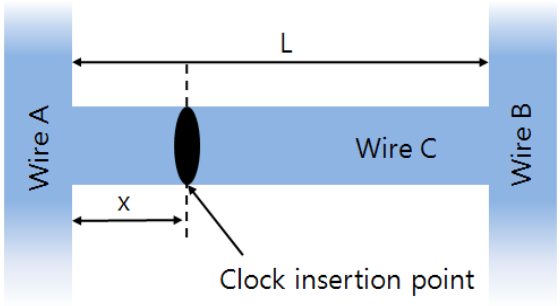

Fig. 2. Clock insertion point under non-uniform thermal profile

Consider the example of finding a clock insertion point shown in Fig. 2. Assuming the uniform temperature distribution, the clock insertion point insuring zero-skew point will be when $x = L/2$. However, if there is such a thermal gradient in a non-uniform temperature profile that the temperature in the path from wire C to wire A is higher than that from wire C to wire B, then the resistance in the former path becomes higher than that in the latter path, which differentiates delay times. Accordingly in Fig. 2, the clock insertion point *x* will be where $x < L/2$ to insure skew minimization, although the distances from *x* to A and from *x* to B are not same. Since the clock insertion point could be different depending on either uniform thermal distribution or non-uniform thermal distribution, clock insertion point has to be somewhere between two insert points to insure delay equalization.

A new balanced skew tree generation technique proposed in this paper is based on a modified DME algorithm. The original DME algorithm does not yield skew minimized design under non-uniform thermal profile with a temperature gradient since the center point of two nodes is not the zero skew point.

Therefore, this paper proposes the balanced skew tree generation technique for minimizing skew under non-uniform thermal profile with a thermal gradient.

III. Clock Routing Technique Guaranteeing Optimal Balanced Skew

This section introduces a new balanced skew tree generation technique. The proposed technique is based on the assumption that wire resistance increases as temperature.

Let two sink nodes are u and v. In Fig. 3 (a), zero-skew point (ZSP) of u and v under uniform thermal profile will be one point on line L which is the equi-distance line of u and v. The clock insertion point will be the point p which makes the shortest lines up to u and v.

However, ZSP will not be p under non-uniform profile since ZSP moves toward the higher temperature region. In Fig. 3 (a), ZSP is p under uniform thermal profile. However, when there is a temperature gradient under non-uniform thermal profile, ZSP moves toward v from p due to higher temperature near v.

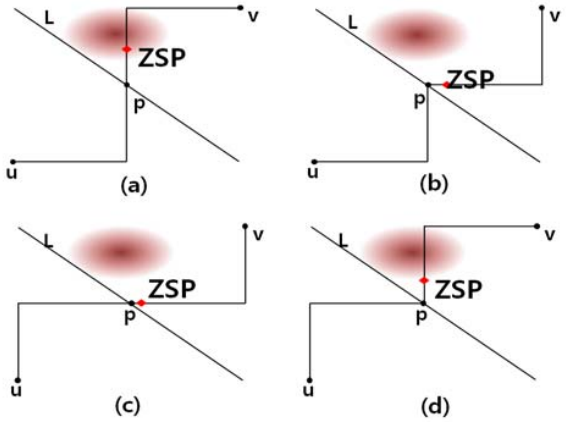

Fig. 3. Four ZSPs on sample interconnect structures

Figure 3 shows 4 ZSPs on sample interconnect structures. The top circles in the figure means a hot spot, p is the zero-skew point under uniform thermal profile, and ZSP is the zero-skew point under the worst temperature gradient condition between clock sink nodes, u and v.

In Fig. 3, it is seen that ZSP in Fig. 3 (a) is further away from p than those in other cases(Fig. (b), (c) and (d)) because the temperature difference between two paths from p to v and from p to u in Fig. 3 (a) is bigger than those in latter cases. The fact that ZSP in Fig.3 (c) is closer to point p than others can be explained likewise.

We describe a new balanced skew tree generation technique under non-uniform thermal profile based on four L-shaped structure in Fig. 3. Figure 4 is an example of generating ZSP with a new proposed technique for the case of Fig. 3 (a).

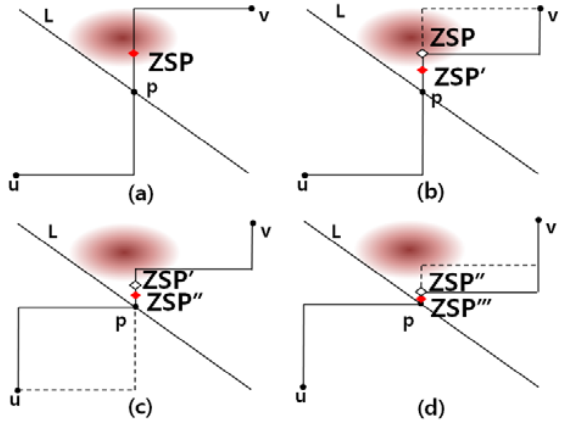

Fig. 4. Proposed generation method of balanced skew tree: Case 1

Figure 4 (a) shows both ZSP (under the worst thermal profile) and p (under the uniform thermal profile) on two L-shaped interconnects. It is shown that there is significant difference between p and ZSP because of temperature gradient. By moving ZSP toward p, we can reduce the worst clock skew and minimize the interconnect length change in routing.

As shown in Fig. 4 (b), the proposed technique moves the interconnect connected between first ZSP and sink node v into a region with lower temperature, the result of which yields new ZSP more close to p. To make ZSP and p more close, the opposite side of wire moves into a region with higher temperature, as shown in Fig. 4 (c). As a result, new ZSP is located closer to p since the temperature difference between two paths from p to v and from p to u has reduced. Then, this routing process can be iterated by moving the interconnect connecting ZSP' and v in Fig. 4 (c) into a region with lower temperature in order to make final ZSP and p even closer, which is illustrated in Fig. 4 (d).

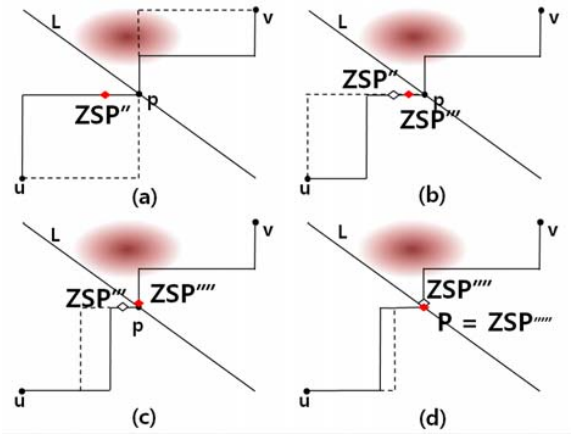

Fig. 5. Proposed generation method of balanced skew tree: Case 2

During the proposed routing process of Fig 4 (c), however, it might happen that ZSP' goes across the point p to the opposite side, as shown in Fig. 5 (a). In this case, if we follow the routing scheme as presented in Fig. 4 (d), ZSP would be getting further away from p. To keep this from happening, we change the routing of interconnect between p and u. As shown in Fig. 5 (b), we move a half of interconnect between p and u into a region with higher temperature, which makes new ZSP closer to p.

To make ZSP and p more closer, we try to move again the half of the modified routing into a region with higher temperature, as it is shown in Fig. 5 (c). By repeating this process, as illustrated in Fig. 5 (d), it is possible to make ZSP located closer to p.

The optimal balanced skew point becomes the equal delay point from each of four $ZSPs$ that are obtained from four interconnect structures under thermal profile and p which is ZSP under uniform thermal profile at each of Fig 3. Through a bottom-up approach, we find balanced skew points at an upper level based on the balanced skew points at a lower level. And then, we find balanced skew point based on these points at the top level.

By shifting ZSP to p as close as possible, we can get two advantages. First, the worst case clock skew has been minimized. Second, the skew under any operating temperature of chip confined to be in an allowable range, which means that we can design a clock routing robust to clock skew incurred by thermal gradient.

IV. Experiments and Results

A. Expression of temperature distribution using Elmore delay

VLSI systems of high performance have non-uniform thermal profile and will have various $T(x)$ as thermal profile. Namely, if the thermal profile of interconnect is expressed in a function, it could vary from a simple linear function to a higher-order functions or some transcendental function. Hence, we use the expression (2) in order to get zero-skew point in this paper since the function for $T(x)$ may be complex.

If we represent the temperature distribution of two nodes, A and B, in a non-uniform thermal profile, as shown in the example of Fig. 6, as $T(x)$, it can be expressed as the curve in Fig. 7.

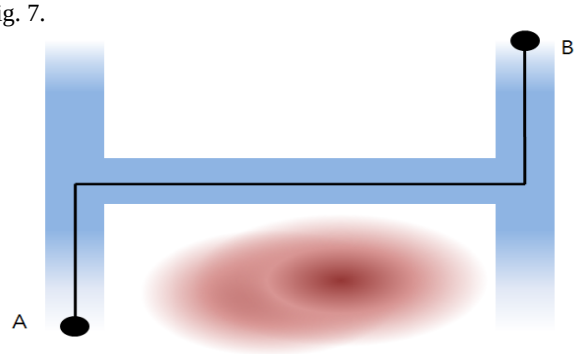

Fig. 6. Example of thermal profile on interconnect

Since it is difficult to express the above thermal profile in a simple equation, we obtain the zero-skew point using delays of each segment, which are found by dividing the section between A and B into N smaller subsections. As expressed in Fig. 7, delays of smaller sections are approximated as linear functions. The following expression indicates the above process.

$$Delay_{A-B} \approx \sum_{k=0}^{N-1} Delay_{K/N-K+1/N} \quad (4)$$

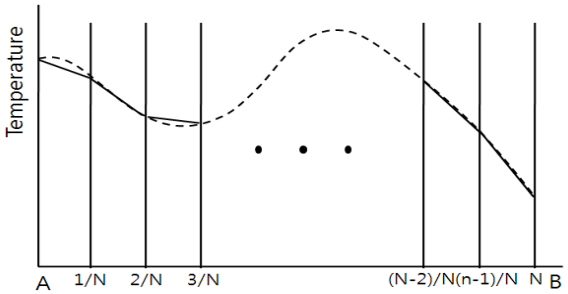

Fig. 7. **D**elay calculation **e**xample of thermal profile divided by N sub-sections

However, it is shown in Fig. 8 [4] that the interconnect delay variation depending on temperature increase is different as wire length varys. Therefore, sum of delays in divided small sections may not be same as the total delay, which prohibits the use of expression (4). In this paper, we use the adjusted *L* value in calculating the delay of small sub-sections, in order to solve this problem.

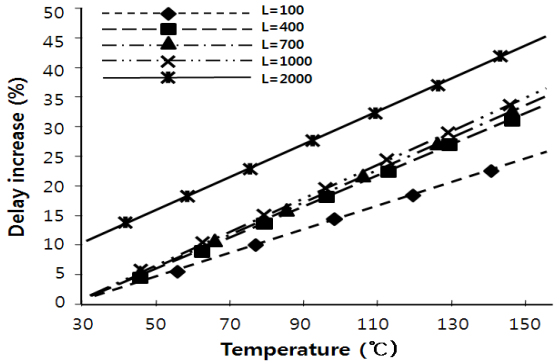

Fig. 8. Delay variation due to the temperature increase

Expression (5) is used in this paper to get the total delay using sum of N-sections.

$$D' = D_0 + \left[(c_0 L + C_L) r_0 \beta \left(\sum_{k=1}^{L} \int_k^{k+1} \left(\left((T(k+1) - T(k)) / (L/N) \right) \cdot k \right) + T(k) \right) dk \right) - c_0 r_0 \beta \left(\sum_{K=1}^{L} \int_k^{k+1} k \left(\left((T(k+1) - T(k)) / (L/N) \cdot k \right) + T(k) \right) dk \right) \right] \quad (5)$$

B. Performance Evaluation

We have implemented the proposed balanced skew tree generation technique using C language and evaluated the performance of the technique. The parameters used in all simulations are $r_0 = 0.03\Omega/um$, $c_0 = 2.0 \times 10^{-16} F/um$ and $\beta = 0.0068\,(1/℃)$.

For simulations, a square with 1000 micrometers on each side is modeled as 1000 by 1000 matrix. We have made an assumption that there are two clock sink nodes at top-right and bottom-left of Matrix. Due to this assumption, the distance between two nodes is 2000 micrometer because diagonal routing is not allowed. For a non-uniform thermal profile, we assigned an arbitrary point on the matrix to be in high temperature(170℃) and assumed that one block of matrix has a uniform temperature gradient.

Table I shows the experimental results of the proposed technique where we set temperature gradient as -0.02℃/block and the position of highest temperature is changed. We have measured the distance difference of *ZSP* between uniform and non-uniform thermal profiles and presented the reduced distance difference of *ZSP* after we apply proposed technique as the performance measure.

As shown in the Table I, it could be verified that *ZSP* under the worst-case thermal profile was approached to *ZSP* under uniform thermal profile over 54% on the average by applying the proposed technique in this paper. This result shows that the proposed technique yields higher performance than TACO proposed in [1].

We have measured the clock skew, before and after applying the technique. The left side of Table I represents the degree of proximity of two *ZSP s*, before and after applying the technique, and the right side of Table I shows the percentage of skew improvement after applying it.

We can verify that two *ZSP s* have been approximately over 55% more closer after applying the proposed technique compared to the case before. The skew value has also remarkably reduced, which means that the designed VLSI system can have higher clock frequency.

TALBE I THE PROXIMITY DIFFERENCE OF ZSPS AND SKEW DIFFERENCE BETWEEN BEFORE AND AFTER APPLYING THE PROPOSED TECHNIQUE

Coordinate of high temperature point		Distance gap of ZSPs (um)		Proximity degree of 2 ZSPs	Worst case skew before applying (ps)		Final skew (ps)	Percentage of skew improvement
X	Y	before	after		Delay	Skew	Skew	
100	0	22	3	86.36%	161.8	0.738	0.098	93.36%
200	0	25	7	72.00%	162.3	0.894	0.228	95.86%
200	100	22	5	77.27%	162.9	0.707	0.163	94.63%
300	0	30	3	90.00%	162.7	1.064	0.098	95.11%
300	100	26	6	76.92%	163.3	0.880	0.195	96.59%
300	200	19	5	73.68%	163.9	0.639	0.163	96.71%
400	0	37	8	78.38%	163.0	1.375	0.26	97.24%
400	100	31	4	87.10%	163.7	1.148	0.13	96.43%
400	200	24	5	79.17%	164.2	0.845	0.163	93.37%
400	300	16	4	75.00%	164.6	0.504	0.13	91.87%
500	0	49	20	59.18%	163.2	1.820	0.65	98.24%
500	100	42	17	59.52%	163.9	1.587	0.553	96.47%
500	200	34	13	61.76%	164.4	1.256	0.423	95.06%
500	300	24	8	66.67%	164.8	0.846	0.26	96.81%
500	400	13	2	84.62%	165.1	0.369	0.077	79.08%
600	0	59	34	41.38%	163.2	2.206	1.106	97.51%
600	100	52	32	38.46%	163.9	1.980	1.041	98.79%
600	200	44	29	34.09%	164.4	1.667	0.943	96.46%

600	300	35	24	31.43%	164.7	1.286	0.78	95.49%
700	0	66	49	27.27%	163.1	2.528	1.561	98.77%
700	100	60	46	23.33%	163.7	2.319	1.496	97.41%
700	200	52	44	15.38%	164.2	2.029	1.431	99.06%
800	0	72	60	16.67%	162.9	2.792	1.951	99.21%
800	100	69	60	11.76%	163.4	2.608	1.951	99.27%
900	0	79	70	10.26%	162.5	2.992	2.276	97.83%
Average				55.11%	Average			95.87%

V. Conclusion

In this paper, we have proposed a clock routing technique generating a balanced skew tree when temperature gradient exists in the chip. We have developed a technique finding the equi-delay point on interconnect under non-uniform thermal profile using the Elmore delay. For the performance evaluation of the proposed technique, we have implemented the technique using C language.

The experimental results show that the distance variance of clock insertion points with and without considering the temperature gradient can be lowered below 54% on the average after applying the proposed technique and the clock skew is remarkably decreased. If the proposed balanced skew tree technique is applied in clock routing, it is possible to improve operational reliability of chip by minimizing clock skew due to temperature gradient.

Acknowledgment

This work was supported by Seoul R&BD Program (10544).

References

[1] M. Cho, S. Ahmed, and D. Z. Pan, "TACO: temperature aware clock-tree optimization," in *Proc. ICCAD'05*, pp. 581-586, Nov. 2005.

[2] K, Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan, "Temperature-Aware Computer Systems: Opportunities and Challenges," *IEEE Micro*, Vol. 23, No.6, pp. 52-61, Nov-Dec 2003.

[3] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter Variation and Impact on Circuits and Microarchitectures," in *Proc. DAC-40*, pp. 338-342, Jun. 2003.

[4] K. Baneragee, A. H. Ajami, and M. Pedram, "Analysis and optimization of thermal issues in high-performance VLSI," in *Proc. Int. Symp. on Physical Design*, pp. 230-237, April 2001.

[5] O. Semenov, A. Vassighi, M. Sachdev, A. Kechavarzi, and C.F. Hawkins, "Burn-in temperature projections for deep sub-micron technologies," in *Proc.* ITC, pp. 719-226, 2003.

[6] *International Technology Roadmap for Semiconductors (ITRS) : Interconnect*, 2008.