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# A 3.125Gb/s Clock and Data Recovery Circuit Using 1/4-Rate Technique

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***Abstract*—**This paper describes the design and fabrication of a clock and data recovery circuit (CDR). We propose a new clock and data recovery which is based on a 1/4-rate frequency detector (QRFD). The proposed frequency detector helps reduce the VCO frequency and is thus advantageous for high speed application. The proposed frequency detector can achieve low jitter operation and extend the pull-in range without using the reference clock. The proposed CDR was implemented using a 1/4-rate bang-bang type phase detector (PD) and a ring voltage controlled oscillator (VCO). The CDR circuit has been fabricated in a standard 0.18 CMOS technology. It occupies an active area of 1 x 1 and consumes 90 mW from a single 1.8V supply.

***Keywords*—**Clock and Data Recovery (CDR), 1/4-rate frequency detector (QRFD), 1/4-rate phase detector.

## I. Introduction

IN recent years the clock and data recovery circuit plays a very important role in data network systems which require gigabit-speed serial data communication. In the receiver stage, one of the key blocks is the CDR which is used in a receiver to extract the clock needed for recovering the transmitted data.[1]

The loop bandwidth of CDRs should be small to improve the noise performance. However, it will result in a small capture range or pull-in range. CDRs without frequency acquisition loops might need either additional reference clock or off chip tuning. By using a frequency detector, the pull-in range can be extended and the acquisition time can be reduced without the reference clock. However, the conventional frequency detector is suitable for CDRs with a full-rate clock or a half-rate clock. Considering the power consumption and relaxed clock frequency, the quarter-rate CDRs can be a better alternative. [2]

This paper presents a CDR that has a 1/4-rate phase detector and 1/4-rate frequency detector using oversampling method without the reference clock.

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## II. Architecture

Fig.1 shows the architecture of the proposed 1/4-rate CDR circuit, consisting of a 1/4-rate bang-bang phase detector, a 1/4-rate frequency detector, charge pumps (CPs), a second-order Low Pass Filter (LPF), and a ring VCO. The proposed clock and data recovery circuit works similarly to the phase-locked loop (PLL). There is a difference between this CDR and an ordinary PLL. The difference is that this CDR has an additional frequency loop, so this CDR has wider acquisition range without the reference clock. It is an advantage because the VCO center frequency may vary considerably with process and temperature variations. [6]

Both the 1/4-rate PD and QRFD make comparisons using the multi-phase clocks of the VCO output. As a result, the PD and the FD generate Pup, Pdn, and Fup, Fdn signals which are used to control the CPs. The outputs of CPs, in turn, determine the input control voltage of the VCO through low-pass filtering that is provided by R, C1 and C2. [4]

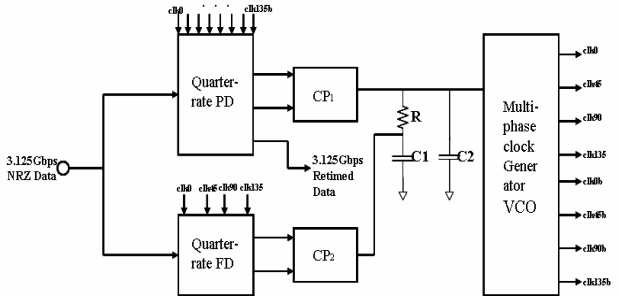



Fig. 1 The proposed 1/4-rate CDR circuit

## III. Circuit Implementation

### A. 1/4-rate Phase Detector

Fig. 2 shows the block diagram of the 1/4-rate bang- bang PD. It consists of eight D flip-flops (DFFs), eight XORs, and two MUXes. The PD uses eight-phase clocks of the VCO output to detect data transitions from the incoming NRZ data. The phase detector output is fed to the eight XORs. Through the two MUXes, the PD generates the final output signals. Fig. 3 illustrates the operation of the 1/4-rate bang-bang PD for the lock condition. If the CDR is in lock, the transition of the input non-return-to zero (NRZ) data coincides with clk0◦, clk0b, clk90◦, clk90b signals. If the transition of the input NRZ data occurs between the clk0◦ and clk45◦, the PD generates phase down (Pdn) signal. On the other hand, if the transition of the

input NRZ data occurs between the clk135b and clk0, PD generates phase up (Pup) signal. [3][5]

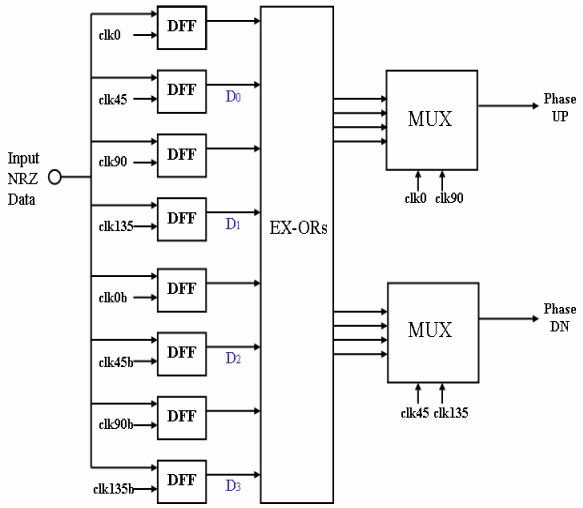



Fig. 2 The 1/4-rate bang-bang PD

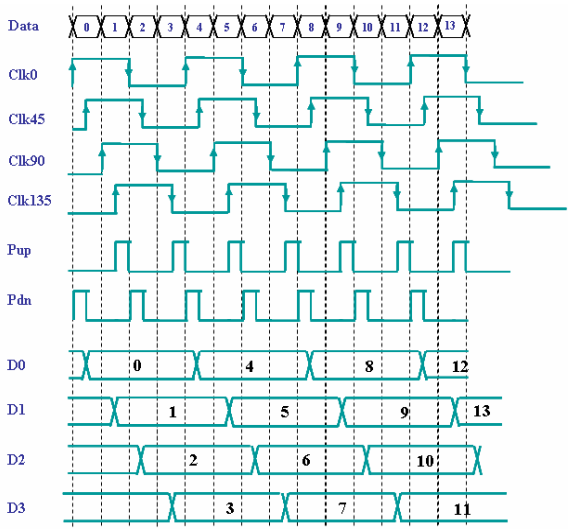
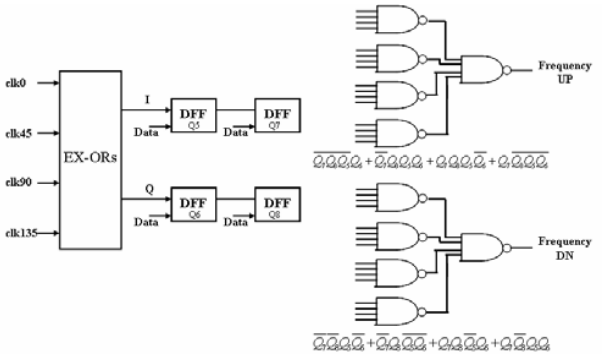



Fig. 3 The operation of the 1/4-rate bang-bang PD

### *B. The Proposed 1/4-rate Frequency Detector*

The proposed 1/4-rate frequency detector can be realized by two XORs, four DFFs, and combinational logic circuits, as shown in Fig. 4(a). The truth table for the combinational logic circuits in the proposed QRFD is shown in Fig. 4(b). The clocks of 0◦, 90◦ and 45◦, 135◦ are processed by the XORs to generate the new clocks I and Q. The new clocks are divided into four states, I, II, III and IV. In the proposed QRFD, four DFFs triggered by the input NRZ data will store the sampled values and record the states. For a slow periodic data as shown in Fig. 5(a), suppose that the first rising edge of the input NRZ data appears in state I and the next transition of the input NRZ data appears in state IV. This state transition indicates that the clock rate is higher than the input NRZ data rate. Then the FD generates Frequency down (Fdn) signal. For a fast periodic data as shown in Fig. 5(b), suppose that the first rising edge of the input NRZ data appears in state I and the next transition of the Input NRZ data appears in state II. This state transition indicates that the clock rate is lower than the input NRZ data rate. Then the FD generates frequency up (Fup) signal. [2]

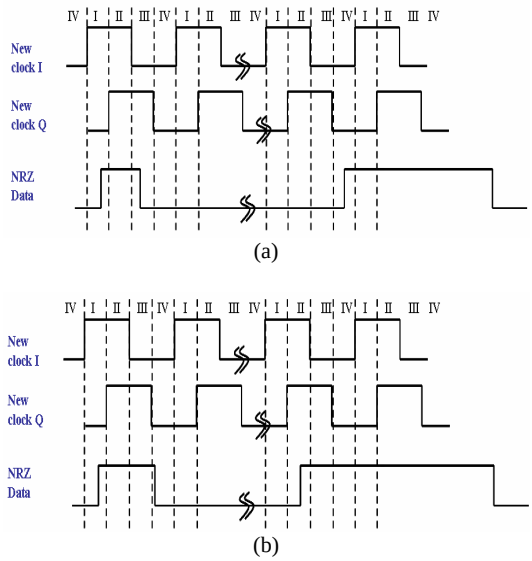



(a)

| Q5Q6 / Q7Q8 | State IV 00 | State III 01 | State II 11 | State I 10 |
|---|---|---|---|---|
| State IV 00 | | UP | | DN |
| State III 01 | DN | | UP | |
| State II 11 | | DN | | UP |
| State I 10 | UP | | DN | |

(b)

Fig. 4 (a) The schematic of 1/4-rate frequency detector. (b) The combinational logic circuits




(a)

(b)

Fig. 5 The timing diagram for (a) the state transition from state I to state IV (b) the state transition from state I to state II

## IV. Simulation Results

SPECTRE simulations of the proposed CDR circuit were conducted using the parameters of 0.18$\mu$m CMOS technology. Fig. 6 shows the clk0◦, clk45◦ and data waveform for the in-lock condition. Fig. 7 shows the simulation results for eye diagrams of the four 1:4 de-multiplexed 0.78-Gb/s data outputs for 3.125-Gb/s random input data. The peak-to-peak jitter for each of the four recovered output data is 60ps. Fig. 8 shows the simulation results for eye diagrams of the recovered clocks. The peak-to-peak jitter for each of the recovered clock is 37ps. Fig. 9 shows the chip layout. The whole chip occupies an area of 1 x 1mm$^2$. The measured results of the test chip would be available soon.

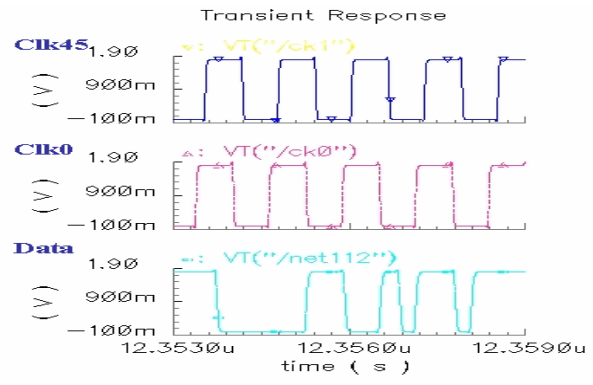



Fig. 6 The simulation results of CDR circuit

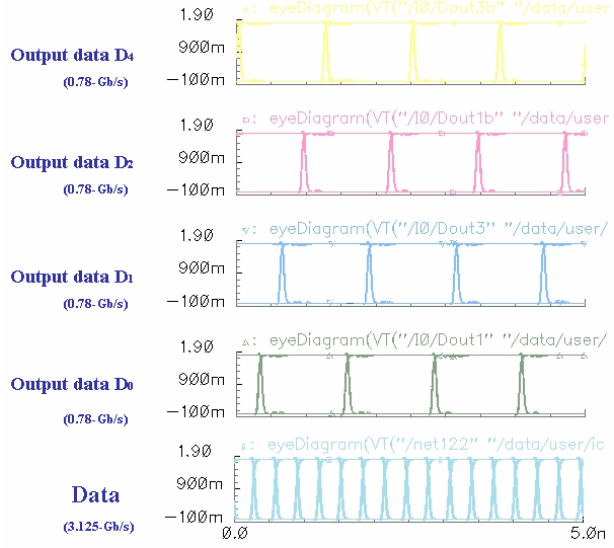



Fig. 7 The eye diagram of 3.125-Gb/s input and four 1:4 demultiplexed output

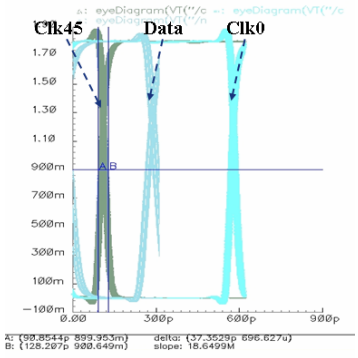



Fig. 8 The eye diagram of recovered clocks

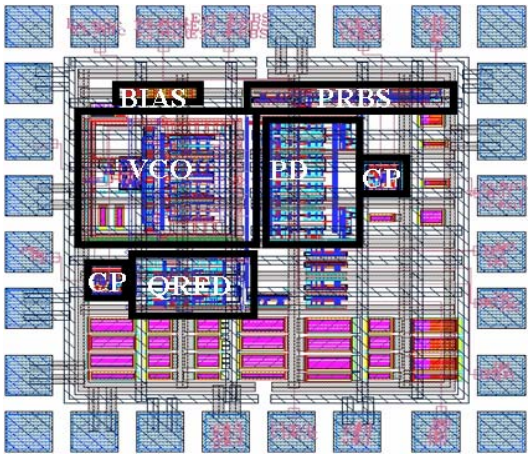



Fig. 9 The chip layout of the proposed CDR circuit

## V. Conclusion

The 3.125-Gbps CDR circuit incorporating the proposed 1/4-rate frequency detector has been realized in a 0.18$\mu$m CMOS technology. The simulation results show that, for the recovered data and clock, the peak-to-peak jitters were 60ps and 37ps, respectively. The chip power dissipation was 90mW from a single 1.8-V supply.

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