International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:2, No:6, 2008

A 1.5V,100MS/s,12-bit Current-Mode CMOS Sample-and-Hold Circuit

O. Hashemipour, and S. G. Nabavi

***Abstract*—**A high-linearity and high-speed current-mode sample-and-hold circuit is designed and simulated using a 0.25μm CMOS technology. This circuit design is based on low voltage and it utilizes a fully differential circuit. Due to the use of only two switches the switch related noise has been reduced. Signal - dependent -error is completely eliminated by a new zero voltage switching technique. The circuit has a linearity error equal to ±0.05μa, i.e. 12-bit accuracy with a ±160 μa differential output - input signal frequency of 5MHZ, and sampling frequency of 100 MHZ. Third harmonic is equal to −78dB.

***Keywords*—**Zero-voltage-technique, MOS-resistor, OTA, Feedback-resistor.

I. Introduction

SAMPLE and hold (S/H) Circuits are important block in data converter systems, such as the front end of A/d Converters. Up to present time, considerable numbers of circuits were designed for S/H in voltage and current mode. Recently more focus is on current-mode circuits due to high speed and low voltage supply in comparison with voltage-mode (switched-capacitor) circuits.

Unfortunately, charge injection error is the main problem of S/H circuits resulting in accuracy reduction of these circuits and hence the creation of non-linearity distortion.

A number of circuits were designed in order to improve either high-speed or high-accuracy [1, 2, 3, 5]. For example, the circuit in [3] which in is shown in Fig. 1, is a high accurate switched-current-memory-cell around 14-bit resolution using zero-voltage technique. In order to remove the signal-dependent-error a constant voltage is set at the sampling switch using a High-gain-opamp and a negative-feedback circuit. This design lacks the speed of operation due to gm considerations; however, it is one of the most accurate SI circuits.

In this work, with the aid of two simple OTA and two MOS-resistors a constant voltage on both sides of switches are generated during sample and hold mode resulting in complete removal of the signal-dependent-error and the offset-error part is also canceled out by using the fully-differential outputs.

Manuscript received September 27, 2006.

O. Hashemipour is with the Electrical and Computer Engineering Department of Shahid Beheshti University, Tehran, Iran (phone: 9821-29902273; e-mail: hashemipour@sbu.ac.ir).

S. G. Nabavi., is with, the Electrical and Computer Engineering Department of Azad University of Arak, Arak, Iran.

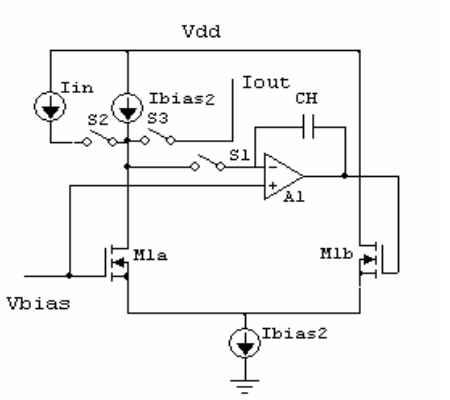

Fig. 1 SI circuit with zero-voltage-technique

II. Circuit Overview

The circuit block diagram is shown in Fig. 2. It constitutes a differential input stage and three simple OTAs, two Sampling switches and MOS-feedback-resistors. In sampling phase, after closing switches, differential input current between OTA-m in upper part and OTA-A, B is divided in K, and K´ ratio respectively. The current at the output nodes will be: $I_{out} = I_{in}$ and $I_{out'} = -I_{in}$. In holding phase the output currents will be equal to input currents. During both phases the two OTAs A and B will hold a constant voltage (V_G) at switches terminals. In order to eliminate the signal dependent error, active feed-back resistors are used for stabilization of V_G.

III. Complete Circuit Design

Fig. 3 shows the designed S/H circuit. It consists of transistors M_{3-5}, M_8, M_m and M_n for differential input stage , transistors M_{1-2}, M_{6-7}, and M_{9-10} for OTA - M , transistors $M_{11}, M_{c11}, M_{13}, M_{c13}, M_f$, and M_{f2} for OTA- A , transistors $M_{12}, M_{c12}, M_{14}, M_{c14}, M_h$ and M_{h2} for OTA –B, transistors M_{S1} and M_{S2} are sampling switches and finally M_{r1} and M_{r2} are MOS-resistors. Common mode feed back circuit is used in order to stabilize the common mode voltage of the fully differential opamp. During sampling mode while

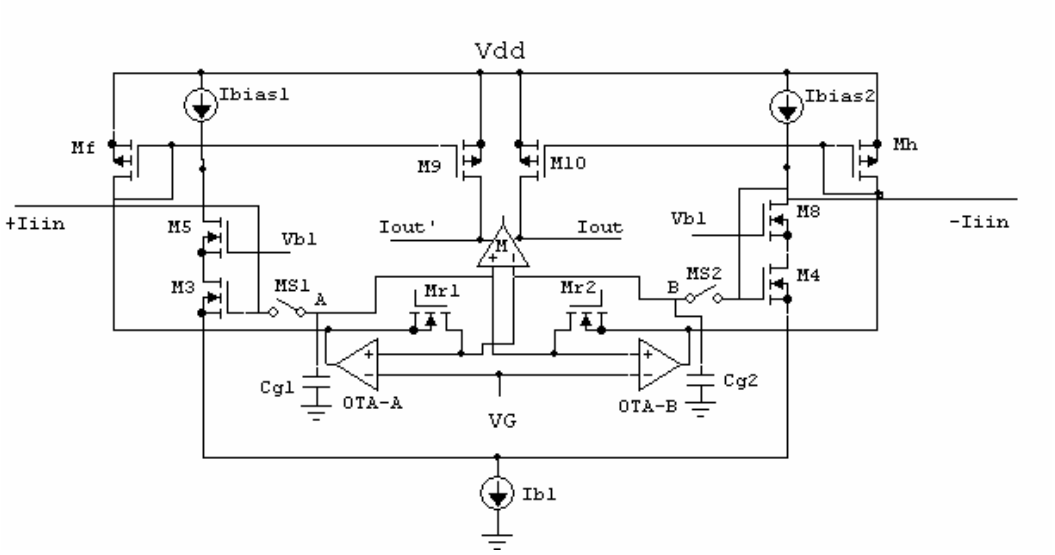

Fig. 2 Block diagram of current-mode S/H

switches M_{S1} and M_{S2} are closed, part of the input differential signal, $\pm K\,I_{in}$ will be at the outputs of OTA-M and the other part, $\pm K'I_{in}$ after inversion will be at outputs of OTA-A and OTA-B:

$$I_{out} = K'I_{in} + K\,I_{in} = (K + K')\,I_{in} \quad (1)$$

$$I_{out'} = -K'I_{in} - K\,I_{in} = -(K + K')\,I_{in} \quad (2)$$

For input and output currents to be equal:

$$K + K' = 1 \quad (3)$$

The dimensions of mm and mn are adjusted in order to satisfy (3). In this design the K and k´ factors are equal to 2/3 and 1/3 respectively and

$$(W/L)_{m,n} = (W/L)_{f,f2,h,h2,9,10} = 2/3(W/L)_{1,2,3,4}$$

in order to keep the circuit fully balanced.

A. Charge Injection Error Cancellation

Signal-dependent charge-injection arises when the voltage at a switch's sampling terminals varies with the signal level. To avoid signal-dependent-error , the voltage at the terminals of switch must remain at a constant level. In this work, due to fully balanced structure of the different stages during sampling period the voltage at $V_A = V_B = V_G$ is equal to the drain voltages of transistor M_{C11} and M_{C12}. During holding period the above voltages must be kept constant , However, practically open loop gain of the OTAs are not high enough to achieve this, and hence a feedback-resistors network is utilizing using two transistors M_{r1} and M_{r2} in order to provide constant voltage in node A and B. This is due to the fact that in holding mode voltage at input nodes are equal to drain voltage of the transistors M_{C11}, M_{C12} and voltage and bias voltage V_G , therefore, using large feedback-resistors from drain of M_{C11} and M_{C12} to nodes A and B, the voltage level of these nodes will be equal to V_G. This means nodes A and B are virtual ground and therefore during sample and hold mode the terminal voltages of switches are constant and equal to V_G, thus error is independent of input signal.

B. Speed of Circuit

Time-constant in basic SI circuits is equal to $\tau \approx (C_{g/}g_m)$. In order for speed to be increased, gm must be increased, i.e. increase the bias-current. This of course will result in an increase in both noise and power dissipation. In this work, the speed improvement of the circuit is achieved by using high-speed OTAs and small memory capacitors C_{g1} and C_{g2}. Moreover, diode connected loads are used instead of current sources in order to increase g_m, the time constant is now:

$$\tau \approx C_{g/}\,(g_{m3} + g_{mn}) \quad (4)$$

Diode connected loads will also result in a decrease in the input impedance of the circuit, from typical value of $1/g_m$ in basic SI to $1/(g_{m3} + g_{mn})$ in this work. Lower input impedance will results in a decrease in distortion.

IV. Simulation Results

The proposed S/H circuit has been designed and simulated using Hspice and the 0.25μm CMOS technology and input-signal-frequency of 5MHz in full-scale mode. The full-scale value of the input current is ±80μa with a sampling frequency of 100MHz. Fig. 4 shows the differential sinusoidal current

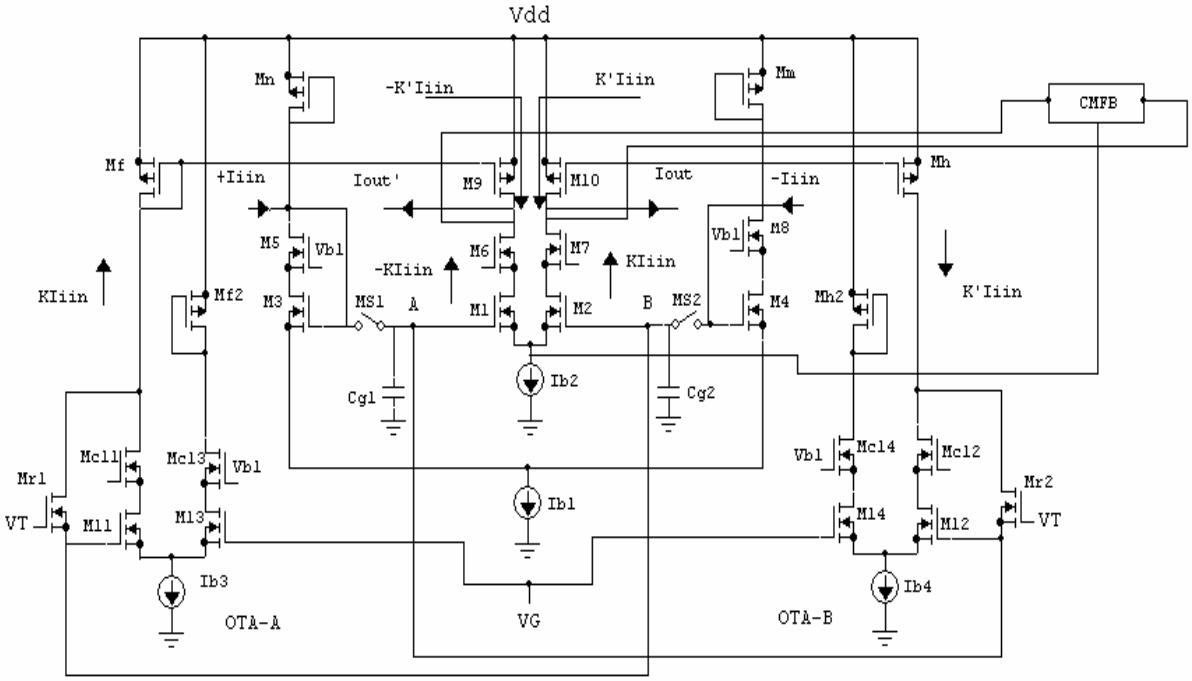

Fig. 3 Complete sample and hold circuit

output. The biasing current is 300μa and the hold-capacitors C_{g1} and C_{g2} are 0.26pf. The supply voltage Vdd is 1.5V and the power-dissipation of the circuit is 2.5mW. The differential current output is ±160μa. Simulation results from a triangular input signal with 5MHz frequency and ±80μa range, measurements shown in Fig. 5 results in a linearity-error of about 0.05μa. This much error is equal to 12-Bit resolution for an S/H circuit.

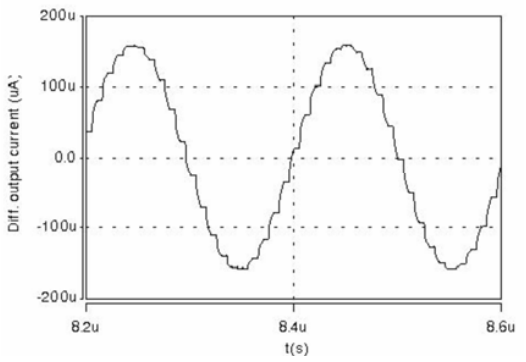

Fig. 4 Differential output current

The total-harmonic-distortion is extracted using PSD output waveform and FFT-method as in [4]. Fig. 6 shows the PSD waveform which results in a 3rd harmonic of less than −78dB. The FFT simulation is performed by using sinusoidal-input signal frequency of 4.88MHz, and a sampling frequency of 100MHz. As shown in Fig. 7 simulation was performed for different input frequency range of 1.22 MHz to 8.544 MHz and the results shows a resolution of 12-Bit under all conditions. Table I shows a summary of the performance of the designed S/H circuit.

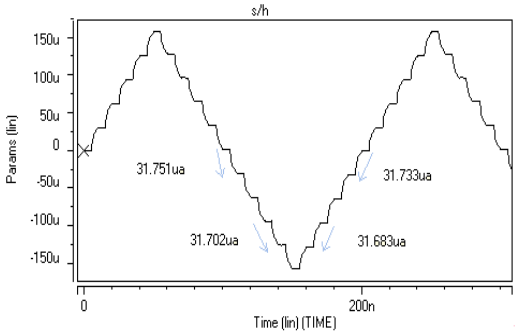

Fig. 5 Triangular output signal for linearity-error Measurement

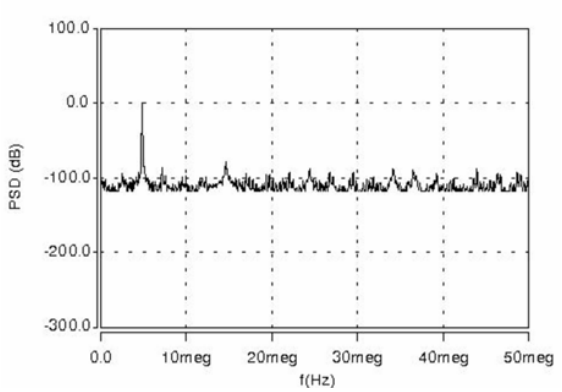

Fig. 6 PSD waveform of sinusoidal response of S/H circuit

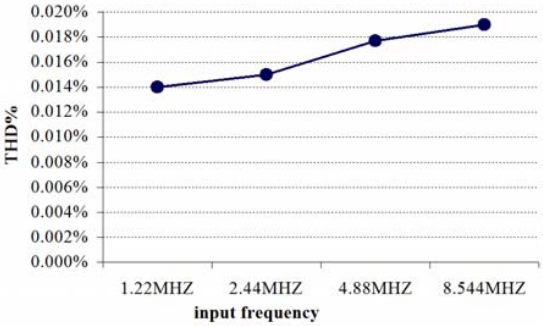

Fig. 7 THD% versus Input-frequency

TABLE I
SUMMARY OF SIMULATION RESULTS

Technology	0.25um CMOS
Supply voltage	1.5V
Power dissipation	2.5Mw
HD3 @ 100MHz-clock & 4.88MHz input frequency	-78dB
Differential input range	± 80ua
Differential output @ iout-iout′	±160ua
Linearity error	±0.05ua
Sampling frequency	100MHz
Input frequency linearity error measurement	5MHz
Resolution	12-Bit
Acquisition time	2ns
3dB bandwidth	178MHz

VII. CONCLUSION

A high-linearity, low-voltage and high-speed current-mode sample-and-hold circuit has been designed. This circuit design is based on low supply voltage at 1.5V and it utilizes a fully differential circuit. Signal - dependent -error is completely eliminated by a new zero voltage switching technique. The circuit has been simulated using a 0.25µm CMOS technology. The circuit has a linearity error equal to ±0.05µa ,i.e. 12-bit accuracy with a ±160 µa differential output ,input signal frequency of 5MHZ , and sampling frequency of 100 MHZ. Third harmonic is equal to –78dB. The measured power-dissipation at 1.5V supply-voltage is 2.5mW.

The hold-settling-time and acquisition time are calculated approximately 1.1ns and 2ns.

The presented S/H circuit is suitable for SI systems requiring precise sample-and-hold circuit.

REFERENCES

[1] Yasuhiro Sugimoto, “A 1.5-V Current -Mode CMOSsample-and-Hold IC With 57-dB S=Nat 20 MS/s and 54-dB S=N at 30 MS/s” IEEE J. OF Solid-State Circuts, vol. 36, no. 4, Apr. 2001.
[2] X. Hu and K.W. Martin, “A switched-current sample-and-hold circuit” IEEE J. Solid State Circuits, vol. 32 , pp.898–904, June 1997.
[3] D. Nairn, “Zero-Voltage Switching in Switched-Current Circuits”, IEEE Int.Symp. on Circuits and Systems, 1994, pp. 289-292.
[4] P. J. Crawley and G. W. Roberts, “Predicting harmonic distortion in switched- current memory circuits”, IEEE trans.on Circuits and Systems II: Analog and Digital Signal Processing, vol. 41, No. 2, pp. 73-86, Feb. 1994.
[5] H. Yang, T. Fiez, and D. Allstot, “Current-feedthrough effects and cancellation technique in switched-current circuits” In IEEE Int. Symp. Circuits and systems, 1990, PP.3186-3188.