International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:11, No:4, 2017

0.13-μm Complementary Metal-Oxide Semiconductor Vector Modulator for Beamforming System

J. S. Kim

***Abstract*—**This paper presents a 0.13-μm Complementary Metal-Oxide Semiconductor (CMOS) vector modulator for beamforming system. The vector modulator features a 360° phase and gain range of -10 dB to 10 dB with a root mean square phase and amplitude error of only 2.2° and 0.45 dB, respectively. These features make it a suitable for wireless backhaul system in the 5 GHz industrial, scientific, and medical (ISM) bands. It draws a current of 20.4 mA from a 1.2 V supply. The total chip size is 1.87x1.34 mm².

***Keywords*—**CMOS, vector modulator, beamforming, wireless backhaul, ISM.

I. Introduction

HIGH-SPEED data rate is necessary in order to comply with the requirements of advanced services. However, with higher frequencies, higher data rate, and higher user density, multipath fading and cross-interface become serious problems, resulting in the degradation of bit error rate solve these issues.

Achieving higher communication and beamforming capability have proven to be very effective in suppression of the interference and multipath signals [1]. In addition, due to steerable directional antenna patterns and high directivity, beamforming system is applied to the non-line of sight (NLoS) wireless backhaul systems for point to multi-point (P-to-MP) [2]. However, additional phase shifters are required for implementing the beamforming system, and their phase errors play a major beamforming performance role.

Vector modulator can be designed using passive or active method. Passive phase shifters, such as switched-line networks, loaded-line networks, reflective-type phase shifters, switched-filter phase shifters, etc. [3]-[6], have advantages of low power and high linearity, but are not normally used in beamforming receiver because of high insertion losses (IL), high noise figure (NF), and large area on chip. On the other hand, active phase shifters, such as vector modulators [7], have higher gain and higher phase shift resolution, and smaller area on chip.

Another publication [8] showed a CMOS vector modulator only being able to steer the phase of the vector. As shown in Fig. 1, both in-phase (I-) and quadrature-phase (Q-) signal amplitudes are controlled by following I-path and Q-path variable gain amplifiers (VGAs), and I-, Q- vector are added through a combiner. In order to shift accurate phase, I-path and Q-path outputs should be exact 90-˚shift and equal amplitude. Furthermore, I-path and Q-path VGAs need to be matched well because gain mismatches lead directly combiner output phase mismatches. For high frequency vector modulator, many researches focus on improving linear phase shifting, but neglect the in-phase/quadrature-phase (IQ) signal amplitude mismatch. However, the phase error due to IQ amplitude mismatch must be concerned carefully [9]-[11].

This paper is organized as follows. In Section II, the proposed system architecture is presented and its operating principle is explained and analyzed in detail. In Section III, the design of proposed vector modulator for beamforming system is addressed. In Section IV, the results of experimental characterizations are reported.

J. S. Kim is with the Korea Electronics Technology Institute, Gyung-gi, Seongnam-si, South Korea (phone: +82-31-789-7220, fax: +82-31-789-7259, e-mail: kim812@ keti.re.kr).

II. System Architecture

The system architecture of the conventional vector modulator is shown in Fig. 1. A differential input signal is split into quadrature phased I- and Q-signals using a quadrature all-pass filter (QAF). The conventional QAF is based on L-C series resonators. In this paper, proposed vector modulator is used Q-factor calibration circuit for reducing phase error and amplitude mismatch, which will be discussed in detail in the next section. The QAF provides differential I- and Q-components at its output. The variable gain amplifiers (VGA) is conventionally composed of two Gilbert-cell types. It adds the I- and Q-inputs from the QAF with proper amplitude weights and polarities. The selected orthogonal vectors are added together by a combiner.

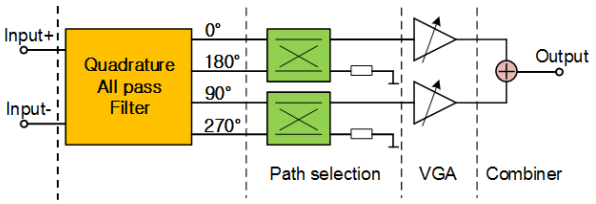
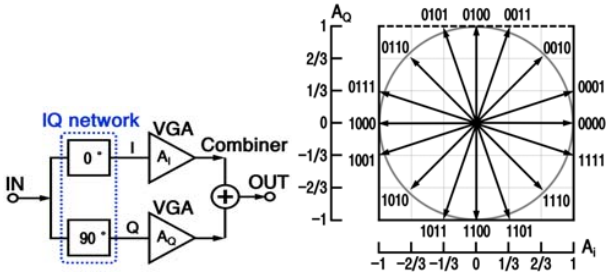


Fig. 1 System architecture of the conventional vector modulator

Fig. 2 shows block and phase shifting diagram of the vector modulator active phase shifter. The IQ network generates I- and Q- signal, and they are weighted by following VGAs gain. For example, for the case of 4-bit full-360˚ phase shifter, gain ratio of VGAs in I-path or Q-path (A_Q/A_I) can be selected to -1, -2/3, -1/3, 0, 1/3, 2/3, 1. It is possible to select any phase form 0 – 360˚ with 22.5˚ step as shown in Fig. 2 (b). Output phases

heavily depend on the amplitude weightings of I- and Q-phase inputs. Therefore, output phase error of vector modulator is sensitive to amplitude mismatch and phase mismatch of IQ signal.



(a) (b)

Fig. 2 (a) Block diagram of the vector modulator, (b) Phase shifting diagram through VGAs gain control

III. Circuit Design

A. IQ Network

Conventionally, the multistage R-C based IQ network has been widely used due to its wide operation bandwidth. However, R-C based IQ network has significant insertion loss caused by number of stage for wideband. Consequently, R-C IQ networks are not suitable for RF input signal phase shifting because of bad noise figure (NF). In this work, a polyphase filter topology by using L-C resonance network was chosen that provides best device matching performance regarding the desired quadrature angle. In order to overcome PVT variations and get accurate IQ network, Q-factor calibration circuit is operated by two-stages: The first stage is to find C value for center frequency, and the second stage is to find R value for Q-factor = 1.

Fig. 3 shows C-bank controller to find proper capacitance. The C-bank controller compares on-chip LC time-constant with off-chip LC time-constant. If on-chip LC time-constant is longer than off-chip LC time-constant, the next smaller capacitance among the C-bank's capacitances is selected to reduce LC time-constant. The simulation results are shown in Figs. 4 (a) and (b).

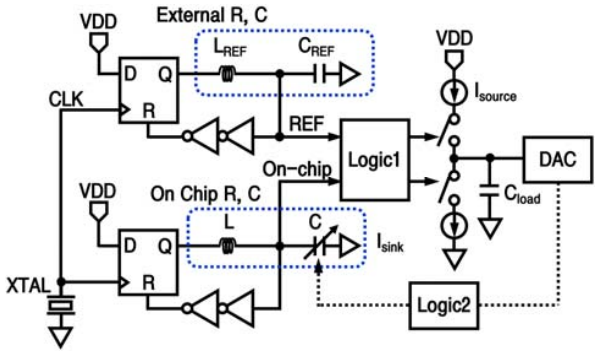
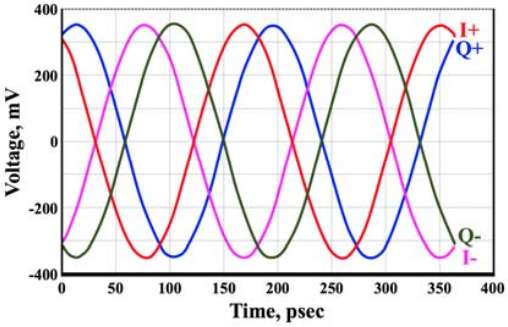
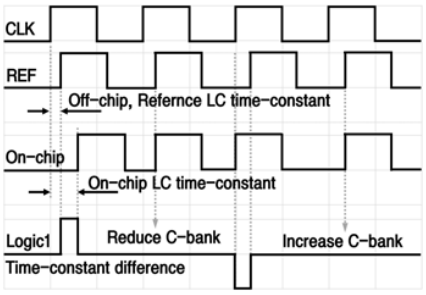


Fig. 3 IQ network with calibration circuits



(a) Simulation result of IQ network



(b) LC time-constant

Fig. 4 Simulation results of IQ network

B. Variable Gain Amplifier

The VGAs are designed with respect to a constant output phase over gain in order to achieve a precise gain control of the quadrature signal vectors. The voltage gain is controlled by 5-bit voltage regulator outputs from resistance ladder. The voltage gain range is 0 – 10-dB with 0.3-dB gain step. Phase shifting resolution is 2.8-˚ in 0 – 90-˚ range. In order to obtain full–360-˚ phase shifting, voltage regulator has auxiliary control bit for VGA's negative gain. If both I- and Q-path VGAs have negative gain, vector modulator change the phase in 180 – 270˚. Otherwise, in case of only one signal of I- or Q-path has negative gain, phase shift results in 90 – 180˚ or 270 – 360˚. Fig. 5 shows applied variable gain amplifier topology.

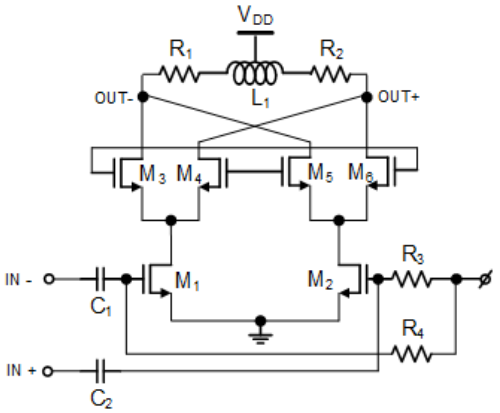


Fig. 5 Variable gain amplifier topology

The VGAs in vector modulator I-path and Q-path are designed using general Gilbert-cell topology. Fig. 6 shows the simulated result of VGA gain.

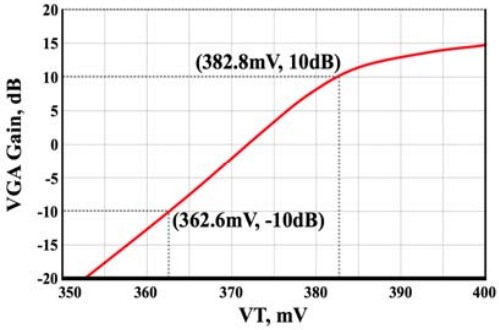


Fig. 6 Simulation result of VGA gain

The complete monolithic circuit was designed using a 0.13 -μm technology. The core size without pads is 1.47x0.75 mm². The designed chip layout is shown in Fig. 7.

The vector modulator features a 360 ° phase and gain range of -10 dB to 10 dB with a root mean square attenuation and phase error of only 3.0 ° and 0.3 dB, respectively. Figs. 8 and 9 show the simulation results.

IV. Experimental Results

The vector modulator is realized in TSMC 0.13–µm on-poly eight-metal (1P8M) CMOS technology. The die size of the proposed vector modulator is 1,873 µm × 1,340 µm shown in Fig. 10. The vector modulator is measured chip-on-board with external balun for differential signal outputs. Figs. 11-13 show the measured results at around 5 – 6 GHz. Fig. 11 shows the characteristics of phase shift vs. frequency in 64 states (6-bit). The Route Mean Square (RMS) amplitude and phase error of the vector modulator when varying the control voltages are shown in Figs. 12 and 13.

The measured RMS amplitude error stays in the same error bound of 0.45 dB. Also, the measured RMS phase error stays in the same error bound of 2.2°. The unit phase step is 2.6°, and the maximum phase difference is 1.7° at 44.95°.

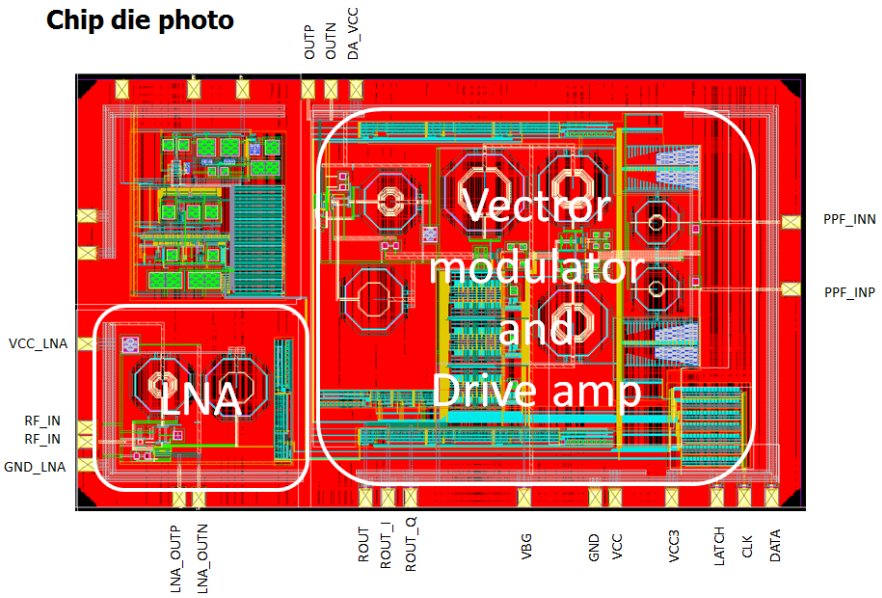


Fig. 7 Layout of vector modulator

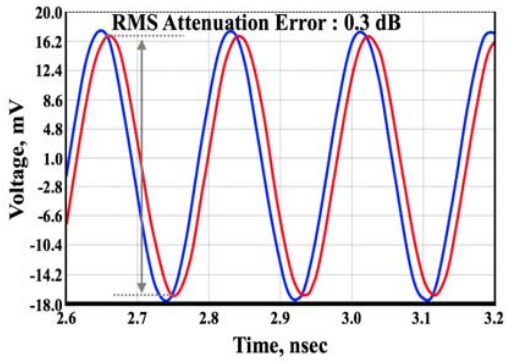


Fig. 8 Simulation result of RMS attenuation error

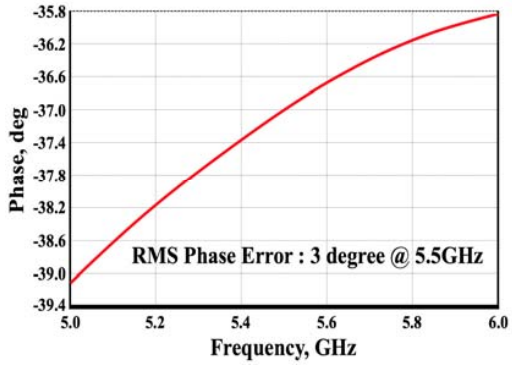


Fig. 9 Simulation result of RMS phase error

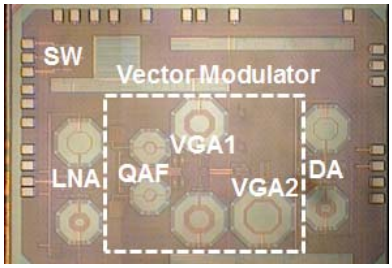


Fig. 10 Fabricated vector modulator

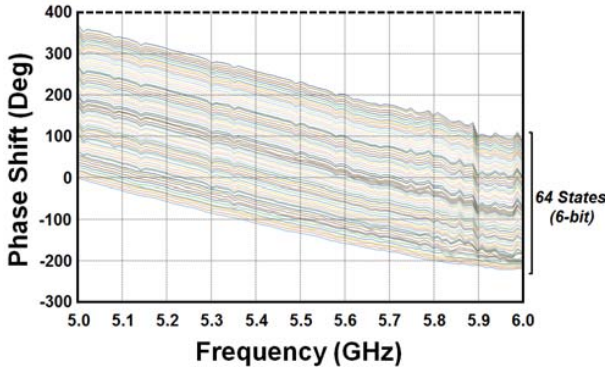


Fig. 11 Measured result of phase shift vs. frequency

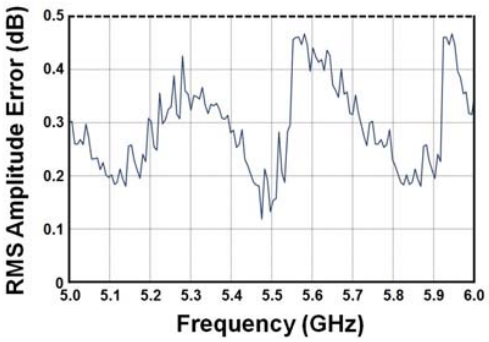


Fig. 12 Measured result of RMS amplitude error

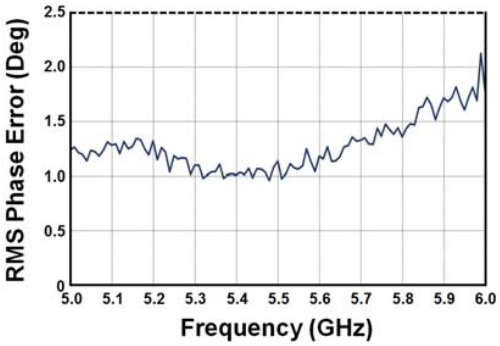


Fig. 13 Measured result of RMS phase error

V. Conclusion

This paper reports the design of vector modulator based on 802.11ac suitable for beamforming system. The measured characteristics are well matched with simulations. The core size of the integrated vector modulator is 1.47x0.75 mm². The proposed CMOS vector modulator is good candidates for integrated beamforming systems.

Acknowledgment

This work was supported by Institute for Information & communications Technology Promotion (IITP) grant funded by the Korea government (MSIP) (No. B0190-16-2003, The Development of Gigabit Wireless Backhaul System with Long Distance in Unlicensed Band)

References

[1] S. S. Jeon, Y. Wang, Y. Qian, T. Itoh, "A novel smart antenna system implementation for broad-band wireless communications", *IEEE Trans. Antennas Propag.*, vol. 50, no. 5, pp. 600-606, May 2002.

[2] G. Caire, S. Shamai, "On the achievable throughput of a multiantenna Gaussian broadcast channel," *IEEE Trans. Inf. Theory*, vol. 49, pp.1691-1706, 2003.

[3] H. Huang, C. B. Papadias, S. Venkatesan, MIMO Communication for cellular Networks. Springer, 2012.

[4] A. Hajimiri, H. Hashemi, A. Natarajan, X. Guan, and A. Komijani, "Integrated phased array systems in silicon", Proceedings of IEEE, vol. 93, no. 9, pp. 1637–1655, 2005.

[5] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity", IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2515–2524, 2005.

[6] F. Ellinger, R. Vogt, and W. Bächtold, "A high yield ultra small passive vector modulator based phase shifter for smart antenna combining at C-band", *IEEE/CSIRO Asia Pacific Microwave Conference*, pp. 794–797, Dec. 2000.

[7] F. Ellinger, U. Lott, and W. Bächtold, "An antenna diversity MMIC vector modulator for HIPERLAN with low power consumption and calibration capability", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 964– 969, May 2001.

[8] K.-J. Koh and G. M. Rebeiz, "0.13 µm CMOS phase shifters for X-, Ku-, and K-band phased arrays", *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2535-2545, Nov. 2007.

[9] F. V. D. Bogaart and R. Pyndiah, "A 10-14 GHz linear MMIC vector modulator with less than 0.1 dB and 0.8 amplitude and phase error", *IEEE MTT-S Digest*, pp. 465–468, 1990.

[10] J. Grajal, J. Gismero, M. Mahfoudi, and F. A. Petz, "A 1.4- 2.7 GHz analog MMIC vector modulator for a crossbar beamforming network", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 1705–1714, Oct. 1997.

[11] S. Kim, D. Kang, K. Koh, and G. M. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," IEEE Trans. on MTT, Vol. 60, No. 11, pp. 3434-3439, Nov. 2012.