International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:13, No:3, 2019

An Active Rectifier with Time-Domain Delay Compensation to Enhance the Power Conversion Efficiency

Shao-Ku Kao

Abstract**—**This paper presents an active rectifier with time-domain delay compensation to enhance the efficiency. A delay calibration circuit is designed to convert delay time to voltage and adaptive control on/off delay in variable input voltage. This circuit is designed in 0.18 μm CMOS process. The input voltage range is from 2 V to 3.6 V with the output voltage from 1.8 V to 3.4 V. The efficiency can maintain more than 85% when the load from 50 Ω ~ 1500 Ω for 3.6 V input voltage. The maximum efficiency is 92.4 % at output power to be 38.6 mW for 3.6 V input voltage.

Keywords**—**Wireless power transfer, active diode, delay compensation, time to voltage converter, PCE.

I. Introduction

IN modern age, various wireless technologies play an important role in our day-to-day life, especially in wireless power transfer (WPT) system. It is widely used in implantable medical devices (IMDs) such as pacemakers [1], neural recording implants [2], cochlear [3], and retinal prostheses [4]. For these implants, a long-term reliable battery is also implanted. Beside this, IoT node can also be powered by WPT [5]. The WTP system is shown in Fig. 1. In the receiver side, the received AC voltage is firstly converted to a DC voltage by the active rectifier [6]-[10]. The power conversion efficiency of active rectifier plays an important role in wireless power transmission system. The wireless power transmission system is applied in implantable medical products and many portable electrical devices. It can get rid of the limitation of line and reduce the size of device. In addition, wireless power transmission system replaced the traditional way to charge IMD.

In order to improve the power conversion efficiency of wireless power transmission system over wide input voltage range. The active rectifier with synchronous switches is shown in Fig. 2 (a). If the signal V_{GN1} and V_{GN2} drives M_{N1} and M_{N2} in incorrect time, the on and off propagation delay time of the comparator and buffer course the power transistor (M_{N1} and M_{N2}) to turn on and off at incorrect time.

For the ON propagation delay, it leads to decrease the charge time of rectifier. For OFF propagation delay, it induces reverse leakage current on the power MOS. In Fig. 2 (b), it shows the simulation result of the reverse current. So, it is crucial to solve the on/off propagation delay problem, even the delay time varied by input voltage. Until now, many kinds of circuit for compensating have been proposed [9], [10]. In this work [9], both Vac and Vss are fed to the error amplifier (EA) for comparison. The error voltage controls the inject current to the push-pull comparator use to compensation the delay. As the feedback loop is stable, it can generate a reference voltage to set the offset current. In [10], the feedback amplifier OTA is replaced the error amplifier. In this work, it is implemented with a control logic circuit to control the timing of the comparison. For both EA and OTA, it is very slow, and it costs many input cycles to calibrate correct voltage.

A delay calibration circuit is proposed to convert the delay time to voltage and adaptive track the on/off delay time in variable input voltage. This technique can effectively overcome the problem of varied delay time in different input voltage. The advantages of our circuits are with high resolution for accuracy compensated delay time without using EA and OTA. It can generate desired duty cycle to turn on/off the power MOS. The proposed active rectifier circuit is discussed in section II. The HSPICE simulation results are illustrated in section III. Section IV gives the conclusion.

II. Proposed Active Rectifier

As shown in Fig. 3, V_{AC1} and V_{AC2} are the input of rectifiers from receiver coupling inductor V_{AC}. The signal of V_{AC1} and V_{AC2} controls the four of power MOS. When $V_{AC1} > V_{AC2}$, comparator Cmp_2 will deliver high signal to turn on M_{N2}, and the current pass through M_{P1} to charge the output capacitance C_L. During another half cycle, $VAC_2 > V_{AC1}$ the M_{N2} and M_{P1} will turn off and the M_{N1} and M_{P2} turn on to continue to charge rectifier output. However, as the comparators output pass through the buffer to drive the power NMOS transistors, the buffer will generate delay time to turn on/off M_{N1} and M_{N2}. The turn on delay time reduces the charge time of rectifier. The turn off delay time leads to a reverse current problem. These delay problems may waste the power of rectifier. The delay calibration circuit is proposed to compensate the on/off delay time.

Shao-Ku Kao is with the Department of Electrical Engineering and Green Technology Research center, School of Electrical and Computer Engineering, College of Engineering, Chang Gung University, Taoyuan City, Taiwan (e-mail: kaosk@mail.cgu.edu.tw).

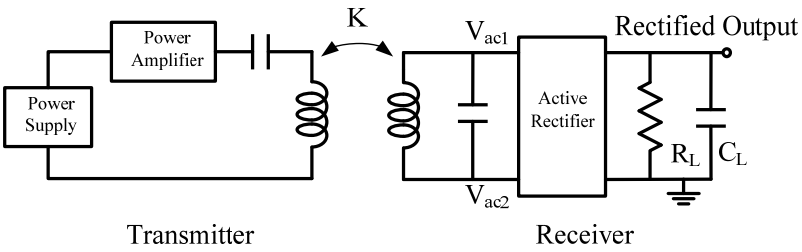
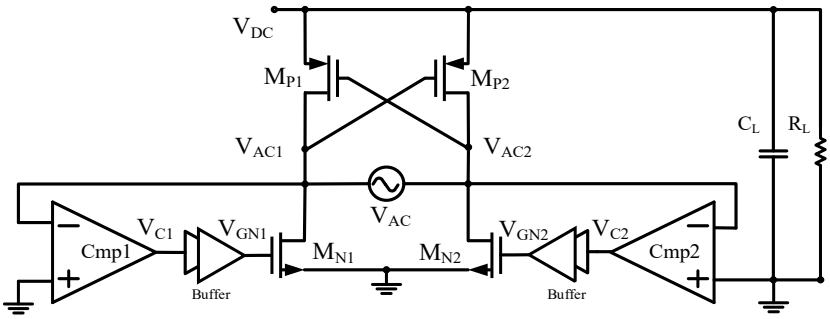
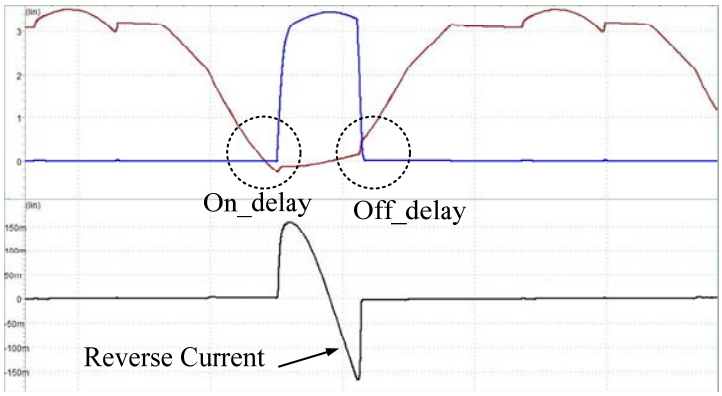


Fig. 1 WPT system



(a)



(b)

Fig. 2 (a) Active rectifier without delay calibration circuit (b) Reverse current problem

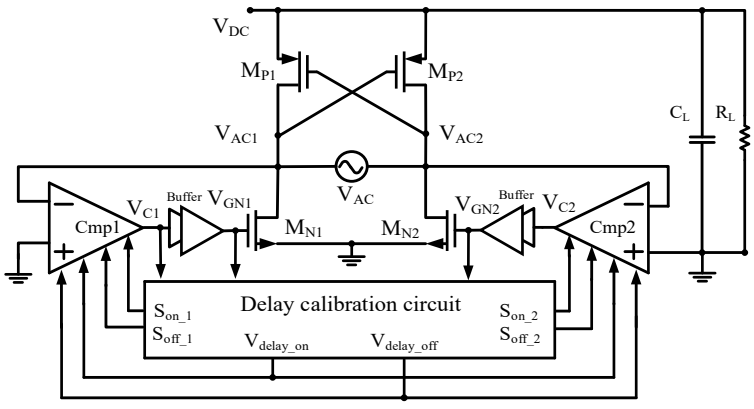


Fig. 3 Active rectifier with proposed delay calibration circuit

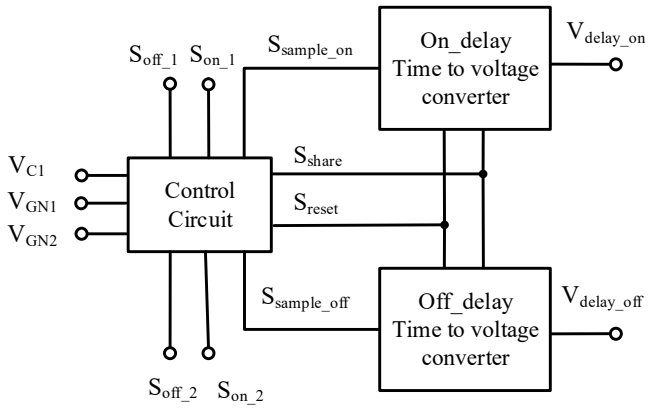


Fig. 4 Delay calibration circuit

As shown in Fig. 4, the proposed delay calibration circuit consists of two time to voltage converters (TVC) and control circuit. The operation of the delay compensation is described as follows. The proposed circuit detects the delay time between the V_{C1} and V_{GN1} or V_{C2} and $V_{GN2.}$ The signal S_{sample_on} is generated by the adjacent rising edge between V_{C1} and V_{GN1}. The adjacent falling edge between V_{C1} and V_{GN1} is generated signal, $S_{sample\_off.}$ Those delay times are converted by two TVC and generated two voltages V_{delay_on} and V_{delay_off}, respectively. The voltages of the V_{delay_on} and V_{delay_off} depend on pulsewidth of signal, S_{sample_on} and S_{sample_off}. To generate the output voltage, V_{delay_on} and V_{delay_off}, the TVC needs control signals from the control circuit, as shown in Fig. 4. The control signals used to control the operation of TVC including S_{sample_on}, S_{sample_off}, S_{share} and S_{reset}. Besides this, each comparator requires two signals, S_{on} and S_{off} to turn on and turn off the extra delay time for comparator.

A. Time to Voltage Converter Circuit

As shown in Fig. 5, this circuit is converted the pulsewidth to form a specific voltage. The voltage is able to control the offset of the comparator in the active rectifier. The timing diagram of delay calibration circuit is shown in Fig. 6. In Fig. 6, it only presents the timing diagram to compensate the delay in off delay time. The on-delay time is the same structure circuit and operation procedure, but input signal is the S_{sample_on}.

The operation of time to voltage converter circuit is divided into three steps. The first step, the signal S_{sample_off} switchs on the M2 and chargs the capacitor, C_1 for the time caused by delay of buffer. The pulse width of the S_{sample_off} is the phase difference between falling edge of V_{C1} and falling edge of V_{GN1}. When M_2 is on, the voltage of V_{sample} is charged. The second step, the charging sharing between two capacitors, C_1 and C_2, the voltage V_{delay_off} is charged up. It is controlled by the signal S_{share}. The third step, the voltage of V_{sample} is discharging by the signal S_{reset} to a zero voltage. Those steps repeat itself and generated a stable voltage V_{delay_off}. The desired voltage V_{delay_off} converted by input pulse width T_{sample_off} can be presented as below:

$$I_{M1} * T_{sample\_off} = V_{delay\_off} * C_2 \quad (1)$$

where I_{M1} is the drain current of transistor M_1.

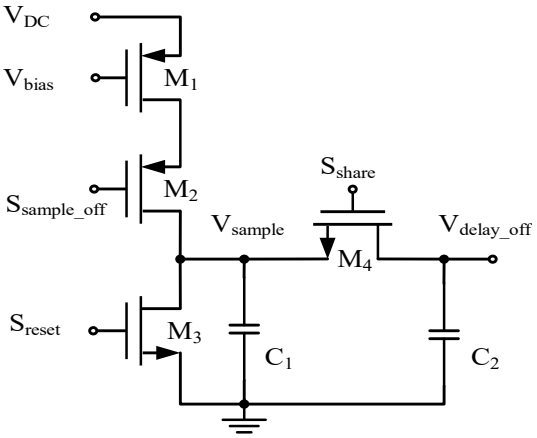


Fig. 5 Time to voltage converter

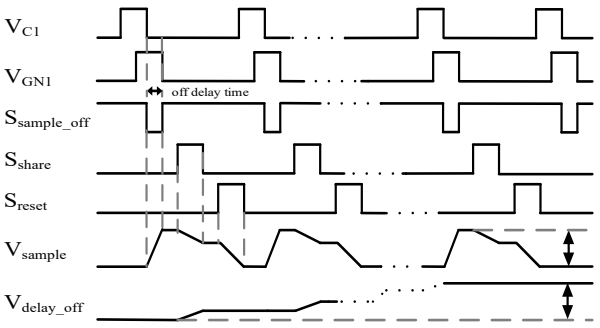


Fig. 6 Timing diagram of time to voltage converter

B. Active Diode Circuit

As shown in Fig. 7, the active diode circuit with comparator, current compensation transistors, buffer and power MOS. The comparator is implemented with transistors, M1~M8. The current compensation circuit is composed of delivery to the output voltage VDC and induce the reverse current. Therefore, to minimize the reverse current, the delay time Td needs to reduce as shown in Fig. 8. Fig. 8 shows the timing diagram of with and without calibration circuit. Delay time Td can be controlled by the current compensation circuit. The delay

calibration circuit generated two voltages and two clock phases to minimum the delay of Td for each comparator. There are two comparators in this active rectifier as shown in Fig. 3. The two clock phases Son_1 and Soff_1 turn on transistor M10 and M12 for injection the current into the comparator. The Son_1 turn on M10 when the Vac1 start to reduce to 0V, until Vac1 lower than 0V. After Son_1 turn off, Soff_1 turn on M12 until Vac1 to Vdc. Son_1 and Soff_1 make the compensation in correct time and reduce the reverse current.

The voltage VAC1 and zero voltage is inputted to the comparator for comparison and generated signal VC1, as shown in Fig. 8. The signal is fed into buffer to turn on the power MOS by signal VGN1. Due to the delay of the buffer, there is a delay time Td between VC1 and VGN1. As a result, the effective conduction time is reduced at the power MOS, which reduces the available time for energy.

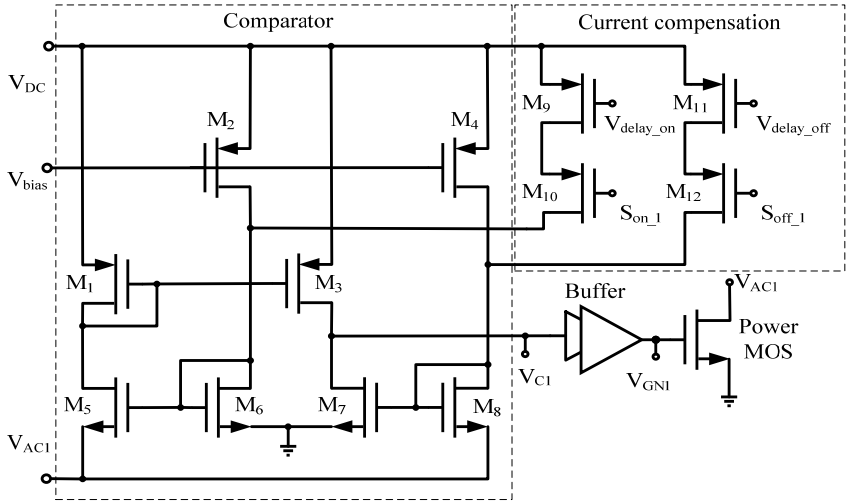


Fig. 7 Active diode circuit

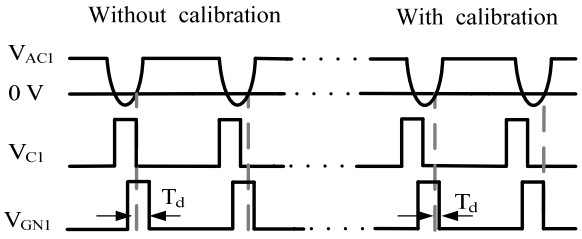


Fig. 8 Timing diagram of with/without delay calibration

III. Simulation Results

The proposed boost converter has been simulated in 0.18 µm CMOS process with standard I/O devices, as shown in Fig. 9. The chip area is 1.09 mm^2 including the pads. If excluding the power MOS and pads, the area is 79 µm×61 µm, as shown in Fig. 10. The output of active rectifiers included in external resister and capacitor are 300 Ω and 2 nF, respectively. Fig. 11 (a) shows the post-simulation waveform of the active rectifier without delay calibration circuit, which makes V_{GN1} turn on lately. The current of M_{N1} (I_{MN1}) induces reverse current. In Fig. 11 (b), V_{GN1} rising and falling edge are in correct point. There are almost no reverse currents in the current of M_{N1} (I_{MN1}). Fig. 12 shows the simulated PCEs with RL that range from 50 Ω to 1500 Ω when input voltage is 3.6 V. Comparison between the enable and disabling delay calibration circuit. With the delay calibration circuit, the PCE are 15%~45% improved at different load. Fig. 13 shows the performance of rectifier in various input voltage. The simulated PCEs with the output voltage that ranges from 2 to 3.6 V are higher than 92.4% when R_L = 300 Ω and 90.5% when R_L = 600 Ω, respectively. The improvement is due to the time to voltage converter can generate accurate compensation for different load.

Comparison with prior work is shown in Table I. Both the PCE and VCE are higher than previous works at different loading conditions thanks to the proposed delay compensation circuit.

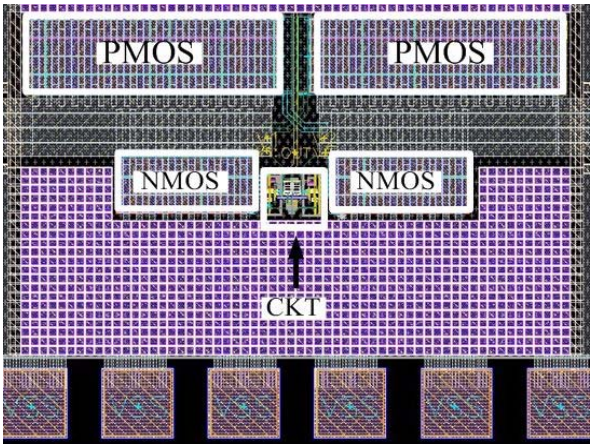


Fig. 9 Layout of proposed circuit

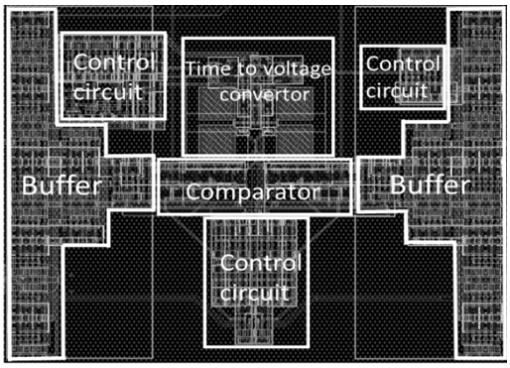
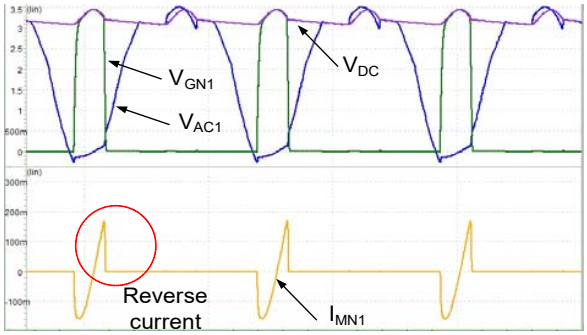
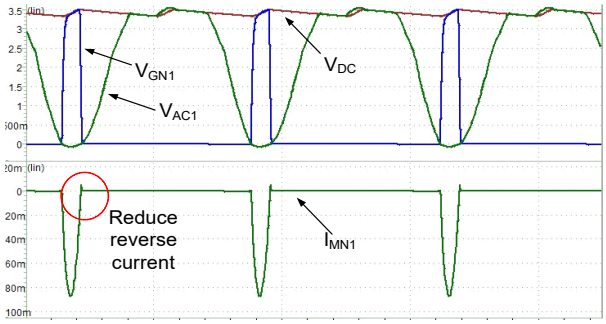


Fig. 10 Layout of core area with power MOS and pad



(a)



(b)

Fig. 11 Simulation waveforms of the proposed rectifier (a) without delay calibration circuit (b) with delay calibration circuit

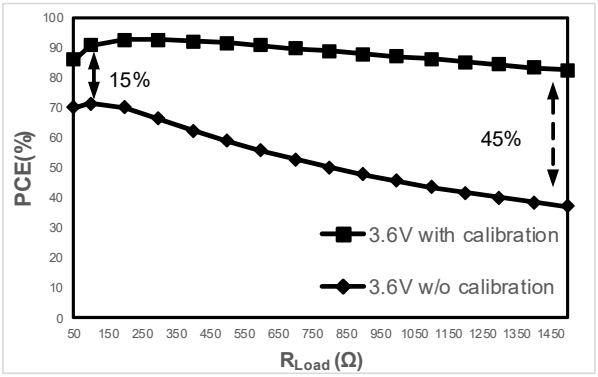


Fig. 12 With and without delay calibration circuit of PCE

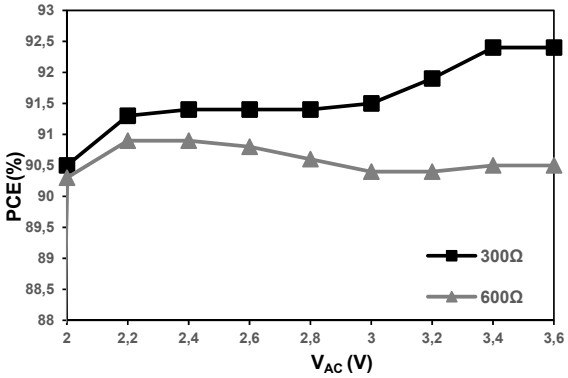


Fig. 13 PCE of different input voltage

TABLE I
COMPARISON WITH PRIOR ART

	[7]	[9]	[11]	This work*
Technology (μm)	0.35	0.18	0.35	0.18
Frequency (MHz)	13.56	13.56	13.56	13.56
Input range (V)	1.5-4	1.5-4.5	1.8-3.6	2-3.6
Output capacitor	1.5nF	0.1μF	2nF	2nF
POUT (Max.)	24.8mW	102mW	64.8mW	38.6mW
PCE	84.2%-90.7%	88.5%-92.2% @RL=500Ω	89.1%-91.4% @RL=500Ω	90.5%-92.4% (RL=300Ω)
VCE	79%-93%	89%-93%	90.4%-94.6%	91.5%-93.5% (RL=300Ω)

*Simulation results

IV. CONCLUSION

In this paper, an active rectifier with delay calibration circuit is presented to compensate the delay to due to the buffer in the active diode. The rectifier has the high power efficiency over a wide input range from 1.6 V to 5.2 V. A peak PCE of 92.4%, a peak VCE of 94.2% and a maximum output power of 38.6 mW are achieved at 3.6V input voltage.

ACKNOWLEDGEMENT

The research was supported by Ministry of Science and Technology, R.O.C. under Grant MOST 107-2221-E-185-061.

REFERENCES

[1] T. Campi, S. Cruciani, F. Palandrani, V. D. Santis, A. Hirata, and M. Feliziani, "Wireless power transfer charging system for AIMDs and pacemakers," IEEE Trans. Microw. Theory Techn., vol. 64, no. 2, pp. 633–642, Feb. 2016.

[2] T. Akin, K. Najafi, and R. M. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," IEEE J. Solid- State Circuits, vol. 33, no. 1, pp. 109–118, Jan. 1998.

[3] P. T. Bhatti and K. D. Wise, "A 32-site 4-channel high density electrode array for a cochlear prosthesis," IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2965–2973, Dec. 2006.

[4] A. Rothermel, L. Liu, N. P. Aryan, M. Fischer, J. Wuenschmann, S. Kibbel, and A. Harscher, "A CMOS chip with active pixel array and specific test features for subretinal implantation," IEEE J. Solid-State Circuits, vol. 44, no. 1, pp.290–300, Jan. 2009.

[5] M. M. Rana, W. Xiang,E. Wang , X. Li, B. J. Choi," Internet of Things Infrastructure for Wireless Power Transfer Systems," IEEE Access, Vol. 6, pp. 19295 – 19303, 2018.

[6] J. Fuh, S. Hsieh, F. Yang, and P. Chen, "A 13.56MHz Power-Efficient Active Rectifier with Digital Offset Compensation for Implantable

Medical Devices" In IEEE WirelessPower Transfer Conference (WPTC), 2016, pg. 1-3.
[7] Y. Lu, and W. H. Ki, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," IEEE Trans. Biomed. Circuits Syst., vol. 7, no. 7, pp. 256–265, June. 2013.
[8] Y. Lu, W. Ki," A 13.56 MHz CMOS Active Rectifier With Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Systems" IEEE Trans. Biomed. Circuits Syst., vol. 8, no. 3, June. 2014.
[9] X. Li, C. Tsui, and W. Ki, "A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices" IEEE J. Solid-State Circuits, vol. 50, no. 40, April 2015.
[10] C. Huang, T. Kawajiri, and H. Ishikuro, "A Near-Optimum 13.56 MHz CMOS Active Rectifier With Circuit-Delay Real-Time Calibrations for High-Current Biomedical Implants" IEEE J. Solid-State Circuits, vol. 51, no. 8, August 2016.
[11] L. Cheng, W. Ki, Y. Lu, and T. Yim," Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems" IEEE J. Solid-State Circuits, vol. 51, no. 3, March 2016.