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An 8-Bit, 100-MSPS Fully Dynamic SAR ADC for Ultra-High Speed Image Sensor

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***Abstract*—**In this paper, a dynamic and power efficient 8-bit and 100-MSPS Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is presented. The circuit uses a non-differential capacitive Digital-to-Analog (DAC) architecture segmented by 2. The prototype is produced in a commercial 65-nm 1P7M CMOS technology with 1.2-V supply voltage. The size of the core ADC is 208.6 x 103.6 μm^2. The post-layout noise simulation results feature a SNR of 46.9 dB at Nyquist frequency, which means an effective number of bit (ENOB) of 7.5-b. The total power consumption of this SAR ADC is only 1.55 mW at 100-MSPS. It achieves then a figure of merit of 85.6 fJ/step.

***Keywords*—**CMOS analog to digital converter, dynamic comparator, image sensor application, successive approximation register.

I. Introduction

ULTRA-HIGH-SPEED image sensors are more and more developed for several applications as motion analysis, explosives, ballistic, biomechanics research, crash test, airbag deployment, deformation, droplet formation or fluid dynamics. The highest frame rate achieved by an image sensor is 16.7-Mfps with a burst capturing speed of 5.2-Tpixel/s [1]. The speed is limited by the sensors input/output interconnections. To overcome this bottleneck, the image is first stored in an on-chip memory and after the end of the event to be recorded, the readout is executed. Previous architectures designed in the BIS principle are based in a full analog approach in which the embedded memory is limited to 100 frames and the acquisition rate is in the order of 10-Mfps for large 2D arrays [2]-[4]. A digital storage allows storing one order of magnitude more frames as the information density per surface unit is higher [5]. The specificity of the digital storage BIS architecture is the in-line analog to digital (AD) conversion at full speed. In order to handle a pixel rate above 1 Tpixel/s, it is mandatory to propose a massively parallelized approach for the AD conversion. A solution is to use a stack of silicon dies that allows to split the analog front end, the AD conversion, and the memory on three different layers and to fit the subparts of the sensor within the pitch of a pixel or a cluster of pixel. Moreover, "Through-Silicon-Via" (TSV) is necessary for power supply or data communication between the dies. The speed, the area, and the power supply of the several parts of the sensor are highly constrained. In this kind of BIS structure, regarding the state-of-the-art, the ADC is still the bottleneck. We present here a fully-dynamic SAR ADC running at 1-GHz for a sampling of 100-MSPS and 8-bit resolution designed for a cluster of 10 pixels working at the sampling rate of 10 Mfps at full resolution up to 100 Mfps with reduced spatial resolution. The proposed AD converter is fully dynamic and can achieve high power efficiency. It does not consume any static power.

The paper is organized as follows. Section II describes the proposed SAR ADC architecture. Section III shows the circuit implementation. Section IV presents the simulation results of the designed ADC. The conclusion is drawn in Section V.

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II. SAR ADC Architecture

The main building blocks of a SAR ADC are the comparator, the sample-and-hold (S/H) circuit, a Digital to Analog Converter (DAC) interfaced with a SAR logic. It works by using a DAC and a comparator to perform a successive binary search to find the best value close to the input voltage. The DAC is based on a switched capacitor array to save the power dissipation. In a charge-redistribution based architecture, the capacitor network is used to integrate both the S/H circuit and DAC function.

A. SAR ADC Implementation

The designed SAR ADC is a single-ended architecture based in a feedforward principle with a binary capacitor array segmented by two to reduce the total value of the capacitors seen by the input nodes during the sampling phase, and also to reduce the total area of the chip. Fig. 1 illustrates the SAR ADC implementation.

During the sampling phase, the top plates of both the MSB and the LSB capacitor arrays sample the analog input signal V_{IN}, while the bottom plates of all capacitors are connected to the common-mode voltage V_{MC}. In the same time, the sampling capacitor C_{SMPL} is connected to V_{MC}. At the end of the sampling phase, the first comparison is performed immediately. Depending on the result at the comparator output, the largest capacitor of the MSB array (8C) is switched to VDD or "0", while the other capacitors remain connected to V_{MC}. This procedure is repeated until the last bit (LSB) is found. One may notice that only one capacitor is switched following each comparison step. This strategy helps to reduce the dynamic power dissipation sunk from the power supply.

III. Implementation of Key Building Blocks

The design considerations of the key elements of the SAR ADC are described in the following subsections.

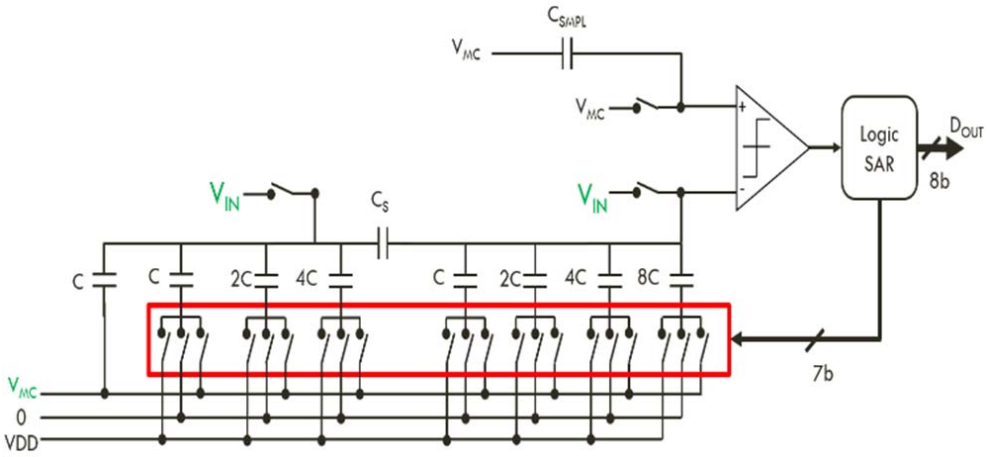

Fig. 1 SAR ADC schematic implementation

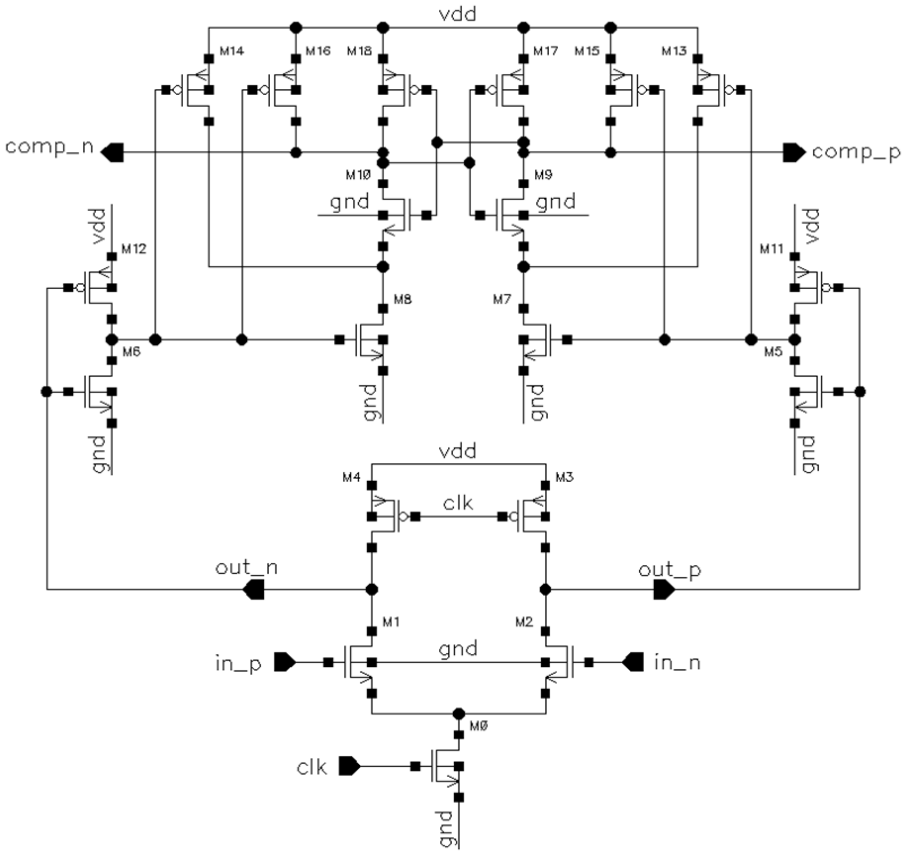

Fig. 2 Schematic of the dynamic comparator

A. Dynamic Comparator

Fig. 2 shows a schematic of the dynamic comparator. It is based in the comparator designed by [6]. Our comparator shows a lower input-referred latch offset voltage but a higher delay time than the one presented in [6]. It does not consume any static current; therefore it is suitable for a very low power design. The proposed comparator is based in two latch stages: the first stage M0 to M4 is the dynamic amplifier with a high gain to ensure a low input offset, while the second stage is the latch comparator.

The main drawbacks of dynamic comparator are the offset and the kick-back noise. But, this designed comparator displays a better input–referred offset features and less kickback noise issue than the conventional one. For our application, 8-bit resolution which is necessary over 1.2-V dynamic range means an LSB of 3.9-mV. The maximum

acceptable offset is about half LSB (1.95-mV). Metastability in latch comparator is a real issue that occurs when both input signals are very close to one another. The probability of metastability error can be defined by (1) [7]:

$$P_{error} = \frac{2 \cdot V_L}{A_{UL} \cdot LSB} \cdot e^{\frac{-T}{t_2 - t_1}} \quad (1)$$

where LSB is the quantum size, V_L is the minimum valid logic level comparator must generate, A_{UL} is the comparator unlatched gain, T is the maximum time period allowed for the comparator to make a correct decision, and t_2-t_1 is defined as the time regeneration. Fig. 3 shows the plot of (1) for several clock frequency form 800-MHz up to 2-GHz. One can see for 1-GHz clock frequency, the probability of metastability error is about 10^{-8} errors per second.

The Monte Carlo simulation results with 1,000 samples are shown in Fig. 4. We measure an offset of only 1.75-mV without any calibration. It is about 10 times less than in [6] where 16.3-mV was published. In a SAR architecture, this offset could reduce the full dynamic range of the converter.

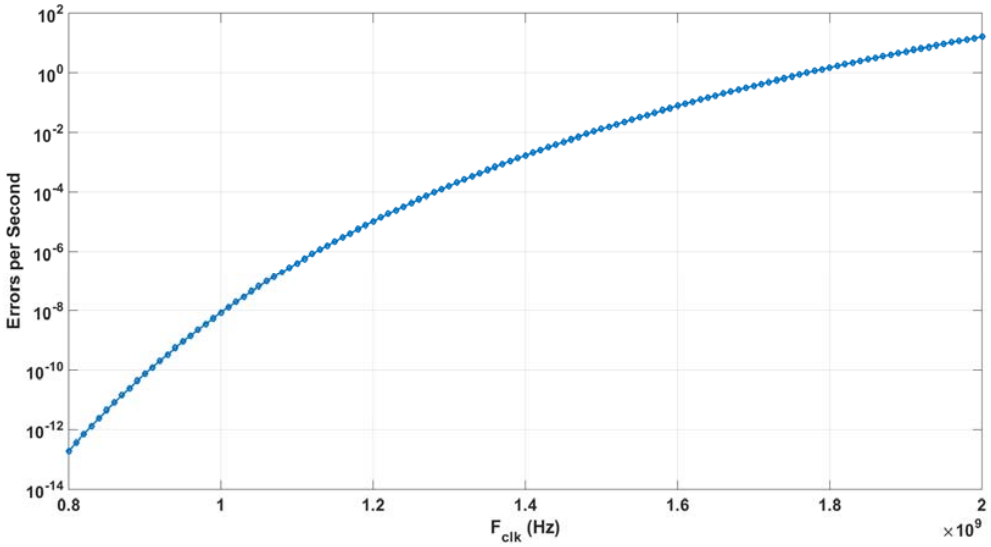

Fig. 3 Probability of metastability error according to clock frequency

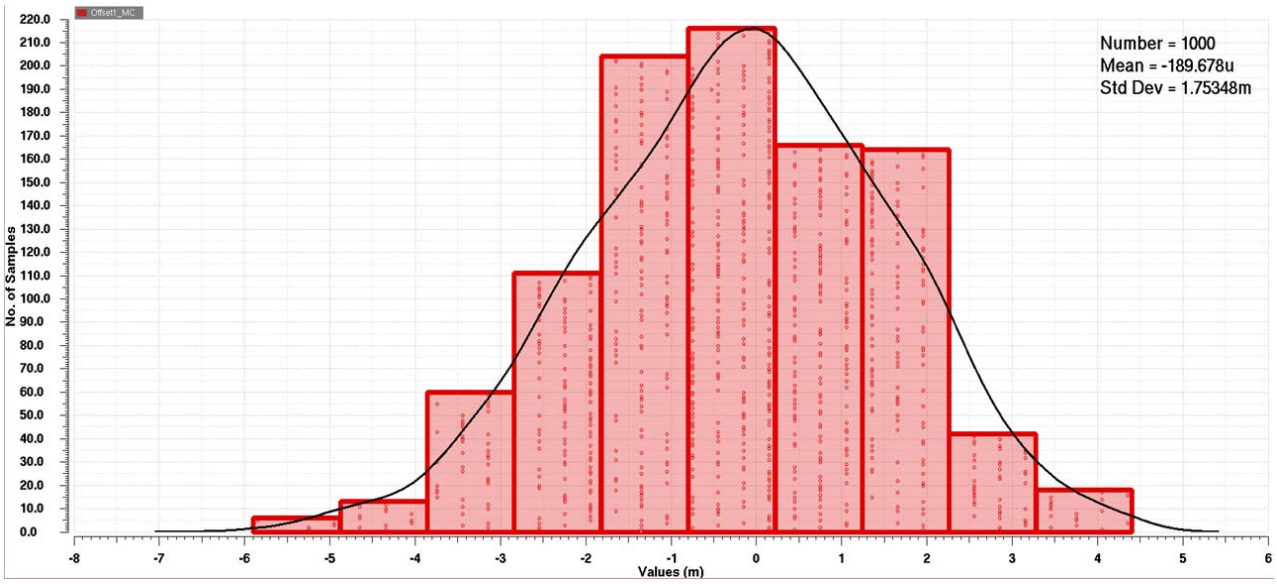

Fig. 4 1,000 samples Comparator offset Monte Carlo Simulation results

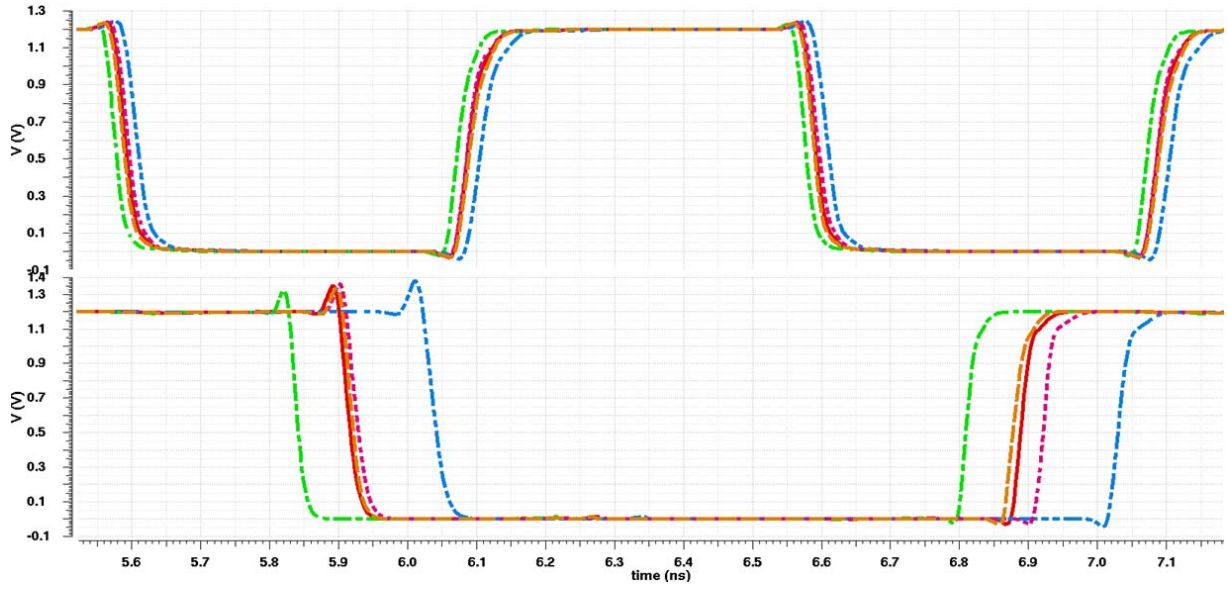

Fig. 5 Corner simulation results of the comparator (dashed-dot: FF, dashed: FS, continued: TT, dot: SF, dashed-dot-dot: SS)

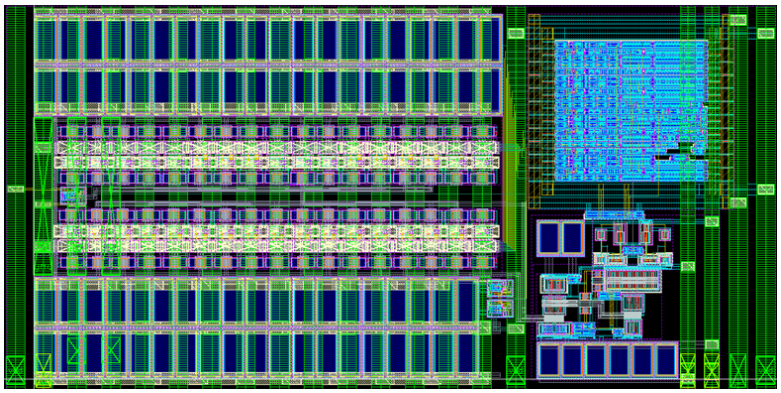

Fig. 6 Layout picture of the radix-2 SAR ADC

The delay time of the comparator following a typical model simulation is about 300 ps with an input signal of 500 µV. The delay time over $\log(\Delta V_{IN})$ is equal to -48 ps/decade. This time is defined as the delay between the 50% clock edge and the instant when the comparator output crosses 50% of V_{DD}. Fig. 5 illustrates the corner (TT, SS, FF, SF and FS model) simulations results of the comparator output. The clock frequency is 1 GHz. We notice that the comparator output changes before the rising edge of the clock whatever the corner model or the output edge. In Table I, the delay times corner simulation results of our comparator are summarised.

TABLE I
DELAY TIME SIMULATION RESULTS

Model	TT	SS	FF	FS	SF
Falling edge (ps)	324.2	430.8	263.8	331.1	331.5
Rising edge (ps)	301.3	421	235.4	292.1	328.1

The simulated power consumption of the proposed comparator is 650-µW at a clock frequency of 1-GHz with a supply-voltage of 1.2-V.

B. DAC Implementation

As indicated before (see Fig. 1), the DAC is implemented by a radix-2 capacitor array segmented in two parts: 4 bits MSB and 3 bits LSB linked through a segmentation capacitor C_s. The limitations of the capacitive DAC are the mismatch in the capacitors array, and also the sensitivity to parasitic capacitors. Moreover, the segmented configuration can increase the non-linearity and distortions, but it helps to reduce the total equivalent capacitor and so for the area consumed and finally it helps to save the dynamic power taken from the power supply. The unit capacitor is a custom MOM capacitance of 6-fF. The MOM capacitor is shielded to reduce the parasitic capacitors effects.

IV. SIMULATION RESULTS

The proposed radix-2 SAR ADC was designed using a 1P7M 65-nm CMOS process. The layout picture is shown in Fig. 6. The total power consumption of the ADC is about 1.55-mW at 100 MSPS. The size of the core ADC is only 208.6 x 103.6 μm^2.

This prototype used custom MOM capacitors with 3-metal layers. The radix-2 capacitor array uses 24-unit capacitors of 2.4-µm x 2.4-µm: 16 unit capacitors for the MSB side and 8 for the LSB one. Therefore, the total sampling capacitance of the capacitor network is 144-fF. The capacitor network occupies a total active area of 157-µm x 55-µm, about 40% of the whole ADC. The comparator fills about 8.3% of the total area, whereas the digital part is about 13.5%. The remaining surface is used for the decoupling capacitors for the reference voltage of the DAC part: VDD and "0" in Fig. 1. The use of decoupling capacitors overcomes the need of a wideband reference voltage buffer which should increase the total power consumption budget of the converter.

The designed SAR ADC is a fully dynamic converter. As illustrated in the plot of Fig. 7, for sampling frequency of 10-MSPS, 50-MSPS and 100-MSPS, the total power consumption increases linearly when sampling frequency is increased. The power consumption is proportional to sampling frequency: at 100-MSPS, we have 1.55-mW, whereas it is about 160-µW at 10-MSPS.

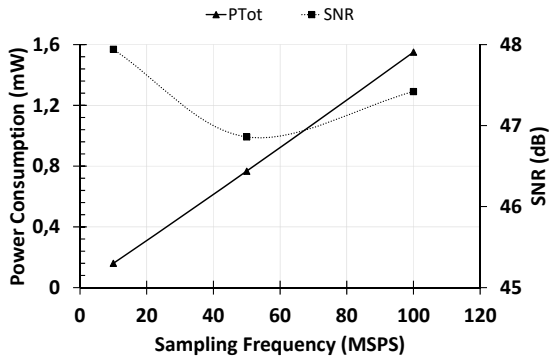

Fig. 7 Total power consumption (continuous line+triangle) and SNR (dot line + square) for several sampling frequency

As indicated in Fig. 7, the simulated SNR results are obtained with 256-samples and a sinusoidal-input signal of 1-MHz with coherent sampling. We can notice that the ENOB estimated by (2) is about 7.55-b for those three sampling clocks (10-MSPS, 50-MSPS, and 100-MSPS).

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (2)$$

At 100-MSPS, for several sinusoidal-input signal frequencies from 1-MHz up to Nyquist frequency (1-MHz, 5-MHz, 10-MHz, and 50-MHz), we obtained a SNR above 46.8-dB as illustrated in Fig. 8.

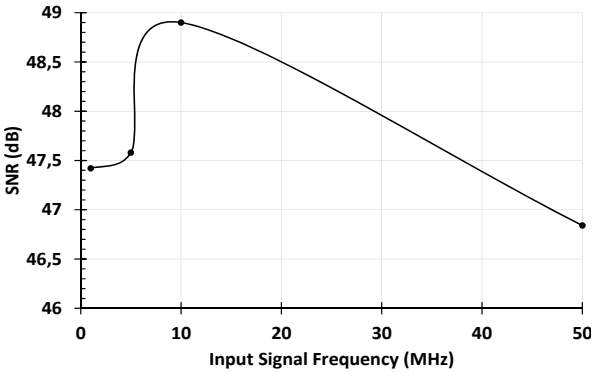

Fig. 8 SNR for different input signal frequency at 100-MSPS

Fig. 9 shows FFT spectrum of the ADC output sampling a 1-V sinusoidal-input signal of 10-MHz with coherent sampling at 100-MSPS. All those results were obtained through post-layout, transient noise simulations and 256 samples data.

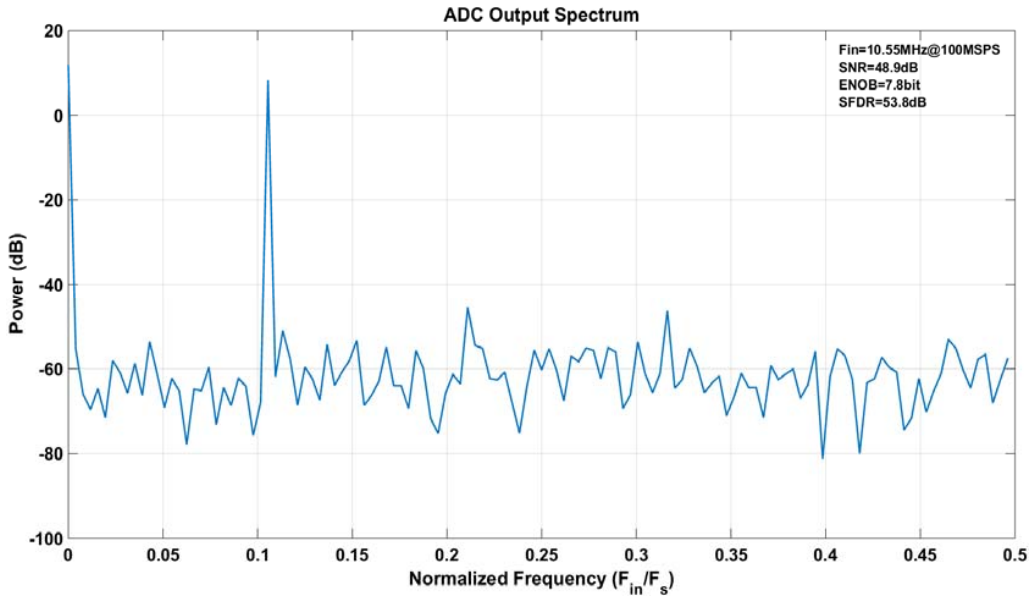

Fig. 9 Post-Layout simulation with noise FFT spectrum at 100-MSPS

Fig. 10 illustrates the power consumption breakdown of each part of the SAR ADC with a sampling frequency of 100-MSPS. We can notice that the digital part dissipates more than the half of the total power consumption with a power supply of 1.2-V.

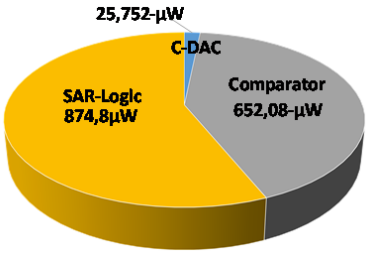

Fig. 10 Power consumption breakdown of the designed SAR ADC with 1.2-V power supply

By using the Walden Factor of Merit (FoM) expression defined in (3), our designed SAR ADC FoM is about 85.6-fJ/conversion step.

$$FOM = \frac{P_{Tot.}}{f_s \cdot 2^{ENOB}} \ [J/conv.] \quad (3)$$

Table II shows the performance summary of the designed 8-bit SAR ADC and a comparison with state-of-the-art ADCs.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	This Work	[8]	[9]	[10]
Technology	65-nm CMOS	65-nm CMOS	90-nm CMOS	65-nm CMOS
Architecture	SAR	SAR	SAR	SAR
Supply [V]	1.2	1.0	1.0	1.2
Fs [MSPS]	100	250	4	450
Resolution [bit]	8	8	9	8
Area [mm^2]	0.0216	0.028	0.01	0.035
Power [mW]	1.55	1.8	0.381	5.4*
SNR [dB]	46.84	46.7	45.6	47.3
FOM [fJ/conversion step]	85.6	60	612.9	76

*Reference voltage buffer and clock generator included.

V. CONCLUSION

A fully dynamic and power efficient 8-bit and 100-MSPS SAR ADC has been presented. The circuit is suitable for very high speed image sensor with a 100 million frames per seconds. The size of the core ADC is only 208.6 x 103.6 µm^2. The post-layout noise simulations show a SNR of 46.9dB at Nyquist frequency, which means an ENOB of 7.5-b. The total power consumption of this SAR ADC is 1.55-mW at 100-MSPS. It achieves then a figure of merit of 85.6-fJ/step.

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