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Dynamic Modelling and Virtual Simulation of Digital Duty-Cycle Modulation Control Drivers

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***Abstract*—**This paper presents a dynamic architecture of digital duty-cycle modulation control drivers. Compared to most oversampling digital modulation schemes encountered in industrial electronics, its novelty is founded on a number of relevant merits including; embedded positive and negative feedback loops, internal modulation clock, structural simplicity, elementary building operators, no explicit need of samples of the nonlinear duty-cycle function when computing the switching modulated signal, and minimum number of design parameters. A prototyping digital control driver is synthesized and well tested within MATLAB/Simulink workspace. Then, the virtual simulation results and performance obtained under a sample of relevant instrumentation and control systems are presented, in order to show the feasibility, the reliability, and the versatility of target applications, of the proposed class of low cost and high quality digital control drivers in industrial electronics.

***Keywords*—**Dynamic architecture, virtual simulation, duty-cycle modulation, digital control drivers, industrial electronics.

I. Introduction

THE DDCM (digital duty-cycle modulation), is a subclass of oversampling discrete modulation policies resulting from discrete time implementation of switching modulation techniques as illustrated in Fig. 1, where the resulting duty-cycle modulated wave $x_m(x, t)$ is defined as:

$$D_m(x_m(x, t) = T_{on}(x, t) / T_m(x, t), \quad (1)$$

In (1), $T_{on}(x, t)$ is the pulse width of output wave $x_m(x, t)$ over a time period: $T_m(x, t) = T_{on}(x, t) + T_{off}(x, t)$.

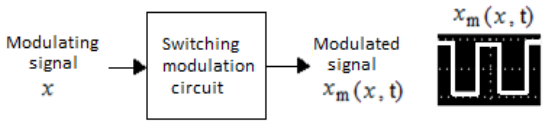

Fig. 1 Switching modulation technique

The basic switching modulation architectures used in industrial electronics since 1962 are presented in Fig. 2. They consist of: a) SDM (sigma-delta modulation) invented by Mammano in 1962 [1], [2] as a new principle of pulse coding modulation technique; b) PWM (pulse width modulation) initiated by Pressman in 1977 [3], as a modern control driver for power converters; c) DCM (duty-cycle modulation), e.g., a relevant class of modulation techniques published in 2005 [4] for industrial electronic systems. The top level analog circuits of SDM, PWM and DCM are summarized in Fig. 2, where a common building technology based on integrated operational amplifiers, is adopted for the sake of better comparison.

The basic SDM topology shown in Fig. 2 (a) behaves as a closed loop digital processing system. However, it consists of a great number of analog sub-circuits and requires an external modulation clock source. As a result, the implementation of most realistic DSDM (digital sigma-delta modulation) architectures [5]-[7], relies on multistage digital signal processing chains. On the other hand, the basic PWM architecture presented in Fig. 2 (b) is widely used as a core of most control drivers in power electronics [8], [9]. In addition, DPWM outputs are widely implemented today in FPGA and CPLD chips [10], [11]. However, the open loop architecture and the lack of embedded modulation clock, appear to be main weaknesses of PWM topology. As a result, most realistic DPWM topologies also consist of complex DSP chains [12], [13]. Fortunately, the basic DCM architecture observed in Fig. 2 (c) offers a number of composite merits including: a) structural simplicity; b) simple set of building operators; c) embedded negative and positive feedback loops; d) embedded clock); e) exact knowledge of analytical characteristics; and f) versatile use in industrial electronics, e.g. DCM-Based ADC [14], [15], DCM-based DC-DC Buck converters [16], and DCM-Based signal transmission [17], [18]. However, an intrinsic and intricate problem arising from the use of DCM policy is the nonlinear analytical structure of (1) given by (2),

$$D_m(x) = \frac{\ln\left(\frac{\alpha_2 x - (1+\alpha_1)E}{\alpha_2 x + (\alpha_1 - 1)E}\right)}{\ln\left(\frac{(\alpha_2 x)^2 - ((1+\alpha_1)E)^2}{(\alpha_2 x)^2 - ((\alpha_1 - 1)E)^2}\right)} \quad (2)$$

where,

$$\alpha_1 = R_1 / (R_1 + R_2), \ \alpha_2 = 1 - \alpha_1, \quad (3)$$

and the ±E notation stands for the voltage power supply of the operational amplifier power supply as seen in Fig. 2 (c).

Since 2005, a number of pioneering solutions have been investigated to overcome the computing constraints due to the drastic nonlinear nature of (3). For example in [4] and [14]-[19], it has been shown that around the point (x= 0, $D_m(0)$ =1/2), there exists a suitable choice of α1 = 1-α2 and a corresponding wide modulating range in which a linear approximation of (3) is almost exact. In [20], an optimal quadratic approximation of (3) has been used for the sake of better modulation quality.

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Recently, it has been proven that a lookup table, pre-computed offline from (3) and stored into an embedded memory for real time use is an excellent solution for maintaining the exact sample of (3) in a DSP policy. However, the use of a lookup table is restricted to DSP problems. In addition, in a multichannel context requiring a data base of look-up tables, the available memory capacity of a DSP chip might significantly affected.

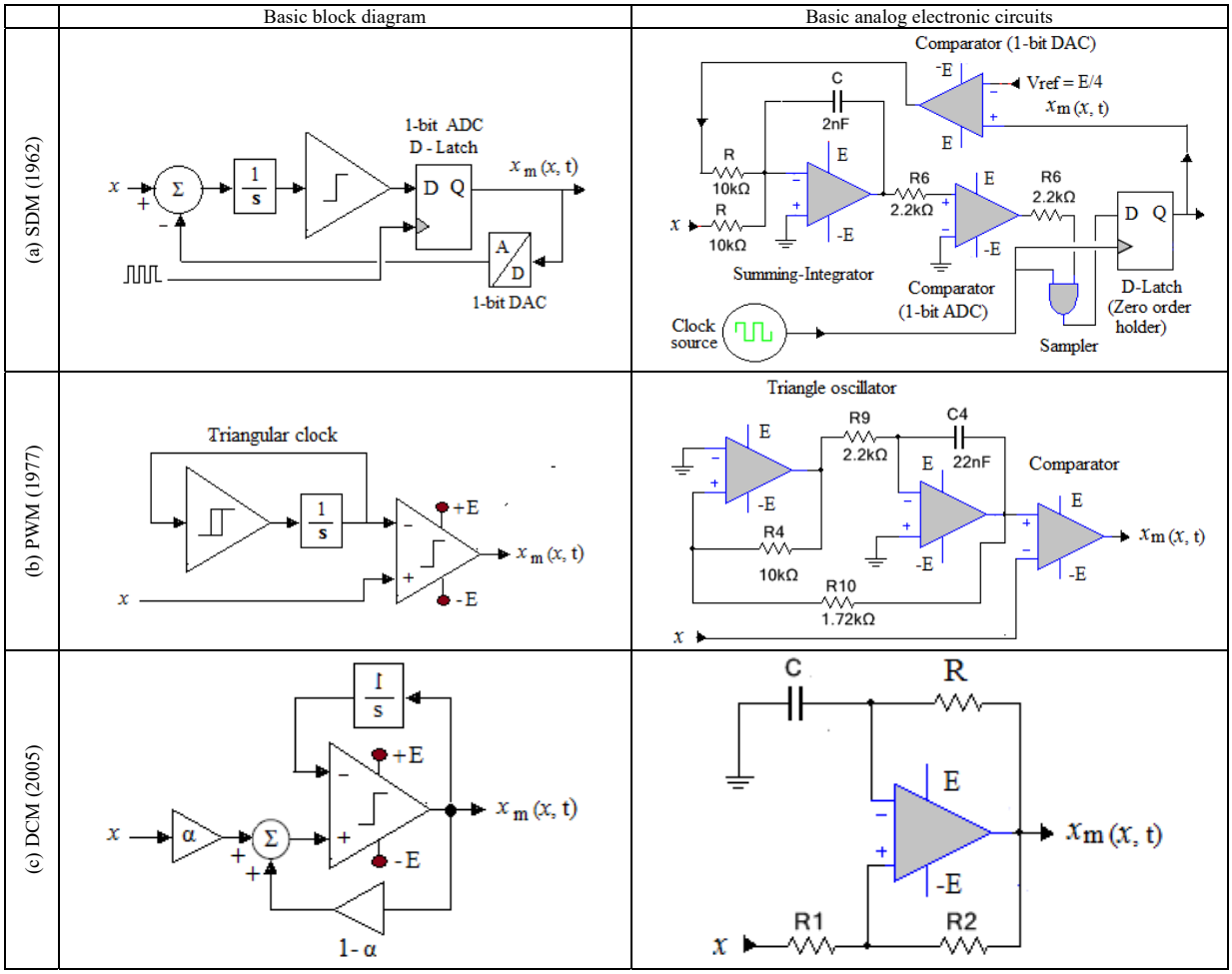

Fig. 2 Sample of basic switching modulation architectures

Unlike most DDCM schemes, which are usually built from either approximations or pre-computed lookup table as in [21], the new topology of DDCM control drivers presented in this paper is synthesized from a discrete dynamic model of an elementary DCM circuit presented in Fig. 2 (c). Compared to most basic oversampling digital modulation schemes, the novelty of the proposed dynamic DDCM topology is founded on a number of composite merits, including; a) Positive and negative feedback loops; b) Embedded clock source; c) Reduced set of design operators and parameters; d) Analytical knowledge of modulation characteristics; d) Neither real time computation of the sample of (3) nor real time use of lookup table is required when processing the modulating input *x*. In addition, as it will be shown later, the scientific relevance arising from these composite virtues is the versatile use of the resulting class of DDCM control drivers in industrial electronics.

The remaining sections of the paper are organized as follows. In Section II, a discrete model of the Dynamic DDCM topology is developed and well tested within Simulink workspace. In Section III, many DDCM-based control systems are outlined in order to show the great relevance of the proposed class of DDCM control drivers in industrial electronics, and the paper is concluded in Section IV.

II. Discrete Model of the Dynamic DDCM Architecture

The behavior of the DCM circuit presented in Fig. 3 (c) is governed under ideal operating conditions of the integrated operational amplifier, by the following set of dynamic equations:

$$\begin{cases} u^+(t) = a_1 x_m(t) + (1-a_1)x(t) & \text{(a)} \\ \varepsilon(t) = u^+(t) - u_C(t) & \text{(b)} \\ x_m(t) = \begin{cases} E, & \text{if } \varepsilon(t) \geq 0 \\ -E, & \text{otherwise} \end{cases} & \text{(c)} \\ \dfrac{duc(t)}{dt} = -\dfrac{1}{\tau} uc(t) + \dfrac{1}{\tau} x_m(t) & \text{(d)} \end{cases} \quad (4)$$

where $a_1 = R_1/(R_1+R_2)$, $R_2 = 1- a_1$, and $\tau = R\ C$. Then, the projection of the dynamic behavior given by (4) into the frequency domain leads to transfer function (5).

$$\frac{Uc(s)}{Xm(s)} = \frac{1}{1+RC\ s} \quad (5)$$

Then, the discretization of (5) using the pole-zero matching transform technique leads to the discrete transfer function (6):

$$\begin{cases} \dfrac{Uc(z)}{Xm(z)} = \dfrac{1-a}{z-a} \\ \text{with } a = e^{-\frac{1}{R\ C}T} \end{cases} \quad (6)$$

After discretization of (5), it is clear that neither (5) nor (6) has a zero, whereas the single pole *a* of (6) results from the z transform of the single pole -1/RC of (5). Furthermore, the discrete time form of (4) or (6) equivalently leads to (7).

$$\begin{cases} u^+(kT) = a_1 x_m(kT) + (1-a_1)x(kT) & \text{(a)} \\ \varepsilon(kT) = u^+(kT) - u_C(kT) & \text{(b)} \\ x_m(t) = \begin{cases} E, & \text{if } \varepsilon(t) \geq 0 \\ -E, & \text{otherwise} \end{cases} & \text{(c)} \\ u_c((k+1)T) = a\ \ u_c(kT) + (1\text{-}a)\ x_m(kT) & \text{(d)} \end{cases} \quad (7)$$

where k = 0, 1, 2, …, whereas T stands for the sampling period.

Fig. 3 presents Simulink virtual model of the proposed Dynamic DDCM topology, associated with the nonlinear discrete algebraic equations (8), and the related unified form is provided in Fig. 3 (b).

It is important to see in Fig. 3 (a) that the unified dynamic core outlined in Fig. 3 (b) only consists of a few linear operators (addition, a time delay, two different gain values *a* and *a1*), a single nonlinear switching comparator, a Zoh (zero order holder) output, and the implicit digital power supply value ±E volts.

As a case study, a prototyping dynamic DDCM core has been simulated in order to test the quality of its dynamic behavior. The set of data used for conducting simulation are given as: a1 = 0.0124, a= 0.99966 and E = 9 V. Then the basic modulation frequency is $f_m(0)$ = 172 KHz, and the sampling frequency retained is 1/T = 25 MHz. As a result, the modulating sine wave *x* with amplitude 2 volts and frequency 5 KHz, and the related modulated output x_m obtained under virtual simulation are presented in Fig. 4. In addition, the frequency spectrum of x_m, computed within MATLAB workspace, shows that the modulating input *x* is adequately encapsulated as a single tone wave with frequency 5 KHz, which is located sufficiently far from the basic modulation frequency located $f_m(0)$ = 172 KHz.

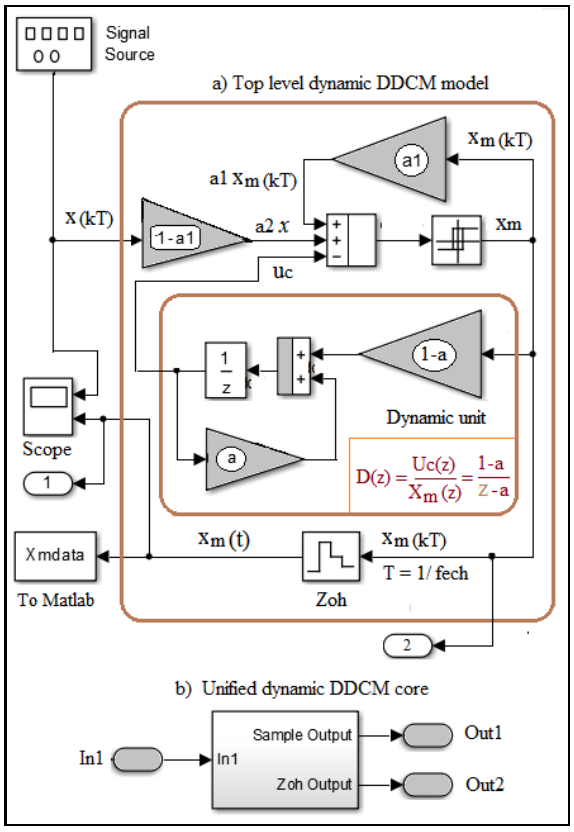

Fig. 3 Simulink model of the proposed dynamic DDCM topology

As expected, many findings with great relevance arise from preliminary results observed in Fig. 4, e.g.: a) Unnecessary explicit knowledge of (3) in the dynamic DDCM policy; b) Following the frequency spectrum of x_m presented in Fig. 4 (b), the modulating control signal *x* can be rigorously extracted from x_m using an appropriate low pass filter; c) As it will be shown in the next section, the proposed dynamic DDCM architecture might be used as a simple digital control driver for a variety of application areas, including digital-to-analog conversion and digital-based control of dynamic systems, which are supplied by power electronic converters.

III. Application of the DDCM Architecture

A. Application I: Digital-to-Analog Conversion (DAC)

For a known modulating band-pass frequency, and a given performance criterion, a complete DAC architecture built from the proposed dynamic DDCM policy, as shown in Fig. 5, consists of an upstream dynamic DDCM core with appropriate

design parameters set {a, a_1, E}, and a downstream analog filter with suitable transfer function F(s). Fig. 5 (a) shows how a prototyping DDCM-Based DAC has been virtually implemented and well tested in Simulink workspace.

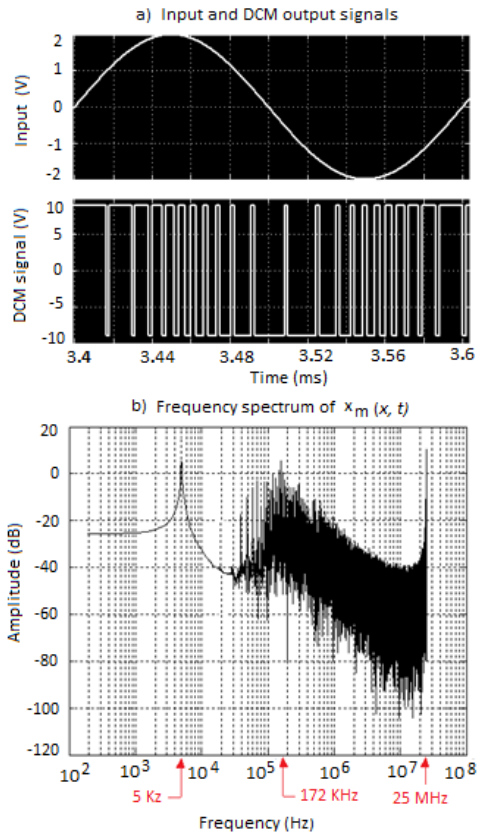

Fig. 4 Simulation results for the prototyping dynamic DDCM core

The set of simulation data used are given as: a) Modulating signal (sine wave with 2 Vpp and fs = 5 KHz); b) Modulation parameters (a1 = 0.0124, a= 0.99966, E = 9); c) Basic modulation frequency (f_m (0) = 172 HKz when x = 0 V); d) A second order active filter with transfer function provided in Fig. 5 (a). Then, the simulation results presented in Fig. 5 (b), show that the digital control input x is rigorously converted into equivalent analog waveform. In addition, the single output tone observed in Fig. 5 (c) exactly occurs at 5 KHz within the frequency spectrum of the analog output signal. Therefore, the overall dynamic DDCM system is a high quality DAC converter, with Spurious Free Dynamic Range (SFDR) value equal to 67 dB. Such a performance level is better than that presented in [21]. In addition, unlike in [21], neither a complex digital processing logic, nor a lookup table saved in the processor memory for real time use are required in the proposed dynamic DDCM algorithm for DAC.

It is important to discover how intrinsic harmonics of the DDCM wave lay within a narrow neighborhood of the basic modulation frequency, $f_m(0)$ = 172 KHz. This expected discovery is a relevant property of DCM policy due to its *feedback loop topology*.

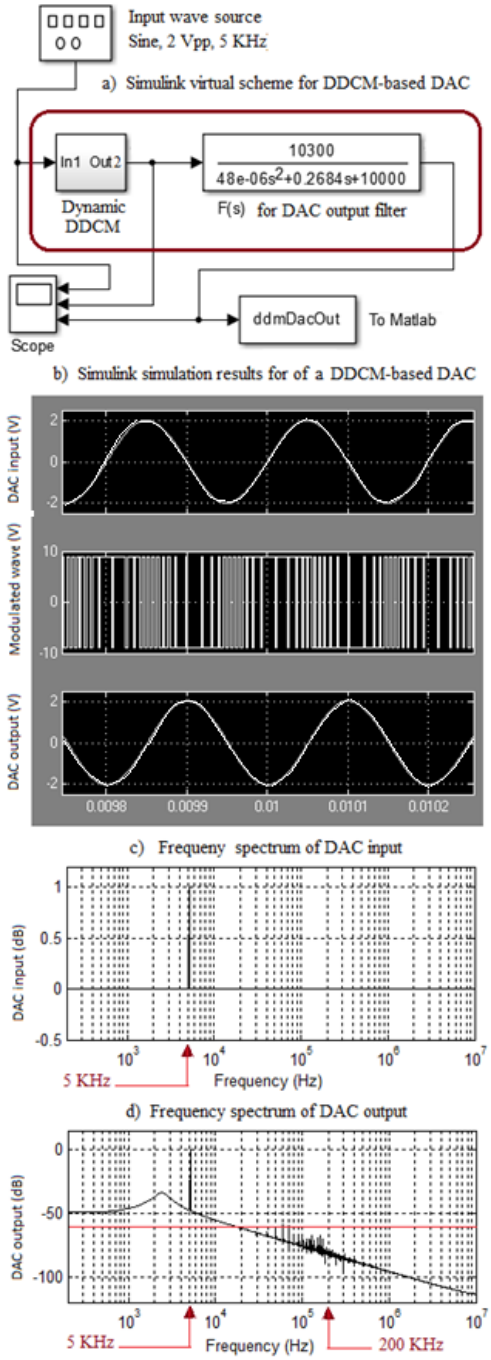

Fig. 5 Characteristics of a prototyping dynamic DDCM-based DAC

B. Application I: Digital-to-Analog Conversion (DAC)

Without loss of generality, let us consider an open loop dynamic system, with input and output $E_m(t)$ and y(t) respectively, and transfer function F(s) = Y(s)/E_m(s), i.e.,

$$F(s) = \frac{Y(p)}{E_m(p)} = \frac{74.4\ s + 21000000}{3.9\ s^2 + 7066\ s + 12000000} \quad (8)$$

where (8) stands for the dynamic model of a prototyping open loop power buck converter, with switching power supply E(t) = ± *9 Volts* under dynamic DDCM control, with parameters T = 0.0005 s, a1 = 0.1071, and a = exp(-T/RC) = 0.27.

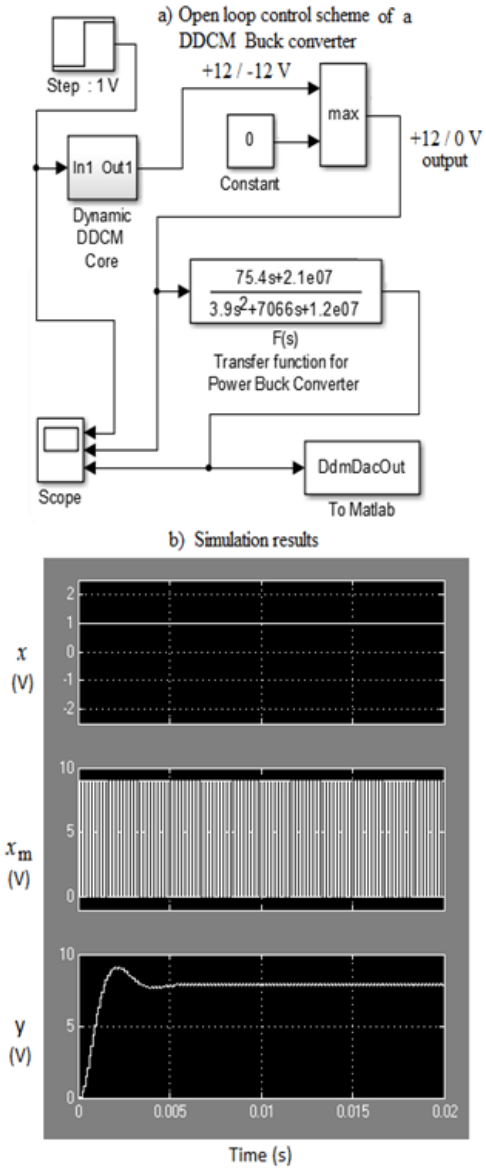

Fig. 6 Simulink design scheme for DDCM-based control of the open loop power Buck converter (8)

Fig. 6 shows the Simulink design scheme for the dynamic DDCM-based control of (6), under a digital step input $x = 1$ volt. From this step, any suitable feedback compensation policy could be designed and implemented, for digital control of the power Buck converter, via the proposed low cost and high quality dynamic DDCM drive.

IV. Conclusions and Perspectives

The dynamic DDCM topology presented in this paper, has been modelled and simulated virtually in MATLAB/Simulink workspace. A few well tested applications investigated and presented have shown that the proposed class of DDCM control drivers, might offer high quality and versatility for a variety of digital instrumentation contexts. However, since the work presented in this paper is limited to virtual design and simulation, it would be very relevant in future research works to implement a prototyping FPGA-based DDCM driver, for digital instrumentation and control systems in industrial electronics.

References

[1] B. Mammano, "Resonnant mode converter topologies, TOP IC1, pp. 1-1/1-11, © Unitode Corporation.
[2] H. Inose, Y. Yasuda and J. Marakami, "A telemetering system by code modulation, delta-sigma modulation," IRE Trans. on Space, Electronics and Telemetry, SET-8, pp. 204-209, Sept 1962.
[3] Abraham Pressman, "Switching and linear power converter design, Volume 2", 372 pages, Hayden Book Co., 1977.
[4] J. Mbihi, B. Ndjali, and M. Mbouenda, "Modelling and simulations of a class of duty cycle modulators for industrial instrumentation," *Iranian J. Electr. Comput. Eng.*, vol. 4, no. 2, pp. 121–128, 2005.
[5] N. Doley and A. Kornfeld, "Comparison of Sigma-Delta converter circuit architectures in digital CMOS technology", Journal of circuits, systems ans computers", vol. 14, No 3, pp. 515-532, © World scientific publishing company, 2005.
[6] Y. Matsuya, et al, "A 16 bit oversampling A-to-D conversion technology using triple-integration noise shaping," IEEE J. of Solid-State Circuits, Vol. SC-22, No. 6, pp. 921-929, Dec. 1987.
[7] K. R. Rekha, S. Vashishtha, "A survey on FPGA based spaced vector PWM motion control, International Journal of Advanced Research in Electrical, Electronics and instrumentation engineering", vol. 4, January pp. 282-288, 2015.
[8] B. J. Patella, A. Prodic, "High frequency digital PWM controller IC for DC-DC converters", IEEE transactions on power electronics, vol. 18, N° 1, pp. 438-446, 2003.
[9] S. K. Mazunder, M. Tahir, S. L. Kamizetty, "Wireless PWM control of a DC-DC buck converter", IEEE transactions on power electronics, Vol. 20, N°6, pp. 1280-1286, 2005.
[10] V. Sabarinath and K. Sivanandam, "Design and implementation of FPGA-based high resolution digital pulse width modulation", International Journal of Advanced Research in Electronics and Communications engineering, Vol. 2, Issue 5, 563-567, 2013.
[11] A. Tashakori, M. Hassanudeen and M. Ektesabi, "FPGA-based controller drive of BLCD motor using digital PDM technique", IEEE PEDS, 9-12 June 2015, Sydney.
[12] S. Chander, P. Agarwal and I. Gupta, "ASIC and FPGA based DPWM architectures for single phase and single output DC-DC converter: a review", Central European Journal of Engineering, Vol 3, Issue 4, pp. 620-643, 2013.
[13] E. Koutroulis, A. Dollas and K. Kalaitzakis, "High frequency pulse width modulation implementation using FPGA and CPLD ICs", Journal of systems architecture, © Elsevier, Vol 52, pp. 332-344, 2006.
[14] Mbihi, J., Ndjali Beng, F., Kom, M., and Nneme Nneme, L. *A novel analog-to-digital conversion technique using nonlinear duty-cycle modulation*", International Journal of electronics and computer science engineering, 1(3), 2012, pp. 818-825.
[15] I. Mbihi, L. Nneme Nneme, "A Multi-Channel Analog-To-Digital Conversion Technique Using Parallel Duty-Cycle Modulation". *International Journal of Electronics and Computer Science Engineering.* 2012; 1(3):826–833p.
[16] J. Mbihi, L. Nneme Nneme, "A Novel Control Scheme for Buck Power Converters using Duty–Cycle Modulation". *International Journal of Power Electronics*, 2013;5(3/4):185–199p.
[17] Nneme Nneme L., Mbihi J., Modeling and Simulation of a New Duty–Cycle Modulation Scheme for Signal Transmission System, *American Journal of Electrical and Electronic Engineering (AJEEE)*. 2014; 2(3): 82–87p.

[18] Moffo Lonla B., Jean Mbihi, Leandre Nneme Nneme. A Low Cost and High Quality Duty–Cycle Modulation Scheme and Applications. *International Journal of Electrical, Electronic Science and Engineering*. 2014; 8(3):82–88p.
[19] Moffo Lonla B., Mbihi J., Nneme Nneme L., Kom M., A Novel Digital–to–Analog Conversion Technique using Duty-Cycle Modulation. *International Journal of Circuits, Systems and Signal processing*. 2013; 7(1):42–49p
[20] Mbihi, Nneme, Kom, A Suboptimal Nonlinear Duty-cycle Modulation Scheme, , Journal of electronic design technology, Vol. 7, Issue 1, pp. 22-31, 2016.
[21] Moffo Lonla B., Mbihi J. A Novel Digital Duty–Cycle Modulation Scheme for FPGA-Based Digital-to-Analog Conversion. *IEEE Transaction on circuits and system II*. 2015; 62(6):543–547p.

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