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Compensated CIC-Hybrid Signed Digit Decimation Filter

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***Abstract*—**In this paper, firstly, we present the mathematical modeling of finite impulse response (FIR) filter and Cascaded Integrator Comb (CIC) filter for sampling rate reduction and then an extension of Canonical signed digit (CSD) based efficient structure is presented in framework using hybrid signed digit (HSD) arithmetic. CSD representation imposed a restriction that two non-zero CSD coefficient bits cannot acquire adjacent bit positions and therefore, represented structure is not economical in terms of speed, area and power consumption. The HSD based structure gives optimum performance in terms of area and speed with 37.02% passband droop compensation.

***Keywords*—**Multirate filtering, compensation theory, CIC filter, compensation filter, signed digit arithmetic, canonical signed digit.

I. Introduction

WITH the increasing applications of digital techniques in signal processing, the requirement for efficient conversion between various sampling frequencies has become apparent such as in narrow-band filtering where an efficient implementation of a digital filter can be realized by using a sampling rate reduction followed by a sampling rate increase [1], [2]. Multirate digital signal processing deals with the sampling rate conversion of a digital signal, including decimation and interpolation.

Crochiere and Rabiner [1] have shown that sampling rate increase and decrease are basically an interpolation process that can be efficiently implemented using FIR digital filters. Bellanger et al. [2] found that efficient implementation of low-pass FIR filters could be obtained by the process of first reducing the sampling rate, filtering, and then increasing the sampling rate back to the original frequency. They proposed a multistage technique of sampling rate reduction by alternately filtering with half-band filters and reducing the sampling rate by factors of two until a desired power of two sampling rate reduction was achieved.

In 1981, Hogenauer developed a coefficient less, hardware efficient filter which is referred as CIC filters [3] that are an economical alternative to conventional decimation and interpolation filters. CIC filters are implemented employing a cascade of ideal integrator stages operating at a high sampling rate and an equal number of comb stages operating on a low sampling rate. The integrator section works on a high input data rate ensuing a large chip area and higher power consumption particularly when the decimation factor is high. Kwentus et al. [4] designed and fabricated a high-throughput programmable CIC decimation filter using carry-save arithmetic through CMOS process whose decimation factor varies in power of two ranges of 2 to 1024. Khoo et al. [5] proposed an efficient architecture utilizing the carry-save integrator stage in a high-speed CIC decimation filter depending on exploiting the carry propagation properties in a carry-save accumulator. Djadi et al. [6] developed a CIC structure based programmable decimation and interpolation digital filter that can be arranged either as a decimation filter or an interpolation filter with conversion ratio from 10 to 256 integer values. Yang and Snelgrove [7] decomposed the decimation ratio D into two factors, for implementing a CIC decimation filter, rather than using one CIC filter to decimate the high-speed digital signal.

Another way of implementing the CIC decimation filter was presented by Gao et al. [8] in which the decimation factor D was constrained to M-th power-of-two whereas in Dolecek et al. [9] developed a multiplierless CIC compensation filter based on the $2D$-order filter along with the sharpening technique. This method tries to improve the passband characteristic as well as the stop band of a symmetric non-recursive filter using the multiple copies of the same filter. A compensation filter design for the two-stage CIC decimation filter is presented in [10]. The design goal has two-folds: (i) to prevent the integrator section at a high input rate and (ii) to attain least wideband passband droop in the overall filter response. While using the polyphase decomposition of the filter at the first stage all filtering is moved to the reduced rate, which can be D times less than the input rate. Further, [11] was published on the enhancement of the decimation process through pipelining in recursive CIC filter structure with modified carry look-ahead adder (MCLA). It leads a high-speed CIC filter with maximum throughput of 190 MHz.

The sampled RF signal may require a high sampling rate which makes it extremely expensive in terms of processing requirements. Dolecek et al. [12] proposed an efficient modification in the arithmetic of the CIC-Cosine decimation filter. In their method, the coefficients of the compensator filter are presented in a CSD form. The newly designed structure can be implemented using only adders and shifts. A second-order compensator filter is introduced at a low rate in order to improve the passband of interest of overall filter. The resulting filter is a multiplier less filter and exhibits a high attenuation in the stop band, in addition to a low passband droop.

This paper presents an extension of the structure proposed

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by Dolecek et al. [12] using HSD number arithmetic along with the mathematical modeling of FIR and CIC decimation filter.

The rest of the paper is organized as follows. In Section II, we review the basic principles of the decimation process with the mathematical modeling of the FIR decimator. In Sections III & IV, we present the general theory of CIC decimation filter and its mathematical modeling respectively. In Section V, we discuss the preliminary work done on the design of compensation filter for efficient performance in various applications. Section VI is the key section of this work which describes the modification and extension of Compensated CIC-Cosine decimation filter [12] structure using HSD arithmetic. Section VII illustrates the efficient filter structure using the HSD number system with its performance. Finally, in Section VIII, an overall conclusion is discussed.

II. Preliminary Considerations of the Decimation Processes and Its Mathematical Modeling

Before proceeding towards the design of optimum decimators, it will be convenient to review some of the fundamental concepts of decimation in the context of digital signal processing as discussed in [1].

Altering the sampling rate implies that one discrete signal is changed into another discrete signal with a different sampling rate [3]. The process of decimating a signal $x\,[n]$ is depicted in Fig. 1. The original sampling rate is denoted as F_s and the final rate is then $\frac{F_s}{D}$. The *down-sampling* or decimation operation with a down-sampling factor D, where D is a positive integer, is implemented by discarding $D-1$ consecutive samples and retaining every D^{th} sample. Applying the down-sampling operation to the discrete signal $\{x[n]\}$, produces the down-sampled signal $\{y[m]\}$ i.e.

$$\{y[m]\} = \{x[mD]\} \tag{1}$$

The down-sampling process can be considered as a two-step operation.

1. In the first step, the original signal $\{x[n]\}$ is multiplied with the sampling function $\{s_D[n]\}$ defined by,

$$s_D[n] = \frac{1}{D}\sum_{k=0}^{D-1} W_D^{kn} = \begin{Bmatrix} 1 & for\ n = 0, \pm D, \pm 2D, \dots \\ 0 & otherwise \end{Bmatrix} \tag{2}$$

where $W_D = e^{-j2\pi/D}$ and evidently, $s_D[n]$ equals to 1 for $n = 0, \pm D, \pm 2D, \dots$ and equals to zero otherwise. Multiplying the sequence $\{x\,[n]\}$ by the sampling function $\{s_D[n]\}$ results in the intermediate signal $\{y_s[m]\}$,

$$y_s[m] = x[n]s_D[n] = \begin{Bmatrix} x[n] & for\ n = 0, \pm D, \pm 2D, \dots \\ 0 & other \end{Bmatrix} \tag{3}$$

2. In the second step, the zero valued samples in $\{y_s\,[m]\}$ are omitted, resulting in the down-sampled sequence $\{y\,[m]\}$,

$$y[m] = y_s[mD] = x[mD] \tag{4}$$

Frequency-domain representation of down-sampling is used to investigate the effects of the sampling rate alterations on the spectrum of the signal. Applying the z-transform on both sides of (1), we obtain,

$$\begin{aligned} Y(z) &= \sum_{m=-\infty}^{\infty} x[Dm]z^{-m} = \sum_{m=-\infty}^{\infty} y_s[Dm]z^{-m} \\ &= \sum_{m=-\infty}^{\infty} y_s[k]z^{-k/D} = Y_s\left(z^{1/D}\right) \end{aligned} \tag{5}$$

From (3), the z-transform $Y_s(z)$ is expressible by,

$$Y_s(z) = \sum_{n=-\infty}^{\infty} s_D[n]x[n]z^{-n} \tag{6}$$

Substituting (2) in (7) we obtain,

$$\begin{aligned} Y_s(z) &= \frac{1}{D}\sum_{n=-\infty}^{\infty}\left(\sum_{k=0}^{D-1} W_D^{kn}\right)x[n]z^{-n} \\ &= \frac{1}{D}\sum_{k=0}^{D-1}\left(\sum_{n=-\infty}^{\infty} x[n]\, W_D^{kn} z^{-n}\right) = \frac{1}{D}\sum_{k=0}^{D-1} X(zW_D^{-k}) \end{aligned} \tag{7}$$

According to (5) & (7), the desired input-output relation for the down-sampler is given by,

$$Y(z) = \frac{1}{D}\sum_{k=0}^{D-1} X\left(z^{1/D}\, W_D^{-k}\right) \tag{8}$$

Substituting $z = e^{jw}$ in (8), we get,

$$Y(e^{jw}) = \frac{1}{D}\sum_{k=0}^{D-1} X\left(e^{j(W-2\pi k)/D}\right) \tag{9}$$

Evidently, the spectrum $Y(e^{jw})$ is a sum of D uniformly shifted and stretched versions of $X(e^{jw})$ then scaled by a factor $1/D$. Equation (9) explicitly shows that the aliasing will occur when the bandwidth of the original signal exceeds π/D. Thus, only signals which are band-limited to π/D can be down-sampled without distortion. For the down-sampling factor D, the highest frequency in the spectrum of $X(e^{jw})$ denoted by w_H should be limited to $w_H \leq \pi/D$.

To satisfy the sampling theorem, a low-pass filter is introduced as an anti-aliasing filter to decrease the bandwidth of the signal prior to the downsampling. Down-sampling only changes the sample rate not the bandwidth of the signal. This means to avoid aliasing the factor-of-D decimation has to be implemented in two steps:

(1) Band limiting of the original signal to π/D.

(2) Down-sampling by the factor-of-D.

Fig. 1 shows the block diagram of a decimator implemented as a cascade of the decimation filter $H(z)$ also called antialiasing filter and the factor-of-D down sampler.

Fig. 1 illustrates the two-step description of the down-sampling operation. The role of the decimation filter $H\,(z)$ is to suppress aliasing to an acceptable range. Since the filter with an ideal frequency response cannot be achieved, some amount of aliasing should be tolerated.

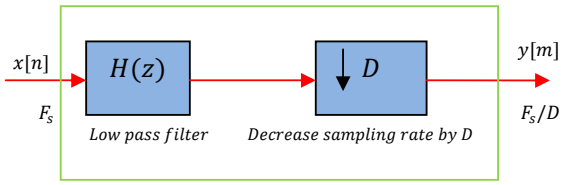

Fig. 1 Decimation Process

An extremely important consideration in the implementation of the sampling rate changing system is the choice of the type of low-pass filter [1]. In the conventional implementation, an FIR filter of length N is characterized by N coefficients, N multiplications and $N-1$ addition per output point. The computational efficiency is determined by the number of multiplications per input sample (MPIS) for the decimator. In the single-rate FIR filter with N no-zero coefficients, N multiplications are needed for computing one output sample. A traditional FIR decimator can be implemented efficiently by using a direct form structure or polyphase configuration of the filter length N with a decimation factor D. Assuming the sampling rate of the input signal is F_s then $N \times F_s$ multiplications is executed by every second and consequently, for decimation D, $\frac{N \times F_s}{D}$ multiplication must be carried out. For this type of system, a significant reduction in computation can be obtained as only one multiplication and addition must be performed for every Dth input point instead of N. The direct implementation filter structure can further transform to the computationally efficient structure by exploiting the linear phase coefficients symmetry property of filter coefficients i.e. $h[n] = h[N-n-1]$, which reduces the number of MPIS to $\frac{N \times F_s}{2D}$.

A polyphase structure of the FIR filter can be utilized to improve the overall system response. In this structure, the system transfer function is decomposed in two lower order transfer functions in the parallel form known as polyphase components, which are finally added together to compose the original transfer function.

Considering the transfer function of FIR filter is $H(z)$and given by,

$$H(z) = \sum_{n=0}^{N-1} h[n] z^{-n} \tag{10}$$

$$H(z) = h[0] + h[1]z^{-1} + h[2]z^{-2} + \cdots + h[N-2]z^{-(N-2)} + h[N-1]z^{-(N-1)} \tag{11}$$

$$= h[0] + h[2]z^{-2} + h[4]z^{-4} + \cdots + h[N-1]z^{-(N-1)} + z^{-1}(h[1] + h[3]z^{-2} + h[5]z^{-4} \ldots + h[N-2]z^{-(N-3)})$$

$$\text{or } H(z) = H_0(z^2) + z^{-1}H_1(z^2) \tag{12}$$

where

$$H_0(z) = h[0] + h[2]z^{-1} + h[4]z^{-2} + \cdots + h[N-1]z^{-(N-1)/2}$$

and

$$H_1(z) = h[1] + h[3]z^{-1} + h[5]z^{-2} \ldots + h[N-2]z^{-(N-3)/2})$$

In general, an N-length transfer function $H(z)$ can be decomposed into P polyphase branches $H_0(z), H_1(z), \ldots, H_{P-1}(z)$ in a manner that $H(z)$ is expressible in the form-

$$H(z) = \sum_{k=0}^{P-1} z^{-k} H_k(z^P) \tag{13}$$

where

$$H_k(z) = \sum_{n=0}^{\lfloor N/P \rfloor} h[Pn+k]z^{-n} \; ; \quad k = 0,1, \ldots \ldots P-1 \tag{14}$$

The down-sampling-by-D occurs at the inputs of the polyphase components $H_0(z), H_1(z), \ldots, H_{P-1}(z)$ and filtering is performed at sampling rate F_s/D and thus the overall computational complexity of the decimator is reduced by D.

III. CIC Decimation Filter

The CIC-filter is a multiplierless filter that uses limited storage, which is very good in an economic perspective. It was introduced by Hogenauer [3] for over two decades back and is used for interpolation and decimation. Furthermore, the filter does not require any storage for the filter coefficients and hence can be designed with only two basic building blocks, i.e. comb and integrator section. Unfortunately, the filter has an undesired passband droop due to the boxcar characteristic which often leads to the use of a conventional FIR filter for compensation.

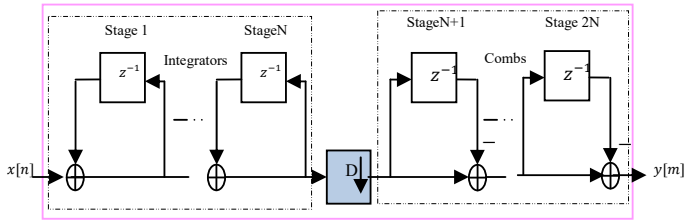

Fig. 2 CIC filter with comb and integrator stages

From Fig. 2, the CIC decimation filter consists of N Integrator and N comb stages, with a sampling rate change ratio D. The input signal is fed to the first integrator stage with a high sampling frequency Fs and is processed through N integrator stages. A down sampler between the integrator and comb stages select one sample out of D samples and fed it into

the first comb stage. This decimation process decreases the sampling rate of CIC decimation filter output Fs/D.

Considering the implementation aspects of CIC decimation filters, the integrator section has a unity feedback coefficient which will result to a register overflow in all integrator stages due to finite word length effects. However, the register overflow is of no consequence if following two conditions are met.

1. The filter is implemented with the two's complement arithmetic or signed digit arithmetic, which allows "wrap-around".
2. In the integrator section, the word-length has to be equal to or greater than $(I_W + N.log_2 D)$ bits, where I_W is the word-length in bits of the input signal.

The computational efficiency of an optimal sampling rate conversion system can be further improved by simplifying the arithmetic operation in different filter stage. Signed digit number system allows the parallel arithmetic that enhances the performance in terms of computational speed. In Section VI, we presented a signed digit number system approach to increase the decimation speed along with the compensation of passband droop using polyphase FIR filter structure.

IV. Mathematical Modeling of CIC Decimation Filter

As we have already mentioned that CIC decimation filter consists of N Integrator and N comb stages, with a sampling rate change ratio D, the transfer function of integrator stage in the z-domain is $\frac{1}{(1-z^{-1})}$ where as for comb section is $(1-z^{-1})$. Data is processed D times slower than the integrator stage, as the clock rate of comb stages is changed of Fs/D. Thus, the transfer function of comb stage, normalized to input sample rate, becomes $(1-z^{-D})$. Hence the overall transfer function of CIC decimation filter is given by-

$$H(z) = H_I^N(z)H_C^N(z) = \frac{(1-z^{-D})^N}{(1-z^{-1})^N} = \left[\frac{(1-z^{-1})(1+z^{-1}+\cdots\ldots+z^{-D+1})}{(1-z^{-1})}\right]^N = [\sum_{k=0}^{D-1} z^{-k}]^N \quad (15)$$

To implement this structure, $2N$ adders and $4N+2$ registers is required, whereas in conventional decimation structure, a total of $N*D$ adder and $N*(2D+1)$ registers are required and thus this implementation saves many adders and registers.

Assuming the Fourier transform of $x(n)$ signal is $X(w)$ and replacing z by e^{jw}, then the output of integrator section in frequency domain is given by-

$$X_1(w) = \left(\frac{1}{1-e^{-jw}}\right)^N . X(w) \quad (16)$$

and the output after down sampler is given by

$$X_2(w) = \frac{1}{D}\sum_{k=0}^{D-1} X_1\left[\frac{w-k.2\pi}{D}\right] = \frac{1}{D}\sum_{k=0}^{D-1}\left[\left(\frac{1}{1-e^{-j\frac{w-k.2\pi}{D}}}\right)^N . X(\frac{w-k.2\pi}{D})\right] = \frac{1}{D}\left[\left(\frac{1}{1-e^{-j(\frac{w}{D})}}\right)^N . X\left(\frac{w}{D}\right) + \left(\frac{1}{1-e^{-j(\frac{w-2\pi}{D})}}\right)^N . X\left(\frac{w-2\pi}{D}\right) + \cdots\right] \quad (17)$$

When $w \in \left[-\frac{\pi}{D}, \frac{\pi}{D}\right]$, then $X(w) = 0$, and (17) could be simplified to

$$X_2(w) = \frac{1}{D}\left[\left(\frac{1}{1-e^{-j(\frac{w}{D})}}\right)^N . X\left(\frac{w}{D}\right)\right] \quad (18)$$

For $2w_{max} < \pi/D$ the signal spectrum centered at $2\pi/D$ or $-2\pi/D$ and does not overlap with region $\left[-\frac{\pi}{D}, \frac{\pi}{D}\right]$.

The integrator section emphasizes on the low-frequency content of the input signal and attenuates the high-frequency component. As the number of integrator stages increases, the high-frequency attenuation increases and when the input is a stream of "1", the integrator output will cause overflow, but the comb stage is a high pass structure that attenuates low frequency components which makes the whole system more stable. The output signal spectrum can be given by

$$Y(w) = (1-e^{-jw})^N . X_2(w) \text{ or } Y(w) = \frac{1}{D}\left[\left(\frac{1-e^{-jw}}{1-e^{-j(\frac{w}{D})}}\right)^N . X\left(\frac{w}{D}\right)\right]$$

$$= \frac{1}{D}\left[\frac{e^{-j(\frac{w}{2})}}{e^{-j(\frac{w}{2D})}} . \left(\frac{e^{j(\frac{w}{2})} - e^{-j(\frac{w}{2})}}{e^{j(\frac{w}{2D})} - e^{-j(\frac{w}{2D})}}\right)^N . X\left(\frac{w}{D}\right)\right] \quad (19)$$

$$= \frac{1}{D} . \left(\frac{\sin\frac{w}{2}}{\frac{sinw}{2D}} . e^{-jw\left(\frac{1}{2}-\frac{1}{2D}\right)}\right)^N . X\left(\frac{w}{D}\right)$$

$$= \frac{1}{D} . \left(\left(\frac{\sin\frac{w}{2}}{\frac{sinw}{2D}}\right)^N . e^{-jNw\left(\frac{1}{2}-\frac{1}{2D}\right)}\right) . X\left(\frac{w}{D}\right) \quad (20)$$

For increasing N, the amplitude frequency response exhibits more attenuation in passband edge and (20) can be reduced to

$$Y(f) = \frac{1}{D^2} . \left(\left(\frac{\sin\frac{w}{2}}{\frac{sinw}{2D}}\right)^{2N}\right) \quad (21)$$

and if the rate change ratio D is large, then the amplitude response of CIC decimation filter $Y(f)$ in (21) can be simplified

$$Y_A(f) = \frac{1}{D^2} . \left(\left(\frac{\sin\frac{w}{2}}{\frac{w}{2D}}\right)^{2N}\right) \quad (22)$$

The error between $Y(f)$ and $Y_A(f)$ is less than 1 dB for $D \geq 10, 1 \leq N \leq 7$ and $0 \leq f \leq 255/256$.

V. Preliminary Work Done on the Design of Compensation Filter

In most applications, it is required to have a flat passband else the original signal may be destroyed. Unfortunately, due to the sinc-like characteristic, the CIC filter suffers with a passband droop, which is not acceptable in many cases. Hence, it is of a great interest to get a flat passband using a compensation filter. The compensation filter will take the form of the inverse of the CIC filter frequency response in the passband, and attenuate as much as possible in the stop band.

Various methods have been proposed by different researchers to compensate the passband droop with optimum performance.

- In 2009, Dolecek and Harris proposed the compensation for a wide bandwidth segment of the CIC main lobe [9]. In their method, the spectral response of the multiple CIC stages has been modified by a Taylor series expansion about zero frequencies dominated by its quadratic term. To improve the compensated gain response characteristics, they proposed the use of the sharpening technique using amplitude change function (ACF) between the amplitudes of the overall and the prototype filters which can be used to simultaneously improve the passband and stop band characteristics of a linear-phase FIR digital filter.
- Kim et al. [13] proposed the use of a CIC roll-off compensation filter in a W-CDMA digital IF receiver. The performance of the compensation filter relies on the value of compensation filter coefficients, which is attained by minimizing the consequent error function. This filter provides compensation in the wideband.
- Recently, in 2012, Pecotic et al. [15] presented a method for the design of finite-impulse-response CIC compensators whose coefficients are expressed as the sums of powers of two (SPT). The proposed technique is based on the minimax error criterion and to obtain the SPT coefficients, a universal optimization technique based on the interval analysis is used.
- Dolecek and Torres [12] proposed an altered and efficient interpretation of CIC Cosine decimation filter. A second-order compensator filter was introduced at a low rate to improve the passband of the overall filter. The compensator filter coefficients were represented in a CSD form that could be realized by means of only adders and shifts. Consequently, the resulting filter is a multiplier-free filter and exhibits a high attenuation in the stop band, as well as a low passband droop. The proposed filter in [14], [16]-[18] is the cascade of CIC filter with second order compensator filter which presents a trade-off between the desired compensation of the passband droop, and the complexity of the CSD representation.
- In 2011, Yasser et al. [19] proposed that the carry-propagation-free addition of the signed-digit number system can be utilized to implement FIR filters along with Booth-3 algorithm to speedup multipliers in the filter and thereafter a 1D filter is utilized to construct a 2D filter that can be assembled on real hardware in an image-processing application using this algorithm.

In the next section, we introduce the concept of signed digit number arithmetic discussed in [19], [20] in the new scenario to improve the passband characteristics and overall cost of compensation CIC decimation filter [12].

VI. Proposed Compensated CIC-HSD Decimation Filter

In this section, we presented an extension of the work done by Dolecek et al. [12] in a new context. To improve the passband of interest in the CIC Cosine decimation filter, Dolecek et al. [12] used CSD number system to represent the filter coefficient and overall structure that is implemented using only adders and shifts. But in CSD representation, a constraint is imposed that two non-zero CSD coefficient bits cannot acquire adjacent positions. This implies that at most 50% of all CSD bits must have non-zero values. This restriction implies that if the coefficient is partitioned into bits pairs, at the most one bit within each pair can be non-zero. Thus in the designed filter, each bit pair of the coefficient is represented by one data tap value and hence representing the quantized coefficients in the CSD form of compensation filter giving a desired passband compensation but with a higher cost in terms of the number of adder, area and power consumption.

In this work, the modification and extension have been done in three phases:

(i) First, we compensate the passband droop by cascading CIC decimation filter with FIR filter. The selection of the order and the number of stages of cascaded FIR filter should be optimum that gives a desired frequency response in the band of interest.

(ii) Second, in integrator section of CIC decimation filter, a high input data rate signal is added to a feedback signal and thus the resultant signal may overflow as well as carry propagation during the process. So in this phase the conventional adder present in integrator stage has been replaced by HSD adder. This modification speedups the decimation process by a factor of the distance of the signed bit position (shown in Fig. 3). In this design, the important issue is to define the word length of the input signal through which the whole decimation process, quantization process and selection of the position of the signed bit has to be done. Starting with signed bit position from one onward, the value of signed bit distance is increased until it satisfied the fast down sampling speed constraint without overflow at integrator stage. The adopted signed digit and hybrid signed algorithm limit the maximum length of carry propagation chain from fully parallel addition to any desired value.

(iii) Third, we introduce an efficient mechanism to design an efficient compensator which utilizes HSD to represent the quantized coefficient generated during the filtering process.

Signed–digit (SD) number representation enables us to limit carry propagation to a single-digit position, i.e. the carry propagation length is fixed irrespective of the word length by introducing redundancy in the system and has been employed to speedup arithmetic operations [21]. The proposed filter structure using a HSD algorithm (explained in Sections VI *A* & *B*) can be given by:

$$H(z)_{PropHSD} = [H_I^N(z)H_c^N(z)] * \left[H_{polyFIR}\right] = [H_I^N(z)H_c^N(z)] * [a_0 + a_1z^{-1} + a_2z^{-2} + a_3z^{-3} + a_4z^{-4} + a_5z^{-5}] \quad (23)$$

$$H(z)_{PropHSD} = [H_I^N(z)H_c^N(z)] * [a_0 + a_5z^{-5} + a_1z^{-1} + +a_4z^{-4} + a_2z^{-2} + a_3z^{-3}] \quad (24)$$

From Table IV, introducing the symmetry property of filter coefficients in (24),

$$H(z)_{PropHSD} = [H_l^N(z)H_c^N(z)] * [a_0(1+z^{-5}) + a_1(z^{-1} + z^{-4}) + a_2(z^{-2} + z^{-3})] \quad (25)$$

$$H(z)_{PropHSD} = [H_l^N(z)H_c^N(z)] * [|a_0|_{HSD}(1+z^{-5}) + |a_1|_{HSD}(z^{-1} + z^{-4}) + |a_2|_{HSD}(z^{-2} + z^{-3})] \quad (26)$$

This modified structure optimizes the overall performance in terms of gate delay, hardware complexity and cost in comparison to other efficient structures. In the next section, we present the basic theory of SD number arithmetic used in the designing of the proposed structure along with the rules for implementing the carry-free addition.

A. Redundant SD and HSD Adder Arithmetic

A symmetrical SD number can assume the following values, i.e. [–α,....,–1,0,1,....,α] where the maximum value of α for radix r must lie within the following range: [(r – 1)/2] ≤ α ≤ r – 1. In the conventional number systems fewer bits, switches and routing are required per digit, although the carry propagates along the entire word length where within the SD number system, more bits, switching devices and routing are essential per digit although the carry propagation is bound with a single-digit position. So a hybrid representation reveals a continuum of possible realizations that reduces the area for speed with the use of the conventional (binary) number system with SD number system arithmetic. In HSD number arithmetic, instead of insisting that every digit be a SD, some of the digits are being signed as well as leaving others unsigned and therefore, this representation limits the maximum length of carry propagation chains to any desired value between one to entire word length. Therefore, the area required in this representation decreases with the increase of the length of carry propagation chain. In addition, HSD representation requires the carry in between all digit positions (unsigned or signed) to assume any value from the set {-1, 0, 1} such as in SD system. The maximum length of a carry propagation chain would be $(d + 1)$, where d is the longest distance between neighboring SDs.

B. Rules for Selecting Intermediate Carry c_i and Sum s_i Based on $\alpha_i = m_i + n_i$ for Radix $r = 2b$ for SD and HSD Number System [20]

The signed-digit position bits produce an intermediate sum and a carry out on the bases of two input signed digits (i.e. m_i and n_i) and the two adjacent lower order unsigned digit position bits (i.e. m_{i-1} and n_{i-1}).

(i) When both signed-digit position bits i.e. m_i and n_i are 1 then the generated intermediate sum s_i and carry c_i are 0 and 1 respectively.

(ii) When both m_i and n_i are non-negative, only one input is non-zero and both m_{i-1} and n_{i-1} bits are non-negative, then the intermediate carry c_i and the intermediate sum s_i is 1 and $\bar{1}$ i. e. $\bar{b}$ respectively else 0 and 1 i.e. b.

(iii) When the addition of input bits m_i and n_i i.e. $\alpha_i = m_i + n_i$ is 0 then the generated intermediate sum s_i and carry c_i is 0.

(iv) When at least one input m_i or n_i is negative and zero and both m_{i-1} and n_{i-1} bits are non-negative, then the generated intermediate sum s_i and carry c_i is 0 and $\bar{1}$ for SD algorithm and $\bar{1}$ and b for HSD algorithm else $\bar{1}$ and 1 for SD and 0 and $\bar{b}$ for HSD algorithm respectively.

(v) When both m_i and n_i is non-positive, then the generated intermediate sum s_i and carry c_i are 0 and $\bar{1}$ respectively.

TABLE I
EXAMPLE OF HSD ADDITION

Notation		BSD	B	B	BSD	B	B	BSD	B	B
		*	-	-	*	-	-	*	-	-
m_i		1	0	1	−1	0	1	−1	0	1
n_i		0	1	1	−1	1	0	0	1	0
		1	1	2	−2	1	1	−1	1	1
c_i		−1			0			−1		
s_i	1			−1			0			
p_i (HSD)	1	−1	1	1	0	1	1	−1	1	1

HSD number system is a combination of unsigned binary (i.e. B) and signed binary (i.e.BSD) digits to represent a number. As shown in example 1, positions 2nd, 5th & 8th are signed bit binary whereas positions (0th, 1st), (3rd, 4th), & (6th, 7th) are in conventional binary.

- In binary number addition, when both bits are 1 then a carry will be produced while in signed digit (SD) number arithmetic, an intermediate sum and carry will be generated in such a way that the concluding addition becomes a parallel addition and the utmost length of a carry propagation chain is confined to the (longest) distance between adjoining signed digits. Therefore, the distance can be set to any desired value from one to the entire word length by choosing the position(s) of the signed digits.
- Signed digit number addition is performed through two steps. In the first step, an intermediate sum s_i and a carry c_i are generated parallel for all digit positions based on the operand digits m_i and n_i at each digit position i. In the second step, the summation $p_i = s_i + c_{i-1}$ is carried out to produce the final sum digit p_i. The most important fact is that there is always a possibility to select the intermediate sum s_i and carry c_{i-1} in such a way that the summation in the second step does not generate a carry [21].
- The position selection of the signed binary bits is the controlling factor to terminate the carry propagation chain.

Since the carry is not propagating through LSB to MSB, i.e. the carry propagation length is fixed irrespective of the word length, it will not require a full adder at 3,6,9… etc.... bit position when the distance (d) between the SD number is 2 and so HSD reduces the number of adders in overall design with the reduction in the area and as the second step can be executed in parallel for all those digit positions, it yields a fixed addition time, i.e. increase in computational speed, in addition to the word length.

VII. Filter Structure and Simulation Results

In this section, we presented the block level structure of the algorithm with its performance. Fig. 3 demonstrated the basic setup of CIC decimation filter with the inclusion of fast adder block replacing the adder block in basic CIC Decimator at Integrator stage. This implemented structure enhances the filter performance in terms of down sampling speed and register overflow, but still limiting with its passband droop. To compensate this droop, we implemented a CIC compensator by cascading the CIC Decimator with polyphase FIR filter as demonstrated in Fig. 4.

Example 1: Consider the design of a compensator for a cascaded CIC decimation filter with $N_{FIR} = 5, N_{CIC} = 2$ and decimation ratio $D = 64$. The -3 dB passband droop of the CIC filter at normalized frequency is 0.01257. Required passband droop should be minimum and response should be flat in the desired passband.

Fig. 5 & Table II present the overall magnitude response of CIC decimation [9], compensated CIC decimation [9] along with compensated CIC [12] and proposed compensated CIC decimation filter structure with its passband droop compensation respectively of specified parameters. In these figures, we clearly observed that the droop in the passband of the structure is significantly improved compared to [12].

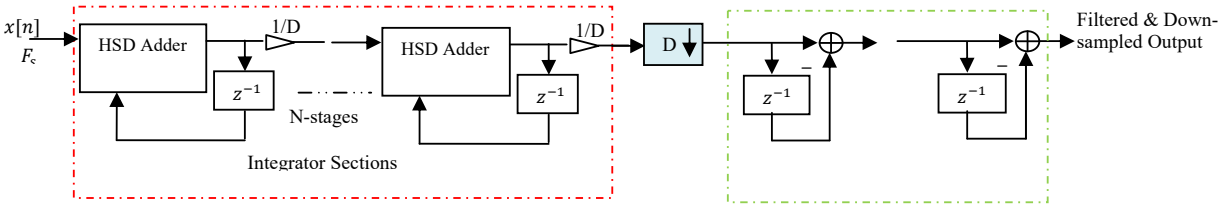

Fig. 3 Block level structure of CIC decimation filter

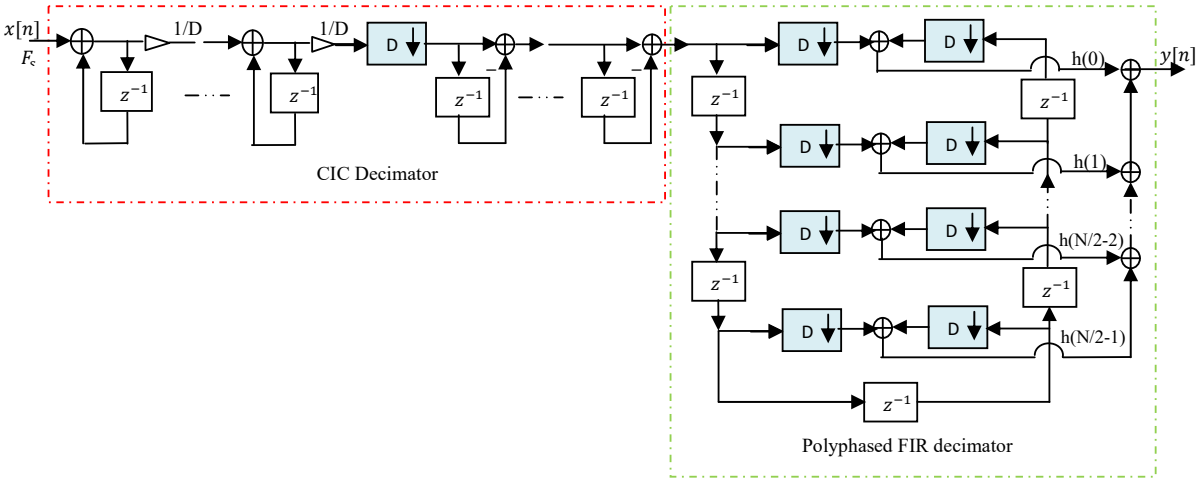

Fig. 4 Compensated CIC decimation Filter structure with polyphase FIR decimator

TABLE II
Passband-Droop Compensation Chart

Filter with decimation Factor (D) = 64	Magnitude (dB) of Passband droop at Normalized Frequency ($\times \pi \frac{rad}{sample}$)								
	0.02	0.1	0.2	0.25	0.3	0.4	0.5	0.6	0.7
CIC decimation Filter	-16.310	---	---	----	----	---	---	----	---
Compensated CIC decimation Filter	-0.0036	-4.774	---	----	----	---	---	----	---
Compensated CIC; Dolecek & Torres [12]	-0.0027	-0.3564	-8.277	-19.94	----	---	---	----	---
Proposed Compensated CIC Filter with HSD	-0.1585	-0.1035	-0.161	-0.447	-0.915	-2.508	-5.364	-10.254	-19.335

Table III & Fig. 6 illustrated the passband details of designed filter. It will clearly be observed that passband droop of CIC decimation filter is extremely large (approx. 16.31 dB) and sluggish without compensation, but once introducing the compensation technique, method demonstrates a steady response at higher frequencies (i.e. approx. 37.02% passband improvement at -3 dB) and starts deteriorating after 0.2 $\pi \frac{rad}{sample}$ frequency though the passband response of Dolecek & Torres [12] compensated CIC decimation filter carry a large droop i.e. 8.277 dB. For making this compensated model more efficient, we introduce signed & hybrid signed digit algorithm and basic ripple carry adder (RCA) algorithm in two phases: Firstly, in the integrator adder block and then in the quantized

FIR coefficients of compensated CIC decimator structure with input word length of 18, 20 and 22 bits.

The compensated structure presented in Fig. 4 with the modified concept given in (26) is properly analyzed in terms of gate delay, number of occupied slices and on-chip leakage power as shown in Fig. 7. It is observed that fully SD algorithm is taking the lower gate delay due to its fully parallel carry free addition property as explained in Section VI *B* by example. HSD algorithm, initially, consumes higher gate delay than RCA and SD but as the number of bits increases, the gate delay of RCA starts increasing rapidly due to carry propagation from LSB to MSB but in HSD, the signed position bits start playing their carry-free addition role and thus the gate delay start reducing in comparison to RCA algorithm as illustrated for 22 bit word length. Hence the compensated filter structure using HSD arithmetic is more efficient in terms of the gate delay by 38.6%, area by 57.5% and on-chip leakage power by 0.1% with SD respectively.

Table V revealed the overall cost in terms of the product of gate delay with the number of used slices and gate delay, number of used slices with on-chip leakage power and it is concluded that as the number of bits (word length) increases, the overall cost of compensated CIC decimation filter (i.e. 752.494) with HSD algorithm provides the most economical outcome in comparison to signed digit algorithm (i.e. 1063.992) and RCA (i.e. 755.921) algorithm. This cost can be further improved with the increase of word length because in the compensated filter with the fully SD algorithm, the chip area becomes a significant parameter to compensate while in RCA algorithm, the gate delay raises with fast rate and therefore, the compensated CIC decimation filter with HSD algorithm offers a tradeoff between its computational cost and down sampling speed.

Additionally, using the polyphase decomposition, the filters at the first stage can be moved at the lower rate and by increasing the number of stages, the amount of passband aliasing or imaging error can be brought within the required ranges.

TABLE III
PASSBAND-DETAILS CHART

Filter with decimation Factor (D) = 64	Normalized Frequency ($\times \pi \frac{rad}{sample}$) of Passband at Magnitude (dB)			
	At -1 dB	At -3 dB	At -5 dB	At -50 dB
CIC decimation Filter	0.0093	0.01257	0.0144	0.02490
Compensated CIC decimation Filter	0.04679	0.0801	0.10241	0.2369
Compensated CIC; Dolecek & Torres [12]	0.1224	0.1564	0.17700	0.3046
Proposed Compensated CIC Filter with HSD	0.3083	0.4224	0.49076	0.7828

TABLE IV
POLYPHASE FIR FILTER COEFFICIENTS

a_0	a_1	a_2	a_3	a_4	a_5
0.1148	0.3302	0.2331	0.2331	0.3302	0.1148

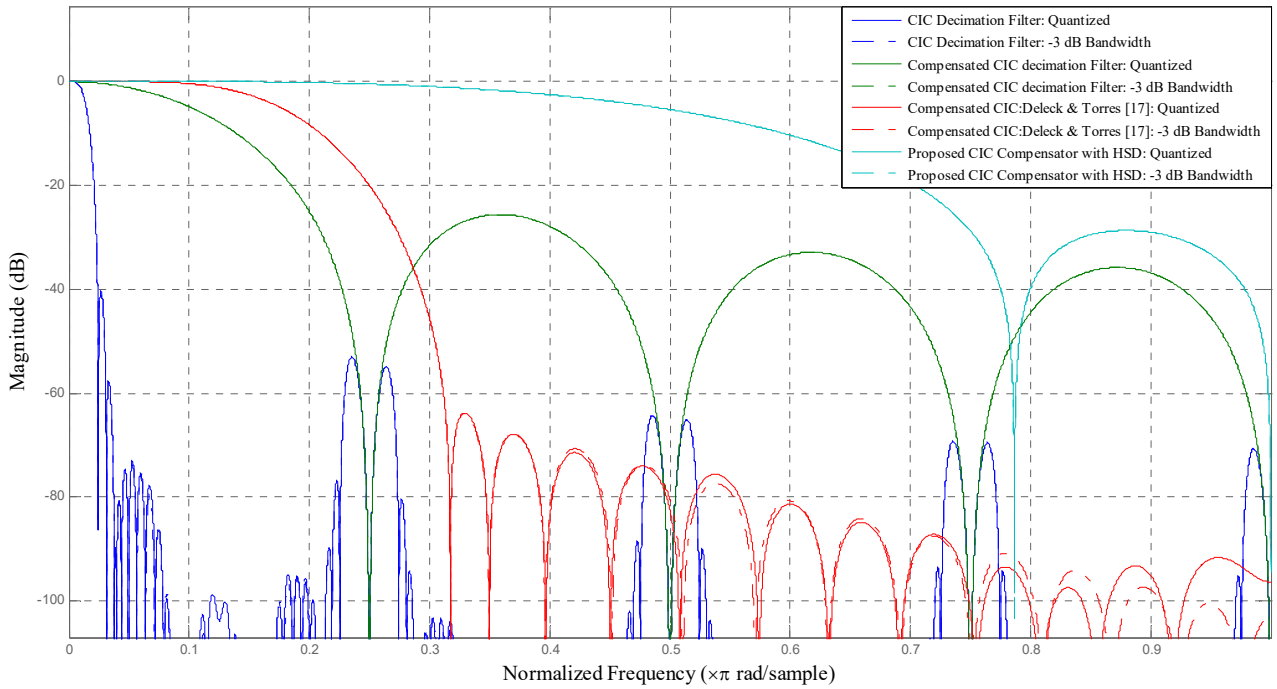

Fig. 5 Overall Magnitude Response

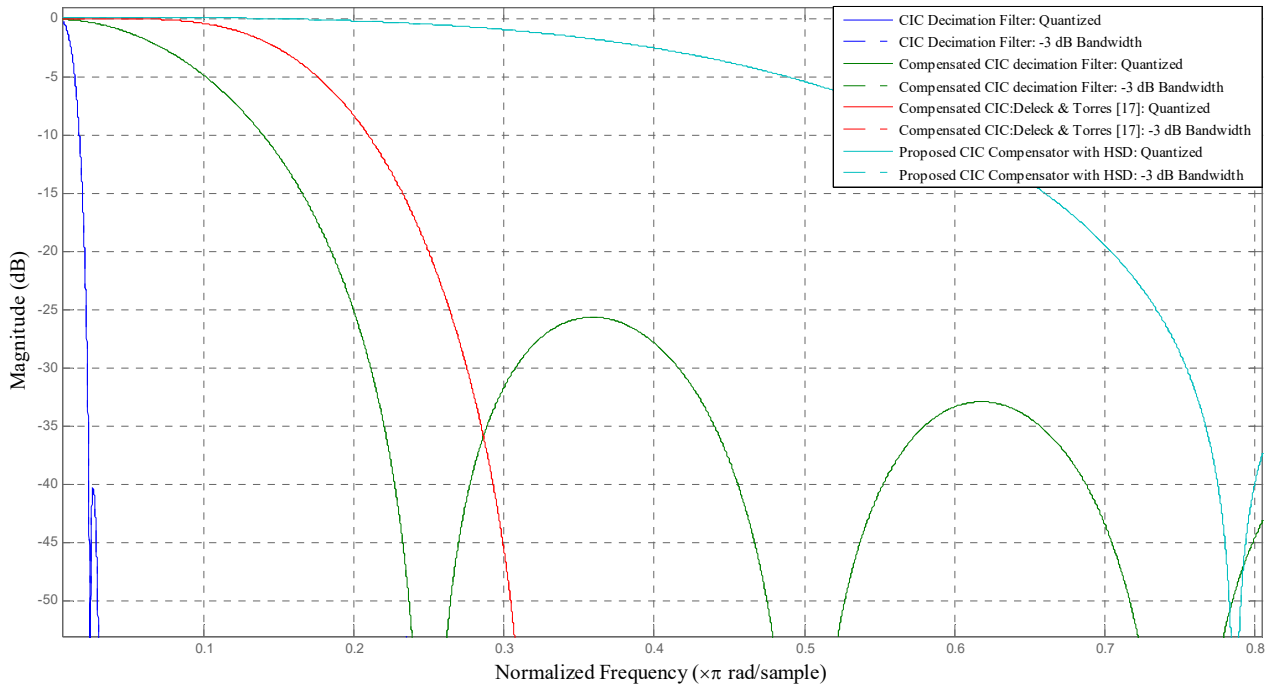

Fig. 6 Passband details (-3dB down): Zoom View

TABLE V
COST CHART (GATE DELAY X NUMBER OF OCCUPIED SLICES AND GATE DELAY X NUMBER OF OCCUPIED SLICES X ON-CHIP LEAKAGE POWER) WITH THE NUMBER OF BITS

Number of Bits	Gate Delay X Number of Occupied Slice			Gate Delay X Number of Occupied Slices X On-chip leakage power		
	RCA	SD	HSD	RCA	SD	HSD
18-Bits	356.34	787.848	536.79	1178.06	2606.201	1776.238
20-Bits	512.012	904.877	675.989	1693.736	2992.428	2237.524
22-Bits	755.921	1063.992	752.494	2498.319	3523.942	2491.508

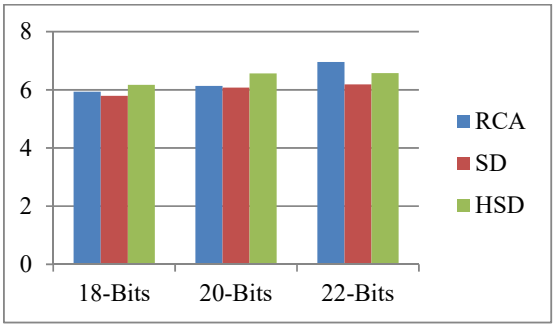

Fig. 7 (a) Gate Delay (nsec.) of Compensated CIC filter with fast adder algorithms

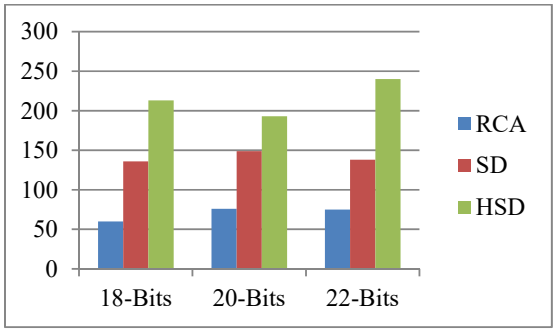

Fig. 7 (b) Number of Occupied Slices of Compensated CIC filter with fast adder algorithm

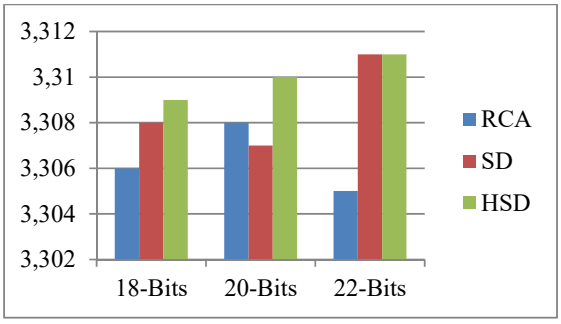

Fig. 7 (c) On Chip Power Leakage (W) of Compensated CIC filter with fast adder algorithm

VIII. Conclusions

We discussed here the issues related to the mathematical modeling of multirate multistage decimator design and also presented a modified view to extend the work proposed by [12] in the new scenario. The proposed implementation of compensated CIC decimation filter with the HSD algorithm, initially compensated the passband droop by 37.02% than compensated CIC filter designed in [12] using the CSD number system, and then it achieves a high throughput in terms of down sampling speed by 65.15% than RCA, area and power by 57.5% and 0.01% than SD algorithms respectively. The inclusion of HSD arithmetic in proposed compensation filter design can control the overall performance in terms of area and speed at the frequencies of interest. This newly designed structure provides an optimum solution for all signal-processing applications which require sampling rate conversion with higher speed and lesser area such as image and speech processing.

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